Ordering number : EN5262

NMOS LSI

LM7001J, 7001JM

Direct PLL Frequency Synthesizers for Electronic Tuning

Features

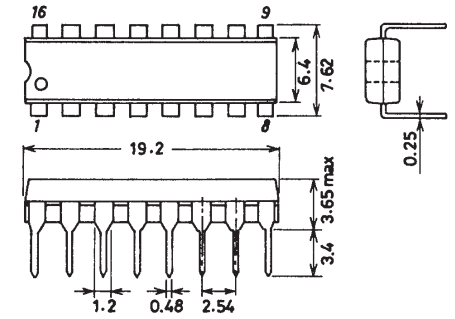
- The LM7001J and LM7001JM are PLL frequency synthesizer LSIs for tuners, making it possible to make up high-performance AM/FM tuners easily.
- These LSIs are software compatible with the LM7000, but do not include an IF calculation circuit.
- The FM VCO circuit includes a high-speed programmable divider that can divide directly.
- Seven reference frequencies: 1, 5, 9, 10, 25, 50, and 100 kHz
- Band-switching outputs (3 bits)
- Controller clock output (400 kHz)
- Clock time base output (8 Hz)
- Serial input circuit for data input (using the CE, CL, and DATA pins)

Package Dimensions

unit: mm

3006B-DIP16

[LM7001J]

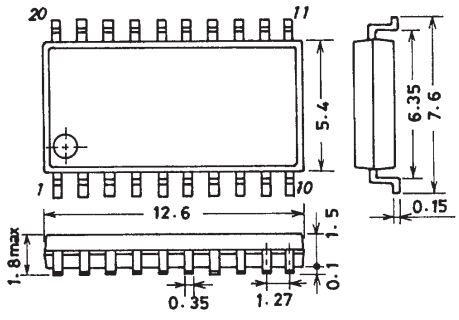


SANYO: DIP16

unit: mm

3036B-MFP20

[LM7001JM]

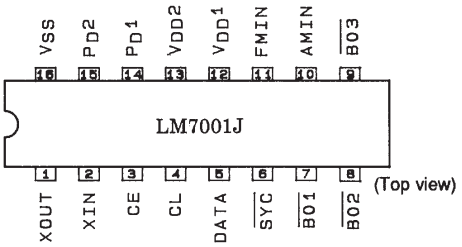


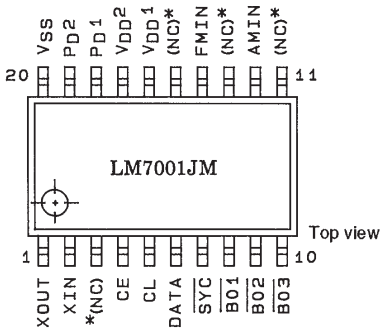
SANYO: MFP20

SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquarters

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Pin Assignments





Note: * NC pins must be left open.

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	$V_{DD}1$, $V_{DD}2$	–0.3 to +7.0	V
Maximum input voltage	$V_{IN}1$ max	CE, CL, DATA	–0.3 to +7.0	V
	$V_{IN}2$ max	Input pins other than $V_{IN}1$	–0.3 to V_{DD} + 0.3	V
Maximum output voltage	$V_{OUT}1$ max	$\overline{SYC}$	–0.3 to +7.0	V
	$V_{OUT}2$ max	$\overline{BO1}$ to $\overline{BO3}$	–0.3 to +13	V
	$V_{OUT}3$ max	Output pins other than $V_{OUT}1$ and $V_{OUT}2$	–0.3 to V_{DD} + 0.3	V
Maximum output current	I_{OUT} max	$\overline{BO1}$ to $\overline{BO3}$	0 to 3.0	mA
Allowable power dissipation	Pd max	Ta = 85°C: LM7001J (DIP16)	300	mW
		Ta = 85°C: LM7001JM (MFP20)	180	mW
Operating temperature	Topr		–40 to +85	°C
Storage temperature	Tstg		–55 to +125	°C

Allowable Operating Ranges at Ta = –40 to +85°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{DD}1$	$V_{DD}1$, PLL circuit operating	4.5 to 6.5	V
	$V_{DD}2$	$V_{DD}2$, crystal oscillator time base	3.5 to 6.5	V
Input high-level voltage	V_{IH}	CE, CL, DATA	2.2 to 6.5	V
Input low-level voltage	V_{IL}	CE, CL, DATA	0 to 0.7	V
Output voltage	$V_{OUT}1$	$\overline{SYC}$	0 to 6.5	V
	$V_{OUT}2$	$\overline{BO1}$ to $\overline{BO3}$	0 to 13	V
Output current	I_{OUT}	$\overline{BO1}$ to $\overline{BO3}$, V_{DD} = 4.5 to 6.5 V	0 to 3.0	mA
Input frequency	$f_{IN}1$	XIN, sine wave, capacitor coupled	1.0 to 7.2 typ to 8.0	MHz
	$f_{IN}2$	FMIN, sine wave, capacitor coupled*1, s*3 = 1	45 to 130	MHz
	$f_{IN}3$	FMIN, sine wave, capacitor coupled*2, s*3 = 1	5 to 30	MHz
	$f_{IN}4$	AMIN, sine wave, capacitor coupled, s*3 = 0	0.5 to 10	MHz
Crystal element for guaranteed oscillation	Xtal	XIN to XOUT, CI ≤ 30 Ω	5.0 to 7.2 typ to 8.0	MHz
Input amplitude	$V_{IN}1$	XIN, sine wave, capacitor coupled	0.5 to 1.5	Vrms
	$V_{IN}2$	FMIN, sine wave, capacitor coupled	0.1 to 1.5	Vrms
	$V_{IN}3$	AMIN, sine wave, capacitor coupled	0.1 to 1.5	Vrms

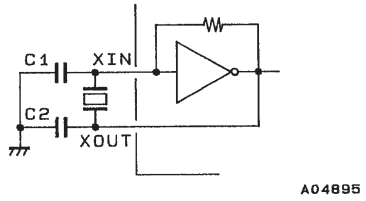
Note: 1. f_{ref} = 25, 50, or 100 kHz
2. f_{ref} = Reference frequencies other than those for *1.
3. "s" refers to the control bit in the serial data.

Electrical Characteristics in the Allowable Operating Ranges

Parameter	Symbol	Conditions	min	typ	max	Unit
Built-in feedback resistance	R_{f1}	XIN		1.0		MΩ
	R_{f2}	FMIN		500		kΩ
	R_{f3}	AMIN		500		kΩ
Input high-level current	I_{IH}	CE, CL, DATA: V_{IN} = 6.5 V			5.0	µA
Input low-level current	I_{IL}	CE, CL, DATA: V_{IN} = 0 V			5.0	µA
Output low-level voltage	$V_{OL}1$	FMIN, AMIN: I_{OUT} = 0.5 mA			3.5	V
	$V_{OL}2$	$\overline{SYC}$: I_{OUT} = 0.1 mA, *1	0.02		0.3	V
	$V_{OL}3$	$\overline{BO1}$ to $\overline{BO3}$: I_{OUT} = 2.0 mA			1.0	V
	$V_{OL}4$	P_D1, P_D2: I_{OUT} = 0.1 mA			0.3	V
Output off leakage current	$I_{OFF}1$	$\overline{SYC}$: V_{OUT} = 6.5 V			5.0	µA
	$I_{OFF}2$	$\overline{BO1}$ to $\overline{BO3}$: V_{OUT} = 13 V			3.0	µA
Output high-level voltage	V_{OH}	P_D1, P_D2: I_{OUT} = –0.1 mA	0.5 V_{DD}			V
High-level 3-state off leakage current	I_{OFFH}	P_D1, P_D2: V_{OUT} = V_{DD}		0.01	10.0	nA
Low-level 3-state off leakage current	I_{OFFL}	P_D1, P_D2: V_{OUT} = 0 V		0.01	10.0	nA
Current drain	$I_{DD}1$	$V_{DD}1$ + $V_{DD}2$: *2		25	40	mA
	$I_{DD}2$	$V_{DD}2$: PLL block stopped		2.0	3.5	mA
Input capacitance	C_{IN}	FMIN	1	2	3	pF

Note: 1. V_{DD} = 3.5 to 6.5 V
2. With a 7.2 MHz crystal connected between XIN and XOUT, $f_{IN}2$ = 130 MHz, $V_{IN}2$ = 100 mVrms, other input pins at V_{SS}, output pins open.

Oscillator Circuit Example

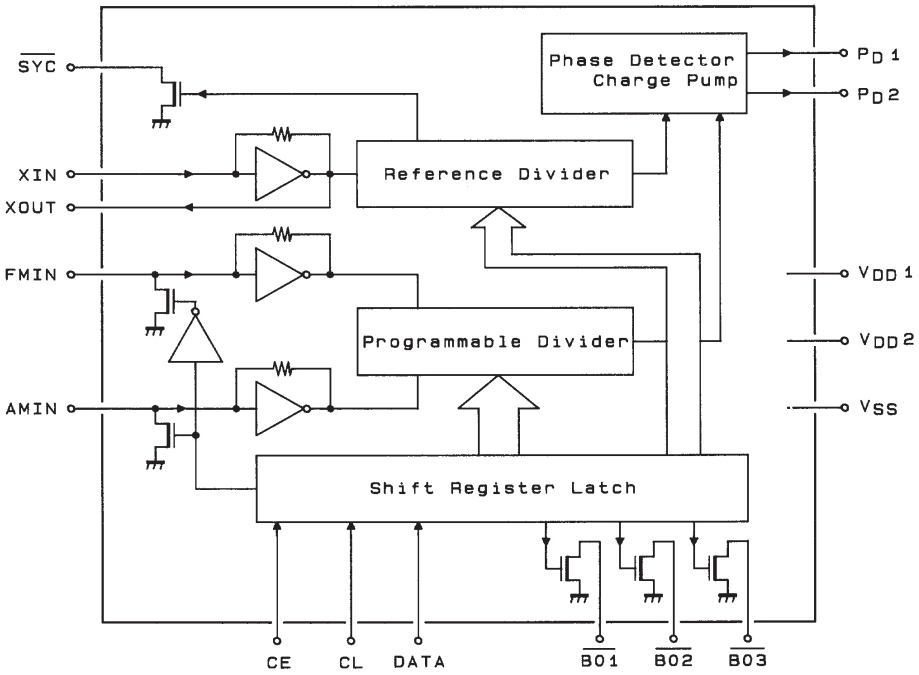


Kinseki, Ltd.
HC43/U: 2114-84521 (1): CL = 10 pF, C1 = 15 (10 to 22) pF, C2 = 15 pF
HC43/U: 2114-84521 (2): CL = 16 pF, C1 = 22 (15 to 33) pF, C2 = 33 pF

Nihon Denpa Kogyou, Ltd.
NR-18: LM-X-0701: CL = 10 pF, C1 = 15 pF, C2 = 15 pF

Since the circuit constants in the crystal oscillator circuit depend on the crystal element used and the printed circuit board pattern, we recommend consulting with the manufacturer of the crystal element concerning this circuit.

Equivalent Circuit Block Diagram



Pin Functions

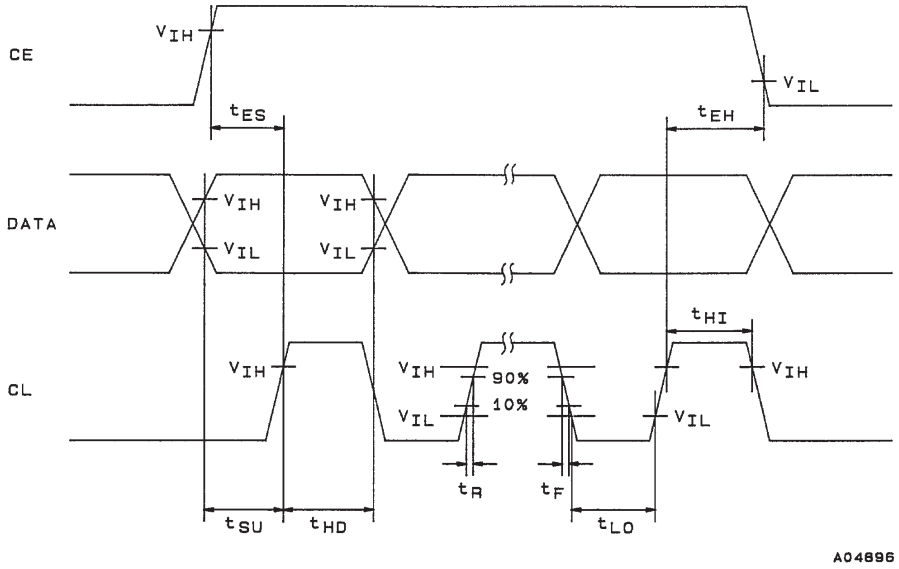
Symbol	Description
$\overline{SYC}$	Controller clock (400 kHz)
XIN, XOUT	Crystal oscillator (7.2 MHz)
FMIN, AMIN	Local oscillator signal input
CE, CL, DATA	Data input
$\overline{BO1}$ to $\overline{BO3}$	Band data output. $\overline{BO1}$ can be used as a time base output (8 Hz).
$V_{DD}1$, $V_{DD}2$, V_{SS}	Power supply (Apply power to both $V_{DD}1$ and $V_{DD}2$ when the PLL circuit is operating. $V_{DD}2$ is the crystal oscillator and time base power supply. Internal data cannot be maintained on $V_{DD}2$ only.)
P_D1, P_D2	Charge pump output

Data Input Timing

V_{IH} = 2.2 to 6.5 V, V_{IL} = 0 to 0.7 V, Xtal = 5.00 to 7.20 (typ) to 8.00 MHz

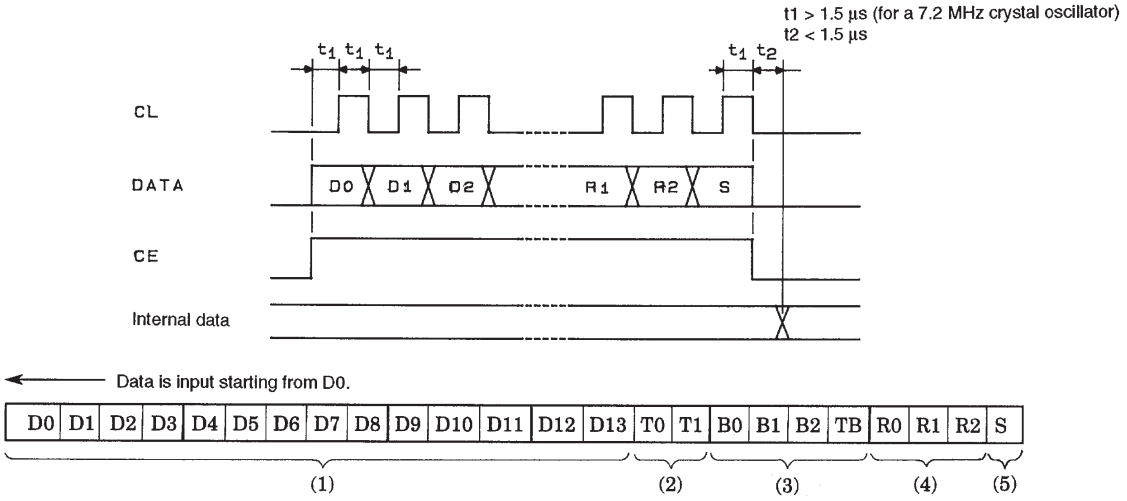
Data acquisition: On the CL rising edge ⌐↑

Note: Data transfers must be started only after the crystal oscillator is operating normally, i.e., after a proper input signal has been supplied to XIN.



Parameter	Symbol	Xtal: 7.20 MHz	Xtal: for frequencies other than 7.2 MHz	Example: XIN = 2.048 MHz
Enable setup time	t_{ES}	At least 1.5 µs	At least $[\frac{1 \times 8}{f\ Xtal}] \times 1.35$	At least 5.27 µs
Enable hold time	t_{EH}	At least 1.5 µs	At least $[\frac{1 \times 8}{f\ Xtal}] \times 1.35$	At least 5.27 µs
Data setup time	t_{SU}	At least 1.5 µs	At least $[\frac{1 \times 8}{f\ Xtal}] \times 1.35$	At least 5.27 µs
Data hold time	t_{HD}	At least 1.5 µs	At least $[\frac{1 \times 8}{f\ Xtal}] \times 1.35$	At least 5.27 µs
Clock low-level time	t_{LO}	At least 1.5 µs	At least $[\frac{1 \times 8}{f\ Xtal}] \times 1.35$	At least 5.27 µs
Clock high-level time	t_{HI}	At least 1.5 µs	At least $[\frac{1 \times 8}{f\ Xtal}] \times 1.35$	At least 5.27 µs
Rise time	t_R	Up to 1 µs	Up to 1 µs	Up to 1 µs
Fall time	t_F	Up to 1 µs	Up to 1 µs	Up to 1 µs

Data Input



(1) D0 (LSB) to D13 (MSB): Divisor data
FMIN uses D0 to D13 and AMIN uses D4 to D13.

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	
1	1	1	1	0	1	1	1	1	1	0	0	0	0	→ Example ①: FMIN divisor = 1007
LSB													MSB	
X	X	X	X	1	0	0	0	1	0	0	1	0	0	→ Example ②: AMIN divisor = 145
				LSB									MSB	

Sample calculation

① FM 100 kHz steps (f_{ref} = 100 kHz)
FM VCO = 100.7 MHz (FM RF = 90.0 MHz, IF = 10.7 MHz)
Divisor = 100.7 MHz (FM VCO) ÷ 100 kHz (f_{ref}) = 1007 → $3EF_{(HEX)}$

② AM 10 kHz steps (f_{ref} = 10 kHz)
AM VCO = 1450 kHz (AM RF = 1000 kHz, IF = 450 kHz)
Divisor = 1450 kHz (AM VCO) ÷ 10 kHz (f_{ref}) = 145 → $91_{(HEX)}$

(2) T0 and T1 are LSI test bits and both should be set to 0.

(3) B0 to B2, TB: Band data
Time base data

Note: *: Determined by R0 to R3. See item (4) on next page.

Input				Output		
B0	B1	B2	TB	$\overline{BO1}$	$\overline{BO2}$	$\overline{BO3}$
0	0	0	0	*	*	*
0	0	1	0	0	0	1
0	1	0	0	0	1	0
0	1	1	0	0	1	1
1	0	0	0	1	0	0
1	0	1	0	1	0	1
1	1	0	0	1	1	0
1	1	1	0	1	1	1
0	0	0	1	TB	*	*
×	1	0	1	TB	1	0
×	0	1	1	TB	0	1
×	1	1	1	TB	1	1
1	0	0	1	TB	0	0

×: Don't care
TB: 8 Hz

(4) R0 to R2: Reference frequency data

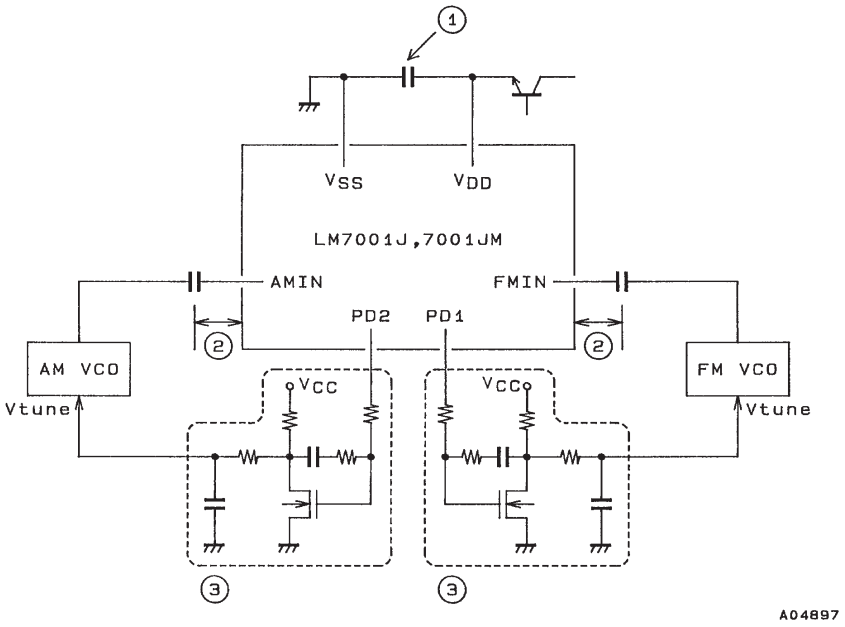
R0	R1	R2	f_{ref} [kHz]	$\overline{BO1}$	$\overline{BO2}$	$\overline{BO3}$
0	0	0	100	1	1	0
0	0	1	50	1	1	0
0	1	0	25	1	1	0
0	1	1	5	0	0	1
1	0	0	10	1	0	1
1	0	1	9	1	0	1
1	1	0	1	0	1	1
1	1	1	5	0	0	1

Note: The values listed for $\overline{BO1}$, $\overline{BO2}$, and $\overline{BO3}$ are for the case when the B0 to B2 data is set to all zeros.

(5) S: Divider selection data
1: FMIN, 0: AMIN

Notes on PLL IC Usage

1. PLL IC printed circuit board patterns



① Power supply pins
A capacitor must be inserted between the V_{DD} and V_{SS} power supply pins for noise exclusion. This capacitor must be located as close as possible to these pins.

② FMIN and AMIN pins
The coupling capacitors must be located as close as possible to these pins.

③ PD pins, low-pass filter
Since those are high-impedance pins, they are susceptible to noise. Therefore, the pattern should be kept as short as possible and the area around this circuit should be covered by the ground pattern.

2. Initial states of the output ports ($\overline{BO1}$ to $\overline{BO3}$)
The initial states of the output ports after power is applied are undefined until data has been transferred.
In particular, it is possible for the $\overline{BO1}$ and $\overline{BO3}$ pins to output the internal clock, so data must be transferred as soon as possible.
However, note that the LSI cannot accept data until the crystal oscillator is operating normally.

3. VCO
   The VCO circuit is designed so that it does not stop oscillating even if the control voltage (Vtune) becomes 0 V. (This is because the PLL circuit could become deadlocked if the VCO stopped.)