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S-8491 Series

The S-8491 is a series of lithium-ion rechargeable battery protection ICs incorporating high-accuracy voltage detectors and a delay circuit. This series is suitable for protecting a single-cell pack.

■ Features

(1) Built-in high-accuracy voltage detection circuits:

① Excess charge detection voltage V_{CU} .. 4.35 ± 0.05 V to 4.25 ± 0.05 V/0.05 V step

② Excess charge release voltage V_{CD} ..... 4.15 ± 0.13 V to 3.95 ± 0.13 V/0.05 V step

* The difference between the excess charge detection voltage and the excess charge release voltage can be selected in the range of 0.2 V to 0.3 V.

③ Excess discharge detection voltage V_{DD} ..... 2.30 ± 0.10 V

④ Excess discharge release voltage V_{DU} ..... 3.00 ± 0.15 V to 2.40 ± 0.15 V/0.10 V step

⑤ Excess current detection voltage V_{IOV} ..... 0.20 ± 0.06 V

(2) Built-in delay circuit

The excess charge, excess discharge or excess current is detected with delay.

(3) Ultra-low current consumption

Operation: 15.0 μA max. (+25 °C)
Power down: 0.48 μA max. (+25 °C)

(4) SOT - 89 - 5 package

■ Selection Guide

S - 8491AUP - DKA - T2

- T2: Direction of the IC [Refer to the tape specifications (T2)]
- DKA: Abbreviation
- UP: SOT - 89 - 5 package

Table 1

Product \ Item	Excess charge detection voltage	Excess charge release voltage	Excess discharge release voltage
S-8491AUP-DKA-T2	4.30 ± 0.05 V	4.00 ± 0.13 V	3.00 ± 0.15 V
S-8491BUP-DKB-T2	4.35 ± 0.05 V	4.10 ± 0.13 V	3.00 ± 0.15 V
S-8491CUP-DKC-T2	4.25 ± 0.05 V	4.05 ± 0.13 V	2.70 ± 0.15 V
S-8491DUP-DKD-T2	4.25 ± 0.05 V	4.05 ± 0.13 V	2.40 ± 0.15 V

Characteristics not specified in Table 1 apply commonly to the S-8491AUP/BUP/CUP/DUP.

■ Block Diagram

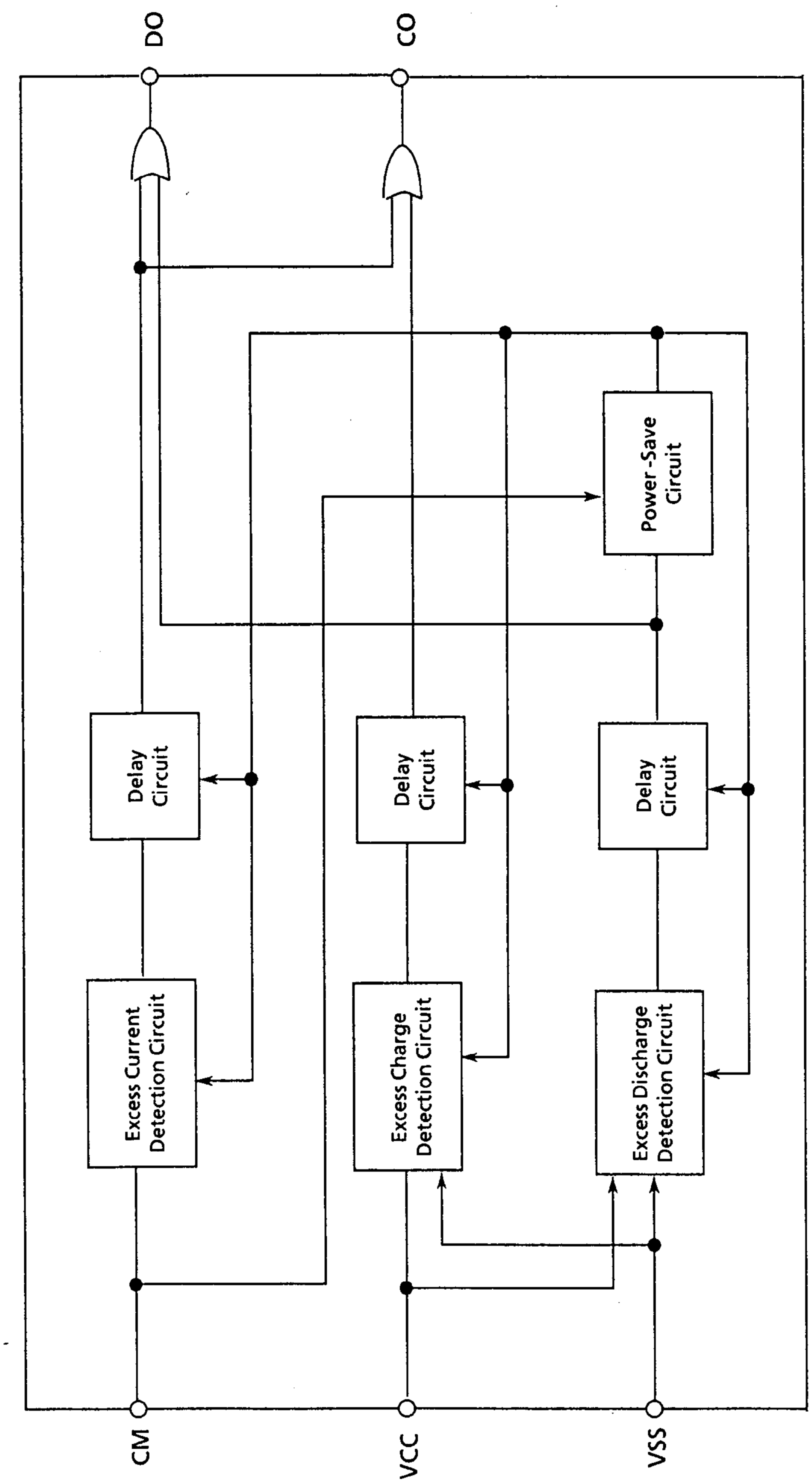
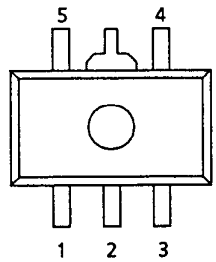


Figure 1

■ Pin Assignment

SOT-89-5
Top view



1. CO
2. VCC
3. DO
4. VSS
5. CM

Figure 2

■ Functions of Pins

- V_{CC} (Pin No. 2) .... Input
  Power supply pin at the positive side of the IC. :

- V_{SS} (Pin No. 4) .... Input
  Power supply pin at the negative side of the IC.

- DO (Pin No. 3) .... Output (CMOS)
  Gate connection pin for the discharge control Nch-FET. It turns OFF the gate during excess charge or excess current, whereas it turns ON the gate in the excess charge or the normal region.

- CO (Pin No. 1) .... Output (Pch open-drain)
  Gate connection pin for the charge control Nch-FET. This pin turns ON the gate in the excess current region, whereas it turns ON the gate in the normal or excess discharge region.

- CM (Pin No. 5) .... Input
  Voltage detection pin (between CM and V_{SS}). Detects the discharge current value of the battery due to a drop in the voltage of the FET.

■ Absolute Maximum Ratings

Table 2

Ta = 25°C

Item	Symbol	Ratings	Unit
Input voltage between $V_{CC}-V_{SS}$ Input voltage between V_{CC} − CM	V_{DS} V_{CM}	$V_{SS}-0.3$ to $+18$ $V_{CC}+0.3$ to -18	V
Input voltage between DO − V_{SS} Input voltage between V_{CC} − CO	V_{DOS} V_{COD}	$V_{SS}-0.3$ to $V_{CC}+0.3$ $V_{CC}+0.3$ to -18	V
Power dissipation	PD	500	mW
Operating temperature range	Topr	−20 to +60	°C
Storage temperature range	Tstg	−40 to +125	°C

■ Electrical Characteristics

Table 3

Ta = 25°C

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Excess charge detection voltage	V_{CU}	Measurement 1	AUP	4.25	4.30	4.35	V
			BUP	4.30	4.35	4.40	
			CUP	4.20	4.25	4.30	
			DUP	4.20	4.25	4.30	
Excess charge release voltage	V_{CD}	Measurement 1	AUP	3.87	4.00	4.13	
			BUP	3.97	4.10	4.23	
			CUP	3.92	4.05	4.18	
			DUP	3.92	4.05	4.18	
Excess discharge detection voltage	V_{DD}	Measurement 1		2.20	2.30	2.40	
Excess discharge release voltage	V_{DU}	Measurement 1	AUP	2.85	3.00	3.15	
			BUP	2.85	3.00	3.15	
			CUP	2.55	2.70	2.85	
			DUP	2.25	2.40	2.55	
Excess current detection voltage	V_{IOV}	Measurement 6		0.14	0.20	0.26	
Temperature coefficient of the detection voltage	T_{COE}	Ta = −20 to +60		−1.5	——	+1.5	mV/°C
Delay time of excess charge detection	T_{CU}	Measurement 2		0.5	——	5.0	ms
Delay time of excess discharge detection	T_{DD}	Measurement 2		0.5	——	5.0	
Delay time of excess current detection	T_{OFF}	Measurement 2		0.5	——	5.0	
Input voltage between V_{CC} and V_{SS}	V_{DS}	——		−0.3	——	16	V
Input voltage between V_{CC} and CM	V_{CM}	Note 1		+0.3	——	−16	
Operating voltage between V_{CC} and V_{SS}	V_{DSOP}	——		2.0	——	16	
Normal operating current consumption	I_{OPE}	Measurement 3		——	3.50	15	μA
Power-down current consumption	I_{PDN}	Measurement 3		——	0.25	0.48	
DO 'H' voltage	$V_{DO(H)}$	Measurement 4		V_{CC} − 0.5	——	——	V
DO 'L' voltage	$V_{DO(L)}$	Measurement 4		——	——	V_{SS} + 0.1	
CO 'H' voltage	$V_{CO(H)}$	Measurement 5		V_{CC} − 0.5	——	——	

Note 1: The V_{CC} pin-based voltage supplied to the CM pin.

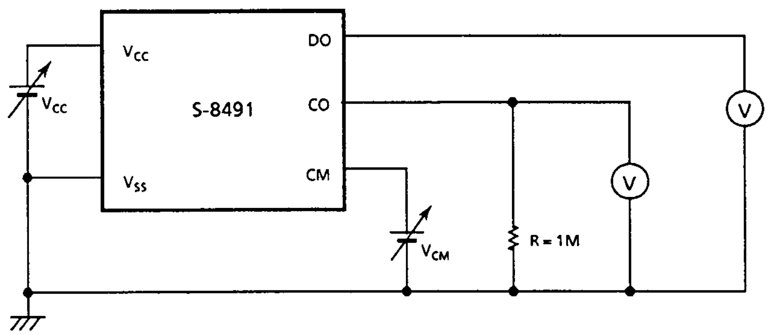
Table 4

Ta = −20 to 60 °C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Temperature coefficient of detection voltage	T_{COE}	Ta = −20 to +60	−1.5	——	+1.5	mV/°C
Delay time of excess charge detection	T_{CU}	Measurement 2	0.5	——	5.0	ms
Delay time of excess discharge detection	T_{DD}	Measurement 2	0.5	——	5.0	ms
Delay time of excess current detection	T_{OFF}	Measurement 2	0.5	——	5.0	ms
Normal operating current consumption	I_{OPE}	Measurement 3	——	3.50	20	μA
Power down current consumption	I_{PDN}	Measurement 3	——	0.25	0.58	μA
DO 'H' voltage	$V_{DO(H)}$	Measurement 4	V_{CC} − 0.5	——	——	V
DO 'L' voltage	$V_{DO(L)}$	Measurement 4	——	——	V_{SS} + 0.1	V
CO 'H' voltage	$V_{CO(H)}$	Measurement 5	V_{CC} − 0.5	——	——	V

■ Measurement Circuits

(1) Measurement 1



To measure excess charge detection voltage V_{CU}, excess charge release voltage V_{CD}, excess discharge detection voltage V_{DD}, and excess discharge release voltage V_{DU}, follow these steps:

① In the normal region with $V_{CC} = V_{CD}$, $V_{CM} = 0$ V, excess charge detection voltage V_{CU} is the voltage of V_{CC} when CO goes low after gradually increasing V_{CC}.

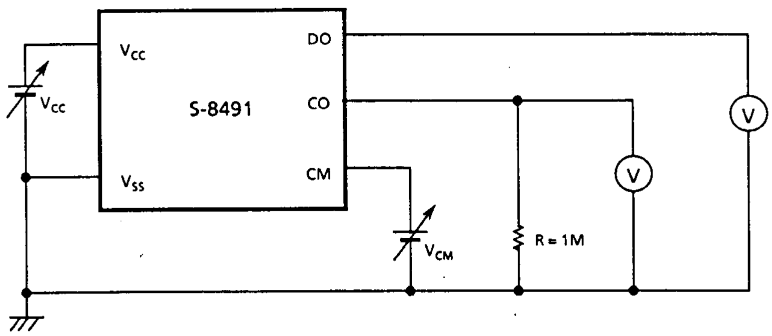
② In the excess charge region with $V_{CC} = V_{CU} + 0.1$ V, $V_{CM} = 0$ V, excess charge release voltage V_{CD} is the voltage of V_{CC} when CO goes high after gradually increasing V_{CC}.

③ In the normal region with $V_{CC} = V_{CD}$, $V_{CM} = 0$ V, excess discharge detection voltage V_{DD} is the voltage of V_{CC} when DO goes low after gradually decreasing V_{CC}.

④ In the excess discharge region with $V_{CC} = 2.0$ V, $V_{CM} = 0$ V, excess discharge release voltage V_{DU} is the voltage of V_{CC} when DO goes high after gradually increasing V_{CC}.

Note: Rise and fall speeds of V_{CC} are each specified at 150 V/sec or less.

(2) Measurement 2



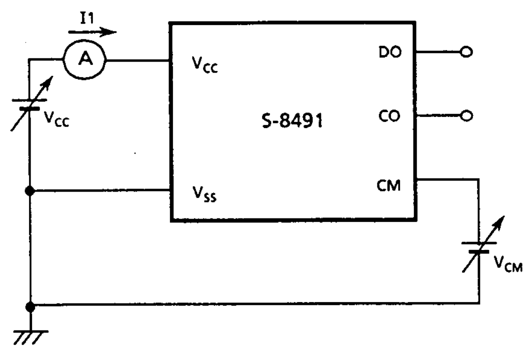
To measure excess charge detection time T_{CU}, **excess discharge detection time T_{DD}**, and excess current detection time T_{OFF}, follow these steps:

① In the normal region with $V_{CC} = V_{CU}$-0.1 V, $V_{CM} = 0$ V, **excess charge detection time T_{CU}** is the time from when V_{CC} is $V_{CU} + 0.1$ V to when CO goes low.

② In the normal region with $V_{CC} = V_{DD} + 0.1$ V, $V_{CM} = 0$ V, **excess discharge detection time T_{DD}** is the time from when $V_{CC} = V_{DD}$-0.1 V to when DO goes low.

③ In the normal region with $V_{CC} = 3.5$ V, $V_{CM} = 0$ V, **excess current detection time T_{OFF}** is the time from when V_{CM} is 3.5 V to when DO goes low.

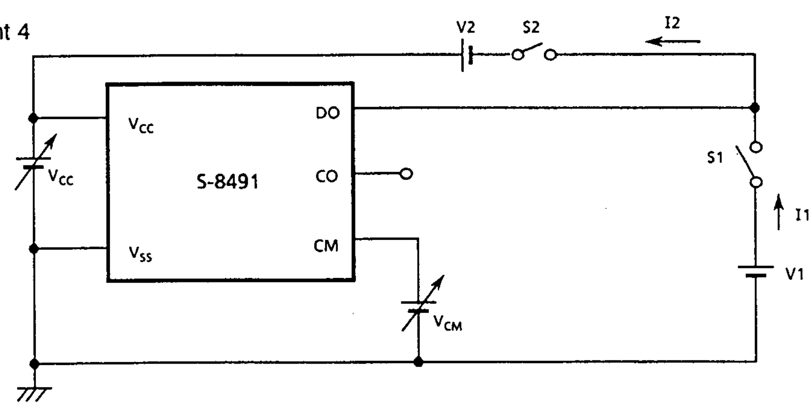
(3) Measurement 3



① In the normal region with $V_{CC} = 3.5$ V, $V_{CM} = 0$ V, **normal operating current consumption I_{OPE}** is I1.

② In the excess discharge region with $V_{CC} = 2.0$ V, $V_{CM} = 2.0$ V, **current consumption I_{PDN} in power-down mode** is I1.

(4) Measurement 4

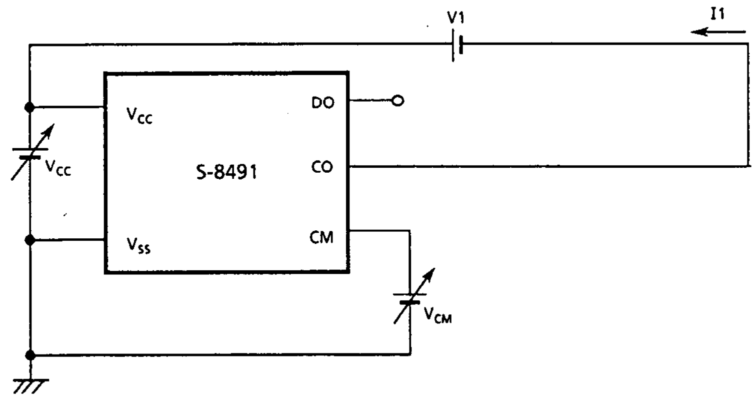


To measures DO 'H' voltage V_{DO}(H), DO 'L' voltage V_{DO}(L), follow these steps:

① In the normal region with $V_{CC} = 3.5$ V, $V_{CM} = 0$V, S1 = open, S2 = close, V2 = 0 V, DO 'H' voltage V_{DO}(H) is the voltage of V2 when I2 is 10 μA after gradually increasing V2.

② In the excess current region with $V_{CC} = 3.5$ V, $V_{CM} = 3.5$ V, S1 = close, S2 = open, V1 = 0 V, DO 'L' voltage V_{DO}(L) is the voltag of V1 when I1 = 10 μA after gradually increasing V1.

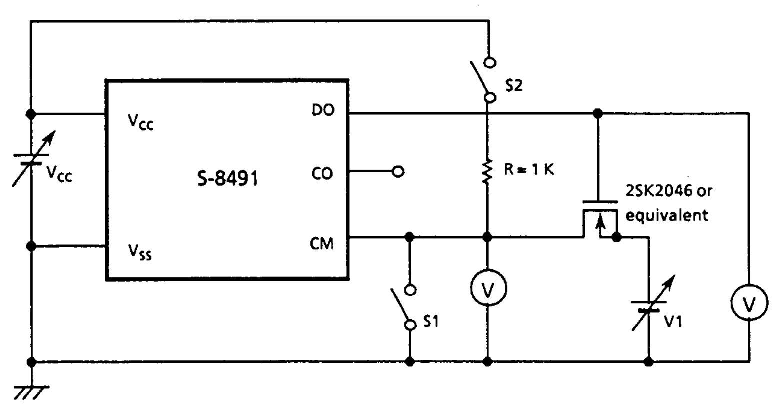
(5) Measurement 5



To measure CO 'H' voltage $V_{CO}(H)$, follow the step:

① In the normal region with V_{CC} = 3.5 V, V_{CM} = 0 V, V1 = 0 V, CO 'H' voltage $V_{CO}(H)$ is the voltage of V1 when I1 = 10 μA after gradually increasing V1.

(6) Measurement 6



To measure excess current detection voltage V_{IOV}, follow the step:

① In the normal region with V_{CC} = 3.5 V, V1 = 0 V, S1 = close S2 = close, **excess current detection voltage V_{IOV}** is the voltage of the CM pin when DO goes low after opening S1 and after gradually increasing V1.

■ Operation

Normal

This IC monitors both the voltage and the current of a battery connected between V_{CC} and V_{SS}, and controls charge and discharge. When the voltage of the battery is over V_{DD}, and below V_{CU}, and the voltage of the CM pin is bewlow V_{IOV}, this IC turns ON the charge and discharge FETs. This is called the normal region.

Excess Charge

In the normal region, when the voltage of the battery being charged exceeds V_{CU}, this IC stops charge by turning OFF the charge FET. This is called the excess charge region. When the battery voltage goes below V_{CD}, the state returns to the normal.

Excess Discharge

In the normal region, when the voltage of the battery being discharged goes below V_{DD}, this IC stops discharge by turning OFF the discharge FET. Current consumption of the IC turns to I_{PDN} at this time. This is called the excess discharge region.
When a charger is connected in the excess discharge region and the battery voltage exceeds V_{DU}, the state returns to the normal.

Excess Current

In the normal region, when the voltage of the CM pin exceeds V_{IOV} during discharge, this IC stops discharge by turning OFF the discharge FET. This is called excess current.

The state is returned to the normal by being more than 500MΩ resistance between EB+ and EB-, for example, by removing load.

Delay Circuit

This IC is provided with a comparator for monitoring excess charge detection, excess discharge detection or excess current. Also, it has delay time from when the comparator detects the voltage to when the output voltage is inverted at DO and CO pins.
Delay occurs only during the following operations.

(1) The "comparator" detects the excess charge detection voltage → Delay time → CO pin changes to the Hi-Z level.

(2) The "comparator" detects the excess discharge detection voltage → Delay time → DO pin changes to the V_{SS} level.

(3) The "comparator" detects the excess current detection voltage → Delay time → DO pin changes to the V_{SS} level.

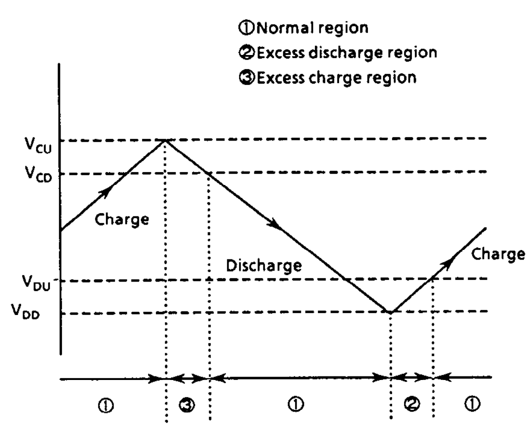


Figure 3

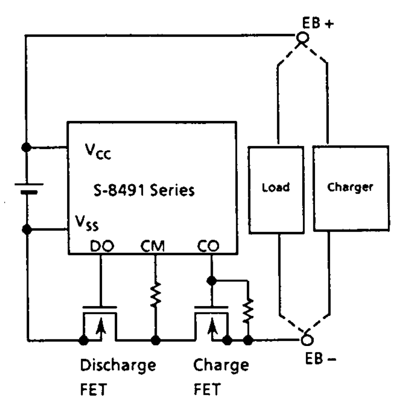
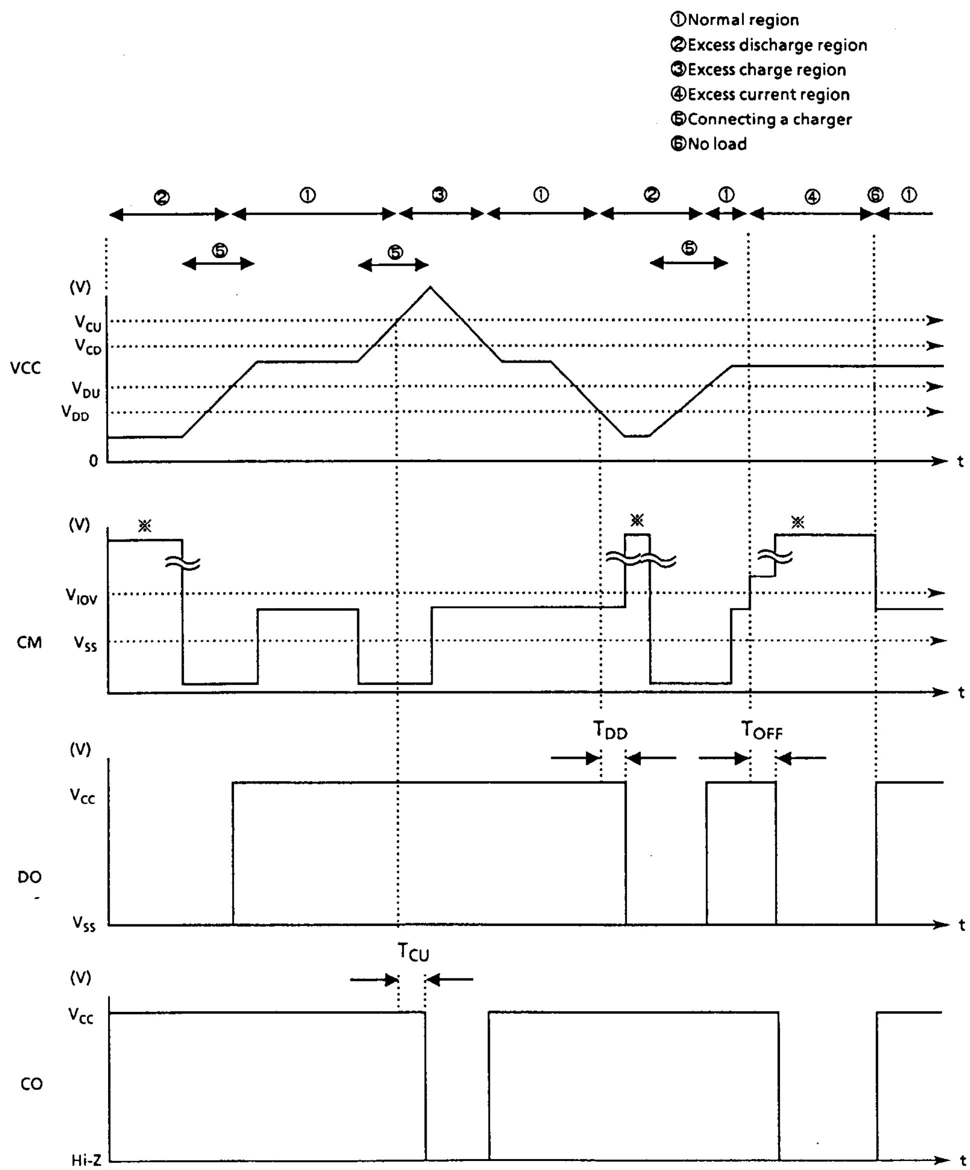


Figure 4

Table 5

Region	DO pin	CO pin
Normal $\xrightarrow{\text{Charge}}$ Excess charge	H	H $\xrightarrow{\text{Delay}}$ Hi-z
Excess charge $\xrightarrow{\text{Discharge}}$ Normal	H	Hi-z → H
Normal $\xrightarrow{\text{Discharge}}$ Excess discharge	H $\xrightarrow{\text{Delay}}$ L	H
Excess discharge $\xrightarrow{\text{Charge}}$ Normal	L → H	H
Excess charge→Excess current occurs	H $\xrightarrow{\text{Delay}}$ L	Hi-z
Normal region→Excess current occurs	H $\xrightarrow{\text{Delay}}$ L	H → Hi-z
Excess discharge→ Load short	L	H

■ Operating Timing Charts



※ Rises up to V_{CC} potential.

Figure 5

Battery Protection IC Connection Diagram

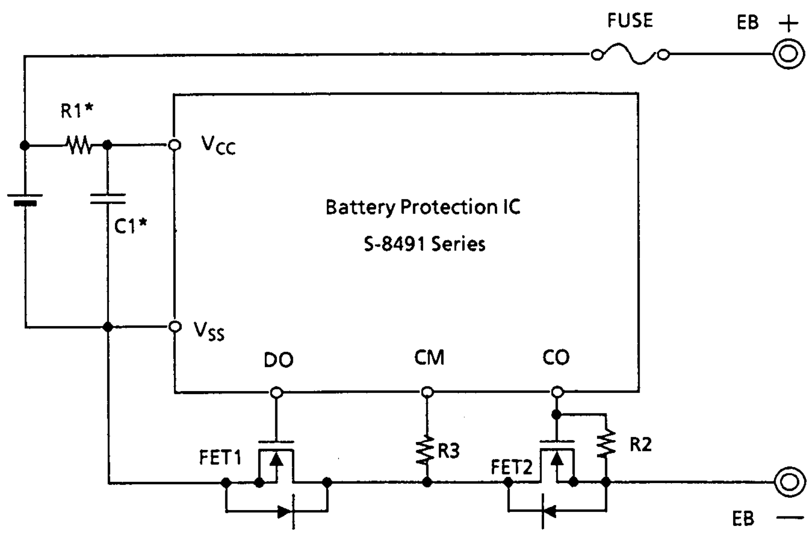


Figure 6

- Install an R1* less than 1 KΩ.
- The R2 is a pull-down resistor which turns OFF FET2. The R2 also protects the IC when the charger is connected reversely. Use a resistor from 100 KΩ or more to 1 MΩ or less.
- The R3 protects the IC when the charger is connected reversely. Use a resistor from 1 KΩ or more to 10 KΩ or less.
- Install a C1* more than 0.47μF.

* if they are needed for ESD (Electric Static Discharge) protection.

* The connection diagram explain typical applications of the products, and do not guarantee any massproduction design.

Handling Precautions

- In the excess discharge region, the voltage of the CM pin rises to the power supply voltage V_{CC}. This forces the built-in comparator to stop. Unless the CM pin is down to the V_{CC} level or less by connecting a charger, the excess discharge state can be retained.
- When initially connecting the battery to the IC, the state may go to the excess discharge state depending upon the characteristics of the capacitor or resistor attached to the CM pin. To return to the normal region, set the CM pin to the V_{SS} level or less (connect a charger).
- Oscillation may occur depending upon the value of the capacitor or resistor attached to the CM or DO pin. Select one from the following parts:
  FET1 gate capacity: A capacitor of 5000 pF or less
  Wiring resistance on the PCB between DO pin and FET1 gate: A resistor of 5 Ω or less
  (Refer to Figure 4, Battery Protection IC Diagram)
- When the excess current generates, the battery voltage drops due to its internal impedance to stop dischrage. If the voltage goes below the operating voltage of the IC (2.0 V), the excess discharge state may be retained even when the load is released. To return to the normal region, set the CM pin to the V_{SS} or less (connect a charger).

■ Dimensions

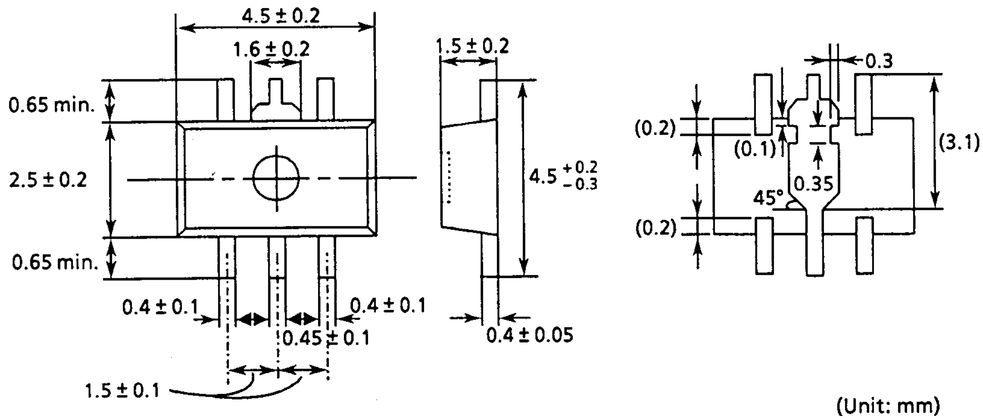
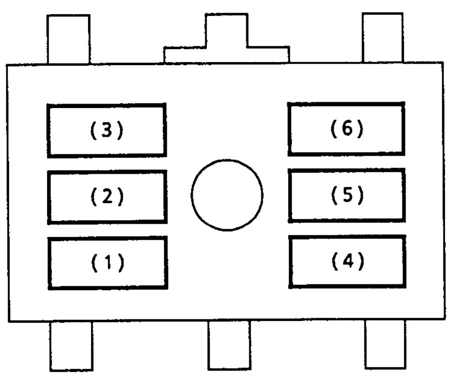


Figure 7

■ Markings



(1) to (3): Product name (abbreviation)
(4) : Year of assembly (last digit)
(5) : Month of assembly
(1 to 9, X, Y, and Z)
(6) : Week of assembly (1 to 3)

Figure 8

■ Taping

1. Tape Specifications

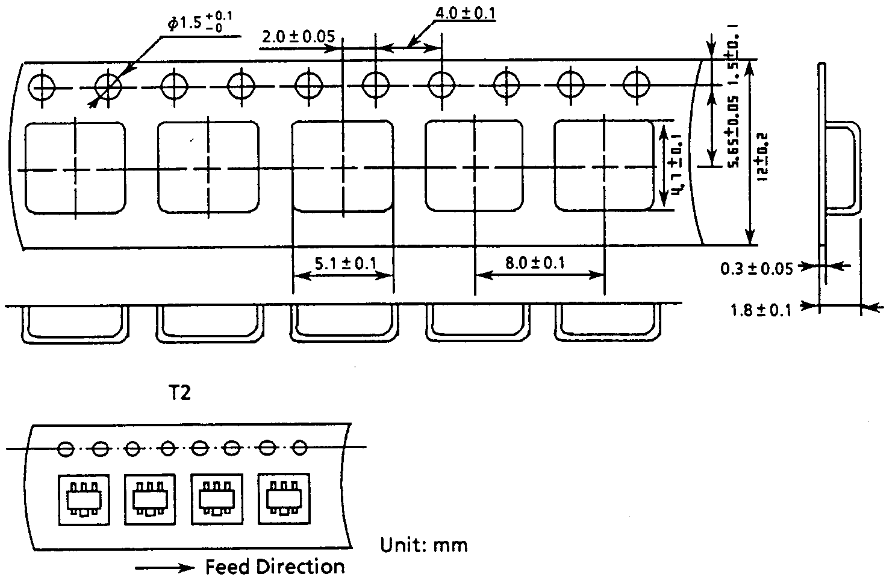


Figure 9

2. Reel Specifications

A reel holds 1000 ICs.

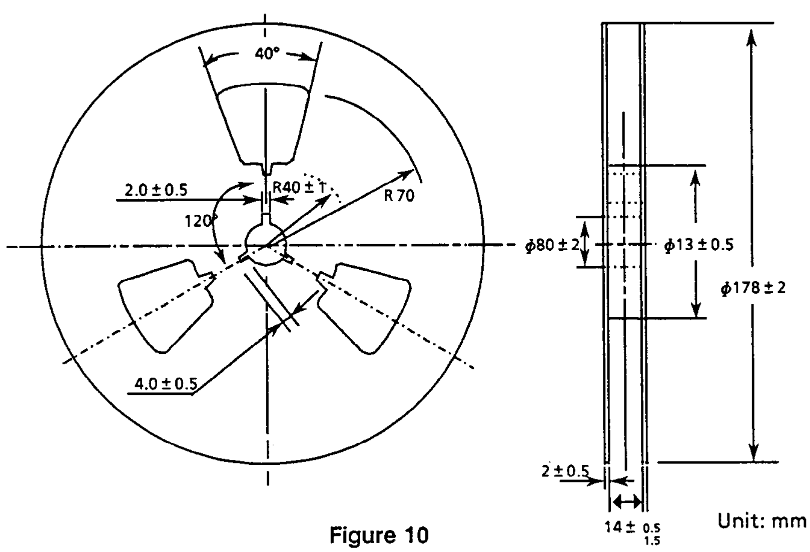
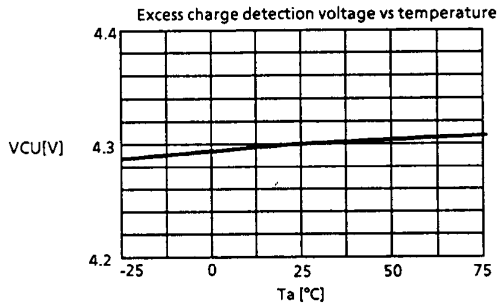
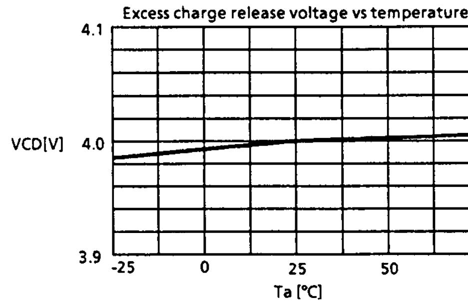


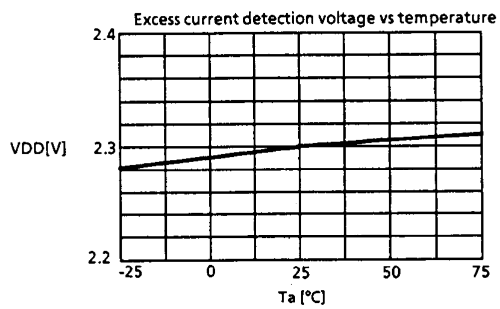
Figure 10

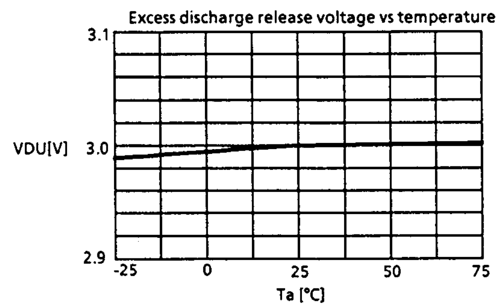
■ Characteristics

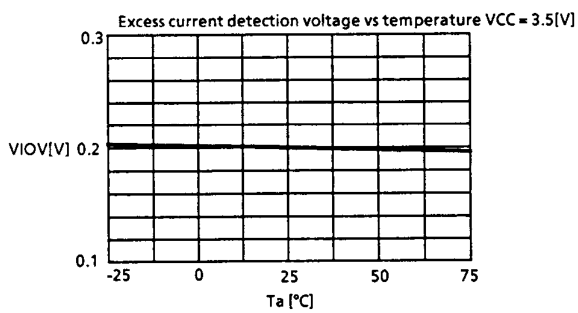
1. Temperature Characteristics of the Voltage Detector (Example: S8491AUP-DKA-T2)



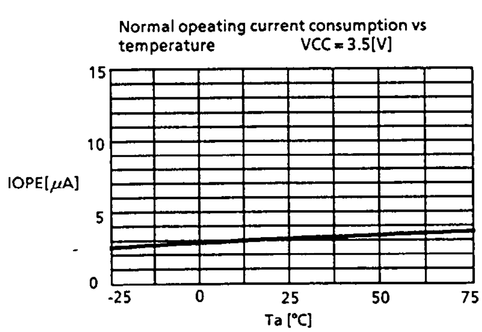


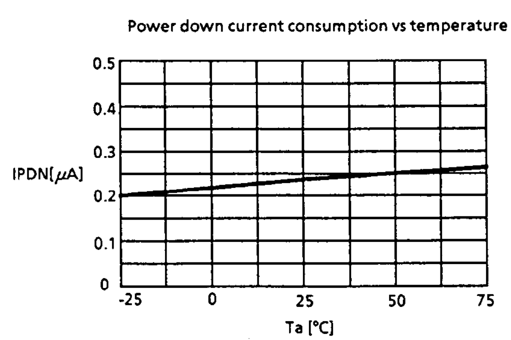






2. Temperature characteristics of current consumption (Example: S8491AUP-DKA-T2)





3. Temperature Characteristics of Delay Time (Example: S8491AUP-DKA-T2)