L4979D
L4979MD

LOW DROP VOLTAGE REGULATOR

1 FEATURES

- OPERATING DC SUPPLY VOLTAGE RANGE 5.6V TO 31V
- LOW QUIESCENT CURRENT (6µA Typ. @ 25° C with Enable Low)
- HIGH PRECISION OUTPUT VOLTAGE (2%)
- LOW DROPOUT VOLTAGE LESS THAN 0.5V
- RESET CIRCUIT SENSING THE OUTPUT VOLTAGE DOWN TO 1V
- PROGRAMMABLE RESET PULSE DELAY WITH EXTERNAL CAPACITOR
- WATCHDOG
- PROGRAMMABLE WATCHDOG TIMER WITH EXTERNAL CAPACITOR
- THERMAL SHUTDOWN AND SHORT CIRCUIT PROTECTION
- AUTOMOTIVE TEMPERATURE RANGE (Tj = -40°C TO 150°C)
- ENABLE INPUT FOR ENABLING/DISABLING THE VOLTAGE REGULATOR OUTPUT

Figure 1. Packages

Table 1. Order Codes

Part Number	Package
L4979D	SO-8
L4979MD	SO-20
L4979D13TR	SO-8 Tape & Reel
L4979MD13TR	SO-20 Tape & Reel

Figure 2. Block Diagram

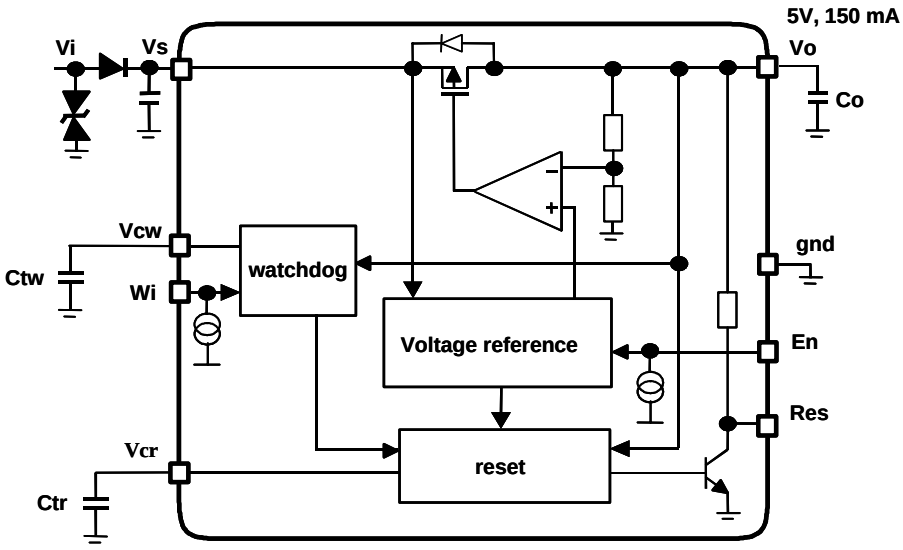


Table 2. Pin Function

SO8 N°	SO20 N°	Pin Name	Function
1	1	En	Enable input If high, regulator, watchdog and reset are operating. If low, regulator, watchdog and reset are shut down.
2	4	gnd	Ground reference
	5,6,15,16	gnd	Ground These pins are to be connected to a heat spreader electrically grounded
3	7	Res	Reset output. It is pulled down when output voltage drops below Vo_th or frequency at Wi is too low.
4	10	Vcr	Reset timing adjust A capacitor between Vcr pin and gnd sets the reset delay time (trd)
5	11	Vcw	Watchdog timer adjust A capacitor between Vcw pin and gnd sets the time response of the watchdog monitor.
6	14	Wi	Watchdog input. If the frequency at this input pin is too low, the Reset output is activated.
7	17	Vo	Voltage regulator output Output capacitor >100nF is needed for regulator stability
8	20	Vs	Supply voltage Supply capacitor (e.g. 200nF) is needed for regulator stability.
	2, 3, 8, 9, 12, 13, 18, 19	N. C.	not connected

Figure 3. Pins Connection (Top view)

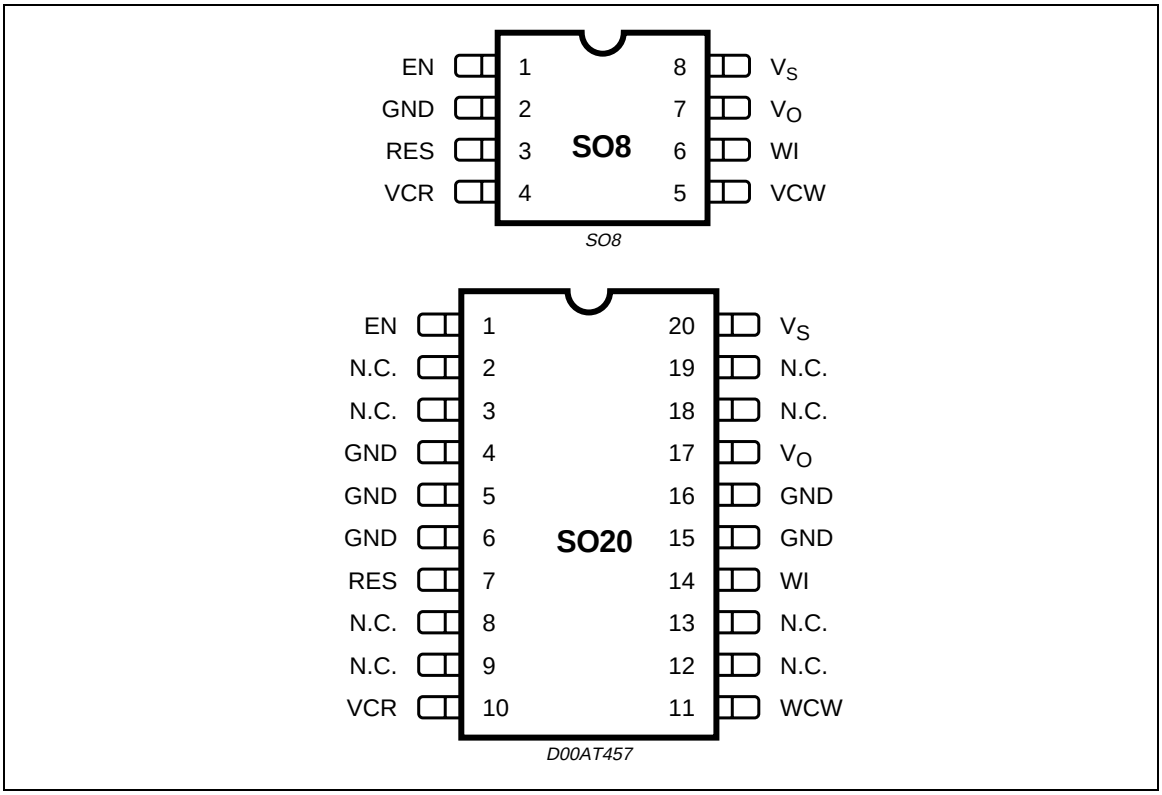


Table 3. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
Vvsdc	DC supply voltage	-0.3 to 40	V
Ivsdc	Input current	internally limited	
Vvo	DC output voltage	-0.3 to 6	V
Ivo	DC output current	internally limited	
Vwi	Watchdog input voltage	-0.3 to V_{vo} +0.3	V
Vod	Open drain output voltage (RES)	-0.3 to V_{vo} +0.3	V
Iod	Open drain output current (RES)	internally limited	
Vcr	Reset delay voltage	-0.3 to V_{vo} +0.3	V
Vcw	Watchdog delay voltage	-0.3 to V_{vo} +0.3	V
Ven	Enable input voltage	-0.3 to 40	V
Tj	Junction temperature	-40 to 150	°C
VESD	ESD voltage level (HBM-MIL STD 883C)	±2	kV

Note: 1. Maximum ratings are absolute ratings; exceeding any one of these values may cause permanent damage to the integrated circuit.

Table 4. Thermal DatA

Symbol	Parameter	SO8	SO16+2+2	Unit
$R_{th\ j\text{-}amb}$	Thermal resistance Junction to Ambient	130 to 180	50 to 80	°C/W

Table 5. Electrical Characteristcs

(V_S = 5.6V to 31V, T_j = -40° C to +150°C u nless otherwise specified)

Pin	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
GENERAL							
V_S, V_O	I_q	Quiescent current	V_S = 13.5V, I_o=150mA, enable high all I/O currents=0		1.5	3	mA
V_S, V_O	I_q	Quiescent current	V_S = 13.5V, I_o = 0mA, enable high all I/O currents = 0		100	200	µA
V_S, V_O	I_q	Quiescent current	V_S = 13.5V, I_o = 0mA, enable low all I/O currents = 0		6	20	µA
	T_w	Thermal protection temperature		150		190	°C
	T_{w_hy}	Thermal protection temperature hysteresis			10		°C

Table 5: Electrical Characteristics (continued)

Pin	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
VOLTAGE REGULATOR							
V_o	V_{o_ref}	Output voltage	V_s = 5.6 to 31V I_o = 1 to 150mA	4.90	5.00	5.10	V
V_o	I_{short}	Output short circuit current (1)	V_s = 13.5V	150	280	400	mA
V_o	I_{lim}	Output current limitation (1)	V_s = 13.5V	150	320	500	mA
V_s, V_o	V_{line}	Line regulation voltage	V_s = 5.6 to 31V I_o = 1 to 150mA			25	mV
V_o	V_{load}	Load regulation voltage	I_o = 1 to 150mA			25	mV
V_s, V_o	V_{dp}	Drop voltage	I_o = 150mA		200	400	mV
V_s, V_o	SVR	Ripple rejection (2)	f_r = 100 Hz	55			dB
RESET							
R_{es}	V_{res_l}	Reset output low voltage	R_{ext} = 5kΩ to Vo, Vo > 1V			0.4	V
R_{es}	I_{res_h}	Reset output high leakage current	V_{res} = 5V			1	µA
R_{es}	R_p_u	Internal Pull up resistance	with respect to V_o	12	25	50	kΩ
R_{es}	V_{o_th}	Reset threshold voltage	V_s = 5.6 to 31V I_o = 1 to 150mA	6% below V_{o_ref}	8% below V_{o_ref}	10% below V_{o_ref}	
V_{cr}	V_{rhth}	Reset timing high threshold	V_s = 13.5V	44% V_{o_ref}	47% V_{o_ref}	50% V_{o_ref}	
V_{cr}	V_{rlth}	Reset timing low threshold	V_s = 13.5V	10% V_{o_ref}	13% V_{o_ref}	16% V_{o_ref}	
V_{cr}	I_{cr}	Charge current	V_s = 13.5V	8	17	30	µA
V_{cr}	I_{dr}	Discharge current	V_s = 13.5V	8	17	30	µA
R_{es}	t_{rr_2}	Reset delay time (3)	Vo = V_{o_th} -100mV	100	250	700	µs
R_{es}	t_{rd}	Reset pulse delay	V_s = 13.5V, C_{tr} = 1nF	65		150	ms
WATCHDOG							
W_i	V_{ih}	Input high voltage	V_s = 13.5V	3.5			V
W_i	V_{il}	Input low voltage	V_s = 13.5V			1.5	V
W_i	V_{ih}	Input hysteresis	V_s = 13.5V		300		mV
W_i	I_i	Pull down current	V_s = 13.5V		10	20	µA
V_{cw}	V_{whth}	High threshold	V_s = 13.5V	2.20	2.35	2.50	V
V_{cw}	V_{wlth}	Low threshold	V_s = 13.5V	0.50	0.65	0.80	V

ELECTRICAL CHARACTERISTICS (continued)

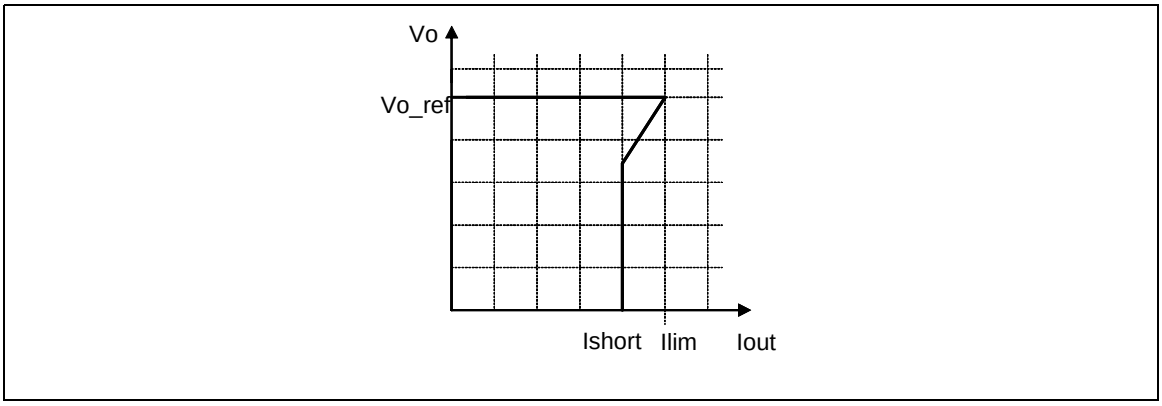
Pin	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{cw}	I_{cwc}	Charge current	V_s = 13.5V, V_{cw} = 0.1V	4	7.5	14	µA
V_{cw}	I_{cwd}	Discharge current	V_s = 13.5V, V_{cw} = 2.5V	1.0	2.4	4.5	µA
V_{cw}	T_{wop}	Watchdog period	V_s = 13.5V, C_{tw} = 47nF	25	50	90	ms
R_{es}	t_{wol}	Watchdog output low time	V_s = 13.5V, C_{tw} = 47nF	6	10	22	ms
ENABLE							
E_n	V_{en_l}	Enable input low voltage				1	V
E_n	V_{en_h}	Enable input high voltage		3			V
E_n	V_{en_hy}	Enable input hysteresis		700	1000	1100	mV
E_n	$I_{\_leak}$	Pull down current	E_n = 5V	2	10	20	µA

Note: 1. see fig4 (behavior of output current versus regulated voltage Vo)
2. guaranteed by design
3. When Vo becomes lower than 4V, the reset reaction time decreases down to 2µs assuring a faster reset condition in this particular case.

2 VOLTAGE REGULATOR

The voltage regulator uses a p-channel MOS transistor as a regulating element. With this structure a low drop-out voltage at current up to 150mA is achieved. The output voltage is regulated up to transient input supply voltage of 40V. No functional interruption due to over-voltage pulses is generated. The high precision of the output voltage is obtained with a pre-trimmed reference voltage. A short circuit protection to GND is provided.

Figure 4. Behavior of output current versus regulated voltage Vo (see a.m. Note 1)



3 RESET

The reset circuit monitors the output voltage Vo. If the output voltage drops below V_{o_th} then Res becomes low with a delay time trr. Real trr value changes as a non-linear function of delta ($V_{o\text{-}th}$ - V_o). The reset low signal is guaranteed for an output voltage Vo greater than 1V.

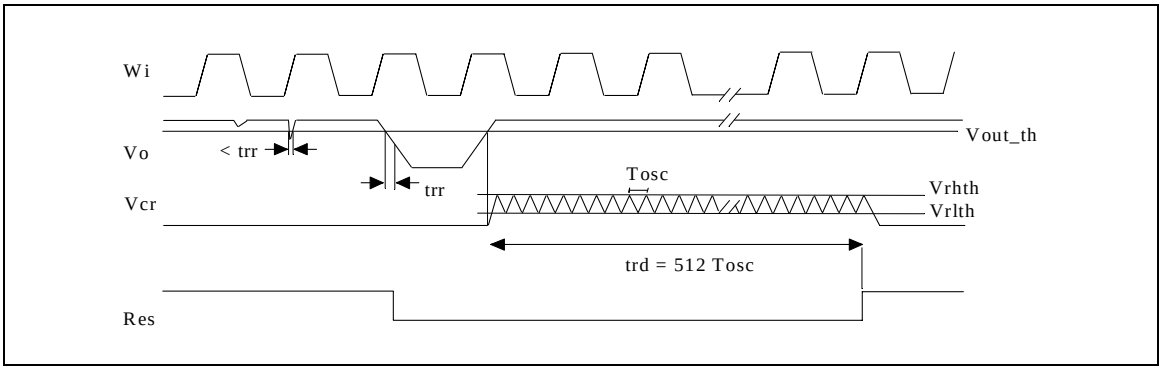
When the output voltage becomes higher than Vo_th then Res goes high with a delay trd. This delay is obtained by 512 periods of an oscillator (see fig. 5). The oscillator period is given by:

$$T_{osc} = \frac{[(V_{rhth} - V_{rlth}) \cdot C_{tr}]}{I_{cr}} + \frac{[(V_{rhth} - V_{rlth}) \cdot C_{tr}]}{I_{dr}}$$

and reset pulse delay trd is given by:

$$t_{rd} = 512 \times T_{osc}$$

Figure 5. Reset Time Diagram.



4 WATCHDOG

The watchdog input Wi monitors a connected microcontroller. If pulses are missing, the reset output Res is set to low. The pulse sequence time can be set within a wide range thorough the external capacitor C_{tw}. The watchdog circuit discharges the capacitor C_{tw} with the constant current Icwd. If the lower threshold Vwlth is reached, a watchdog reset is generated. To prevent this reset, the microcontroller must generate a positive edge during the discharge of the capacitor before the voltage has reached the threshold V_{wlth}. In order to calculate the minimum time Tdis during which the microcontroller must generate the positive edge, the following equation can be used:

$$(V_{whth} - V_{wlth}) \times C_{tw} = I_{cwd} \times T_{dis}$$

Each W_i positive edge switches the current source from discharging to charging; the same happens when the lower V_{wlth} threshold is reached. When the voltage reaches the upper threshold V_{whth} the current switches from charging to discharging. The result is a saw tooth voltage at the watchdog timer capacitor C_{tw}.

Figure 6. Watchdog time diagram

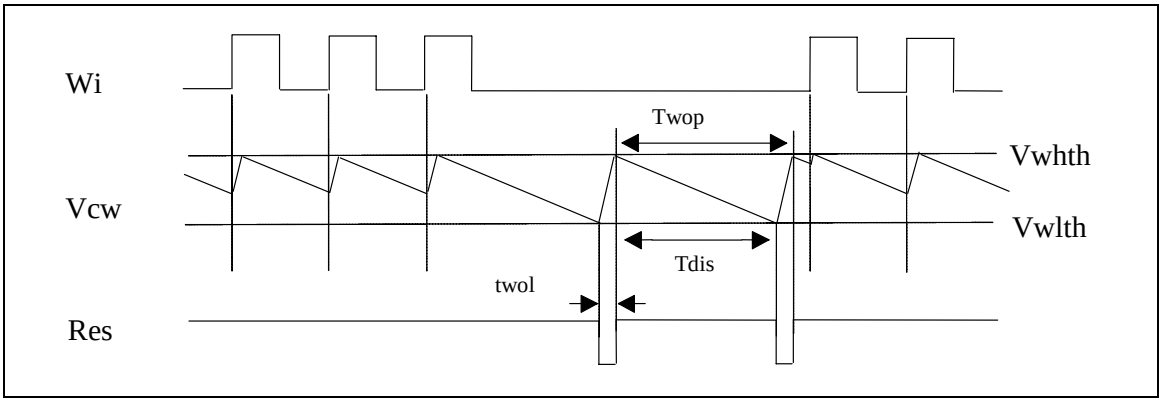
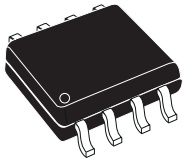


Figure 7. SO-8 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D (1)	4.80		5.00	0.189		0.197
E	3.80		4.00	0.15		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

Note: (1) Dimensions D does not include mold flash, protrusions or gate burrs.
Mold flash, potrusions or gate burrs shall not exceed 0.15mm (.006inch) in total (both side).

OUTLINE AND MECHANICAL DATA



SO-8

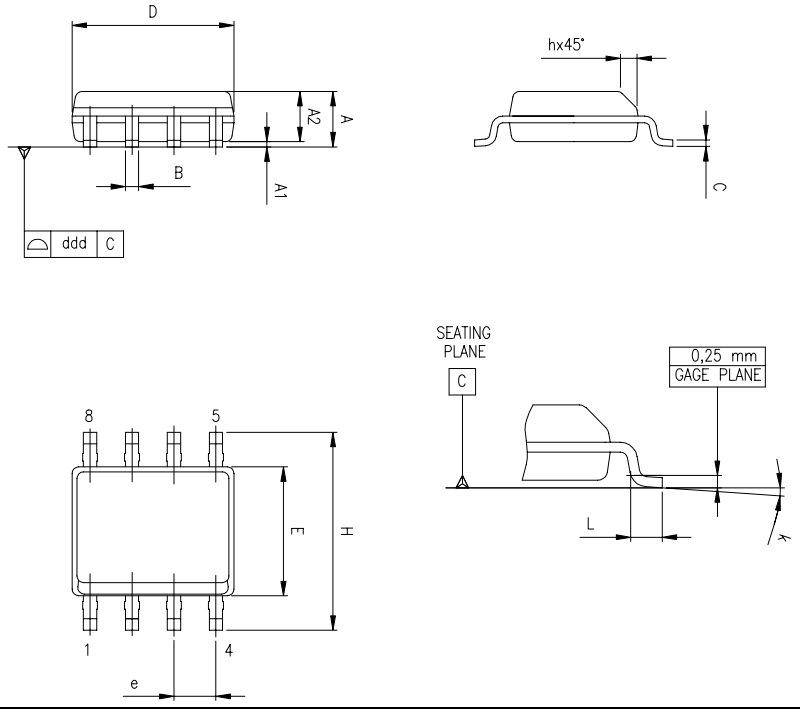
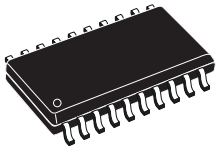


Figure 8. SO-20 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
B	0.33		0.51	0.013		0.200
C	0.23		0.32	0.009		0.013
D (1)	12.60		13.00	0.496		0.512
E	7.40		7.60	0.291		0.299
e		1.27			0.050	
H	10.0		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

(1) "D" dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

OUTLINE AND MECHANICAL DATA



SO20

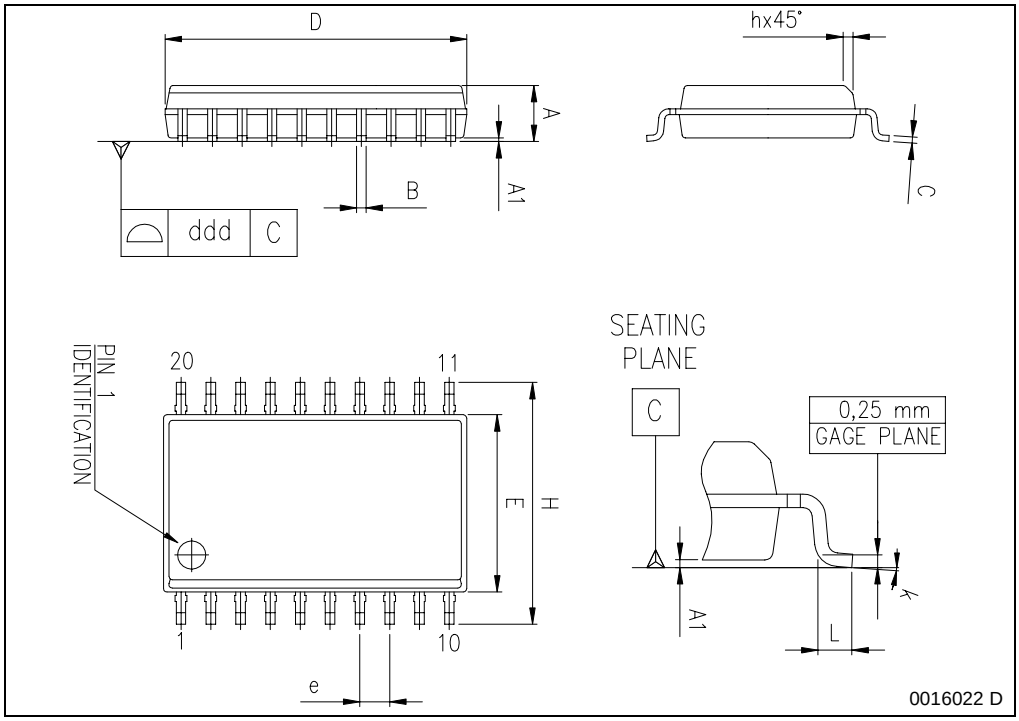


Table 6. Revision History

Date	Revision	Description of Changes
June 2004	3	Changed the values of the parameter “Reset timing high/low threshold.
July 2004	4	Pin Connection SO-20 changed. Changed some textes in the Features and table 2. Changed some values in the tables 3, 4 and 5. Changed some textes in the sections 2, 3 and 4.
October 2004	5	Changed from Product Preview to final datasheet.