· Building in external reset



STRUCTURE : Silicon Monolithic Integrated Circuit

PRODUCT NAME : DC/DC converter IC for camera module for car navigation system

MODEL NAME : BD8674KN

PACKAGE OUTLINE : Fig. - 1 BLOCK DIAGRAM : Fig. - 2

◎ FEATURES : +3.3V output Step down DC/DC converter for synchronous rectification system

· Double booster charger pump

+5V output LDOSoft start function

• Building in low voltage and over voltage protection function

Building in terminal RT OPEN/Short protectionThe frequency can be set by external resistance

Concentrated protection control with built-in sequencer

output function

VQFN-28 package

Parameter	Symbol	Limits	Unit
VIN supply voltage	VIN	18V	V
PVIN supply voltage	PVIN	VIN	V
Power dissipation	Pd	0.725*	W
Operating temperature	Topr	-40 ~ +85	°C
Storage temperature	Tstg	-55 ~ +150	°C

^{* 70}mm×70mm, thickness1.6mm, less than 3% share of copper foil when implementing glass epoxy board. Operating at higher than Ta=25°C, 5.8mW shall be reduced per 1

© OPERATION CONDITION (Please set the power-supply voltage in consideration of a power dissipation.)

Parameter	Symbol	MIN	TYP	MAX	Unit
VIN supply voltage	VIN	4.5	6.0	9.0	V

This product is not designed for protection against radioactive rays.



©ELECTRICAL CHARACTERISTICS

(Unless otherwise noted Ta=25°C, VIN=6.0V,PVIN=6.0V,V33IN=3.3V,V66IN=6.6V,GND=0V)

Parameter	Parameter Symbol specification v		UNII		Condition	
	Оуппоот	MIN	TYP	MAX	J	
VIN,PVIN Circuit current 1	I _{Q1}	-	-	50	μA	EN1,2=0V
VIN,PVIN Circuit current 2	l _{Q2}	-	15	-	mA	EN1,2=VIN
<step-down 3.3v="" converter="" dc="" of="" output="" part=""></step-down>						
3.3V output voltage	V ₀₃₃	3.234	3.300	3.366	V	
Terminal V33 Input bias current	I _{∨33B}	-	14	-	μΑ	V _{V33} =3.3V
Terminal V33 Discharge resistance	R _{V33DIS}	-	325	-	Ω	
Terminal FC33 Clamping voltage H	V _{FC33H}	1.2	-	-	V	V _{V33} =2.9V
Terminal FC33 Clamping voltage L	V _{FC33L}	-	-	0.2	V	V _{V33} =3.7V
Terminal FC33 Sink current	I _{FC33SINK}	0.5	-	-	mA	V _{V33} =3.7V, V _{FC33} =0.4V
Terminal FC33 Source current	I _{FC33SOURCE}	-	-	-14	μA	V _{V33} =2.9V, V _{FC33} =1.4V
Range of oscillation frequency setting	F _{osc}	500	-	1200	kHz	
Terminal SS Charging current	I _{SS33}	-4.0	-2.5	-1.0	μA	V _{SS33} =1.0V
Terminal SS Threshold voltage	V _{SS33TH}	1.0	1.1	1.2	V	V _{SS33} voltage、V _{V33} =0.8V
Terminal SS Clamping voltage	V _{SS33CLM}	1.6	1.9	2.2	V	
Terminal SS Standby voltage	V _{SS33STB}	0.11	0.15	0.19	V	V _{ss33} voltage (L→H)
Terminal SS Standby voltage Maximum hysteresis error	V _{SS33STB HYS}	5	50	100	mV	3.00
Terminal SS Discharge resistance	R _{SS33DIS}	49	70	91	kΩ	
Terminal SS Protection circuit start voltage	V _{SS33PON}	1.0	1.1	1.2	V	V _{SS33} voltage (L→H)
Terminal SS Protection circuit start voltage						3 ()
Maximum hysteresis error	V _{SS33PON_HYS}	10	100	200	mV	V _{SS33} voltage
Terminal V33 Low voltage detection voltage	V _{V33LVP}	1.11	1.32	1.53	V	V _{∨33} voltage (H→L)
Terminal V33 Low voltage detection	V _{V33LVP_HYS}	41.2	412	824	mV	V _{v33} voltage
Maximum hysteresis error						
Terminal V33 Overvoltage detection voltage	V _{V33OVP}	4.45	4.95	5.45	V	V _{v33} voltage
< Charge pump and 5V output LDO part >	T				1	
Terminal V33IN inflow current	V _{V33IN}	-	4	-	mA	V _{V33IN} =3.3V
Frequency of charge pump SW	F _{CP OSC}	-	640	-	kHz	
Terminal V5 Output voltage	V _{V5}	4.900	5.000	5.100	V	
Line regulation	V _{V5Line}	-	-	50	mV	6V~7V
Load regulation	V_{V5Load}	-	-	50	mV	1mA~20mA
Terminal V66 Standby voltage	V _{V66STB}	4.5	5.0	5.5	V	V_{V66} voltage(L \rightarrow H)
Terminal V66 Overvoltage detection voltage	V _{V66OVP}	8.91	9.9	10.89	V	V _{v66} voltage
Terminal V5 Protection circuit start voltage	V_{V5PON}	3.6	4.0	4.4	V	V _{v5} voltage
Terminal V5 Low voltage detection voltage	V_{V5LVP}	1.68	2.0	2.32	V	V _{√5} voltage (H→L)
Terminal V5 Low voltage detection	V _{V5LVP_HYS}	62.5	313	1250	mV	V _{v5} voltage
Maximum hysteresis error		02.5	313	1230	1110	V _{V5} Voltage
Terminal V5 Overvoltage detection voltage	V_{V5OVP}	6.75	7.5	8.25	V	V _{v5} voltage
< Reset part >						
Terminal V33 Reset detection voltage	V_{RSTO}	2.723	2.750	2.776	V	V _{∨33} voltage (H→L)
Terminal RSTDLY Sresshold voltage	V _{RSTDLYTH}	0.8	0.9	1.0	V	V _{V33} =3.3V
Terminal RESET Low output voltage	V _{OL_RST}	-	-	0.5	V	I _{OL} =4mA
< Other >						
Terminal EN Input voltage high level voltage	V _{IH_EN}	2.0	-	VIN	V	Terminal EN1,2
Terminal EN Input voltage Low level voltage	V _{IL_EN}	-	-	0.5	V	Terminal EN1,2
Terminal EN Input current	I _{I_EN}	-	36	54	μA	Terminal EN1,2, EN=VIN
N. V.						

 $\bullet V_{V33}$: V33 voltage, V_{FC33} : FC33 voltage, V_{SS33} : SS voltage, V_{V66IN} : V66IN voltage,

 $V_{V5}: \quad V5 \, voltage, \quad V_{V33IN} \quad : \quad V33IN \, voltage$

[•]This product is not designed for protection against radioactive rays.

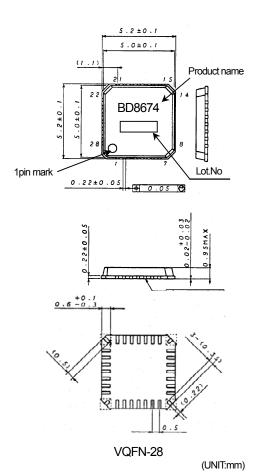
[•]The current ability must not exceed Pd.



©PIN ASSIGNMENT

No.	Symbol	Description	No.	Symbol	Description
1	FB5	5V output voltage detection terminal	15	GND	GND(0V connection)
2	V5	5V regulator output terminal	16	SS33	3.3V soft start adjustment capacity connection terminal
3	V66IN	LDO6.6V voltage input terminal	17	RT	Frequency adjustment resistance connection terminal
4	V66	Charge pump voltage output terminal	18	RSTDLY	Reset Delay adjustment capacity connection terminal
5	CP	Capacity connection terminal for charge pump (+)	19	RSTO	Reset output terminal
6	CM	Capacity connection terminal for charge pump (—)	20	VIN	Power supply input terminal
7	V33IN	Charge pump 3.3V input voltage terminal	21	TEST4	Test terminal 4
8	PGND	Power GND (the same potential as terminal GND)	22	TEST3	Test terminal 3
9	SW	Coil connection terminal	23	TEST2	Test terminal 2
10	PVIN	Power supply input terminal for PowerTr (=VIN)	24	GND	GND(0V connection)
11	TEST5	Test terminal 5	25	EN2	5V output control terminal
12	V33	3.3V output voltage detection terminal	26	EN1	3.3V output control terminal
13	FB33	Error amplifier input terminal	27	SS5	5V soft start adjustment capacity connection terminal
14	FC33	Error amplifier output terminal	28	TEST1	Test terminal 1

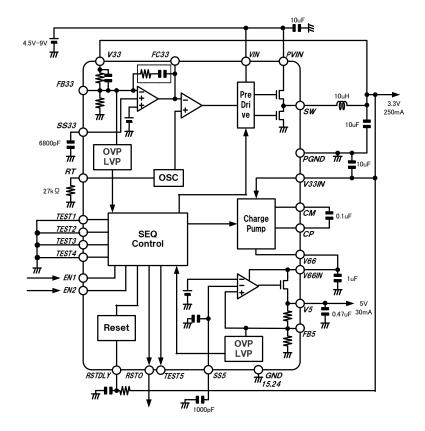
©PACKAGE OUTLINE



PACKAGE OUTLINE -fig.1



©BLOCK DIAGRAM



BLOCK DIAGRAM and recommended external parts constant -fig.2

- * TEST1,2,3,4 terminal should be connected.
- * PVIN and VIN terminal should be connected each other.
- * Phase compensation circuit of switching regulator is in clunded on this IC. But if switching regulator is used with unrecommeded external parts or under unrecommeded condition, external phase compensation is needed.



◎NOTE ON USE

1. About the absolute maximum rating

Attention is brushed off enough to the quality control, it is likely to destroy when the absolute maximum rating such as impressed voltages (VCC_IN,DCIN) and ranges (Topr) of the operating temperature as it is exceeded, the mode of breakings of the short or the opening, etc. cannot be specified, and examine it in this IC to give physical measures for safety such as fuses when a special mode that exceeds the absolute maximum rating is assumed.

2. About the reverse-connection of the power supply connector

IC might destroy it by reversely connecting the power supply connector. Give measures such as putting the diode between power supply terminals of power supply and IC outside for the reverse-touching destruction protection.

3. Power supply line

Please do measures such as putting the bypass capacitor in power supply-GND nearest pin of this IC as the route of the resurrection current to cause the return of the current in which it resurrected it by the counter electromotive force of the coil.

Please confirm the characteristic of the electrolytic capacitor enough as the capacity omission etc. at the low temperature never happen, and decide it.

4. About grand potentia

Any state of operation must become the lowest potential about the potential of the terminal GND. Moreover, confirm whether there is terminal that is actually the voltage of GND or less including transients.

About the heat design

Think about permissible loss (Pd) in an actual state of use, and do the heat design with the margin enough.

6. About the short and the miss-installation between terminals

Note the direction and the miss-registration of IC enough when you install it in the set substrate. IC might destroy it as well as reversely connecting the power supply connector when installing it by mistake. Moreover, there is fear of destruction when the foreign body enters between terminals, the terminal, the power supply, and grandeur and it is short-circuited.

7. About operation in strong electromagnetic field

In use in strong electromagnetic field, note that there is a possibility of malfunctioning.

8. About the capacitor during output-GND

The current charged the capacitor with when VCC is 0V or is GND and is short-circuited when a big capacitor is connected between GND output by some factors flows into the output and it is likely to destroy it. Give the capacitor between GND output to 0.1µF or less.

9. About the inspection by the set substrate

It is likely to suffer stress to IC and discharge electricity every one process when you connect the capacitor with the pin with low impedance when inspecting it in the set substrate. Moreover, detach it after connecting after the power supply is turned off without fail when detaching it to G in the inspection process, inspecting, and turning off the power supply. In addition, be give the earth to the assembly process as a static electricity measures, and careful enough when it transports and you preserve it.

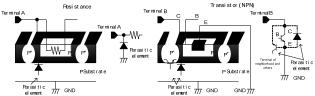
10. About each input terminal

This IC is a monolithic IC which has a P⁺isolations and P substrate to isolate elements each other.

This P layer and an N layer in each element form a PN junction to construct various parasitic elements.

For instance, the potential difference operates in resistance as shown in the figure below when resistance and the transistor connect it with the terminal and the playground (GND) >(terminal B) joint of PN operates as a parasitic diode in playground (GND) >(terminal A) transistor (NPN). In addition, the NPN transistor of parasitism works with N layer of the element of the above-mentioned parasitic diode and the neighborhood and others in transistor (NPN). A parasitic element in IC composition is inevitably formed because of the potential relation.

A parasitic element can operate, the interference with the circuit operation be caused, it malfunction, and, consequently, it cause destruction. Therefore, do not do the usage that a parasitic element operates as a voltage that is lower than the playground (GND;P substrate) is impressed to the input terminal enough. Moreover, do not impress the voltage to the input terminal when you do not impress the power-supply voltage to IC. Give each input terminal to me the voltage below the power-supply voltage or in the guarantee value of an electric characteristic when you similarly impress the power-supply voltage.



Example of IC of simple structure

11. Earth wiring pattern

If small signal GND and large current GND exist, disperse their pattern. In addition, for voltage change by pattern wiring impedance and large current not to change voltage of small signal GND, each ground terminal of IC must be connected at the one point on the set circuit board. As for GND of external parts, it is similar to the above-mentioned.

12 Thermal Shut-Down

When a thermal shutdown operates, the DC/DC converter controller of all Ch is turned off. When a thermal shutdown is released, the DC/DC converter controller of all Ch becomes an operation beginning from turning off.

13. Bypass Capacitor of Power Supply

When PVIN, VIN voltages go down as ENI=HIGH in the state of high impedance with a capacitor in the large effect of the dielectric substance absorption such as the aluminum electric field capacitor installed in PVIN and VIN; PVIN, VIN voltages go up by dielectric substance absorption again, and V33 output voltage goes up.

Notes

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