System Power Supply for TV Series

Built-in 1ch FET Synchronous Rectification Type DC/DC converters

BD8621EFV

●Description

BD8621EFV has realized the high performance and reliability required as a power supply for thin-screen TV.
With built-in FET 1ch current mode control, the DC/DC Converter series has the advantage of high-speed load response and wide phase margin.
Due to the high-speed load response, it is most suitable for TV-purpose processors with increasingly high performance, and due to the wide phase margin it leaves a good margin for board pattern & constant setting and so facilitates its application design.
As a high-reliability design, it has various built-in protection circuits (overcurrent protection, output voltage abnormal protection, thermal protection, and off-latch function at the time of abnormality etc.), therefore as an advantage it does not easily damage in every possible abnormal condition such as all-pin short circuit test etc. and hence most suitable for thin-screen TV which requires the high reliability.

●Features

1) 3A output current
2) Low RDS(ON) internal switches (PchMOS:75mΩ, NchMOS:55mΩ)
3) ±1% reference voltage accuracy
4) Programmable frequency : 250kHz-1MHz
5) (Frequency in programmable by adjusting RT resistance or synchronizing with SYNCLK terminal.)
6) Terminal RT OPEN/SHORT detecting function
7) Over current protection function
8) Output over voltage/low voltage protection function (over : FB > VREF +60mV , low : FB < VREF -60mV)
9) Timer off latch function in abnormal circumstances
10) Thermal shutdown function
11) Under voltage protection
12) Soft start/start delay circuit
13) Soft start time out function
14) Protecting BUS function with terminal PDET
15) HTSSOP-B20 package

Jul. 2008

●Electrical characteristics

(Unless otherwise noted Ta=25℃, VIN=3.3V, GND=0V)

Parameter	Symbol	Specification value			UNIT	Condition
		MIN	TYP	MAX		
VIN supply current (operating)	I_{Q_active}	-	220	350	μA	V_{FB} = 0.83V, V_{FC} = 1V
VIN supply current (standby)	I_{Q_stby}	-	0	1	μA	V_{EN} = 0V
Reference voltage (VREF)	V_{REF}	0.792	0.8	0.808	V	
Output rise detection voltage	V_{OVP}	30	60	90	mV	Monitoring FB terminal
Output decrease detection voltage	V_{LVP}	-90	-60	-30	mV	Monitoring FB terminal
Terminal PDET output current	I_{PDET}	0.4	-	-	mA	V_{PDET}< 0.3V
Oscillation frequency	f_{OSC}	500	550	600	kHz	R_{RT}= 220kΩ
Pch FET ON resistance	R_{PFET}	-	75	110	mΩ	I_{SW} = 1A
Nch FET ON resistance	R_{NFET}	-	55	90	mΩ	I_{SW} = 1A
UVLO voltage	V_{UVLO}	2.35	2.50	2.65	V	
SW leak current	I_{LSW}	-	0	1	μA	V_{EN}= 0V, V_{IN} = 5.5V
EN terminal H threshold voltage	V_{ENH}	1.1	-	-	V	
EN terminal L threshold voltage	V_{ENL}	-	-	0.4	V	
FC sink current	I_{FCSI}	10	20	-	μA	
FC source current	I_{FCSO}	-	-20	-10	μA	
SS/DELAY terminal source current	I_{SSSO}	2	4	6	μA	
Terminal PDET pull-up resistor	R_{PDET}	100	170	250	kΩ	

V_{FB} :FB terminal voltage, V_{EN} :EN terminal voltage, V_{FC} :FC terminal voltage, V_{PDET}: PDET terminal voltage

Current capability should not exceed Pd.

● Block Diagram

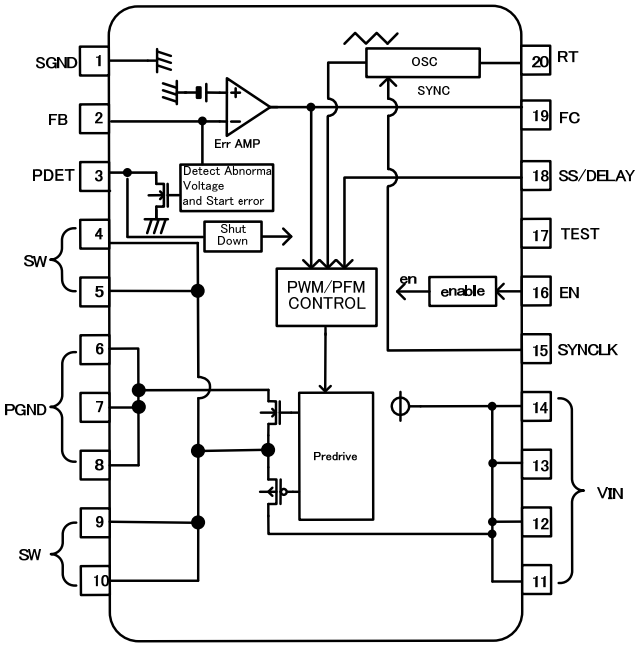
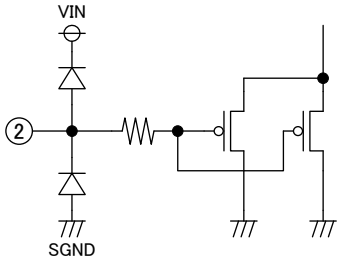
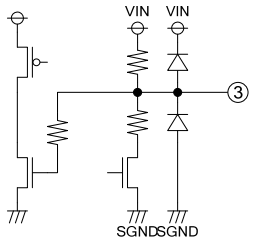
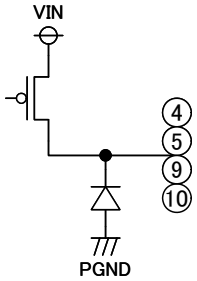


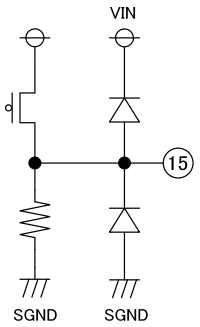
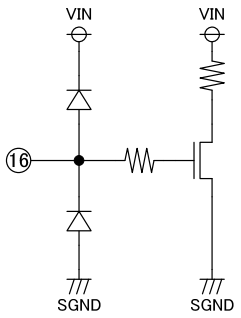
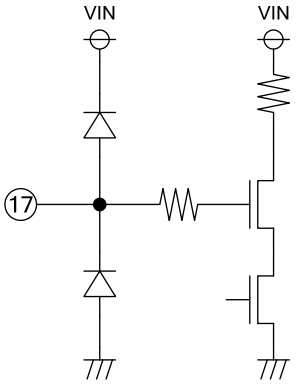
Fig1 Block diagram

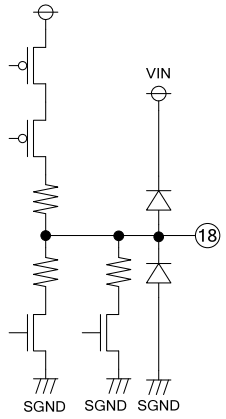
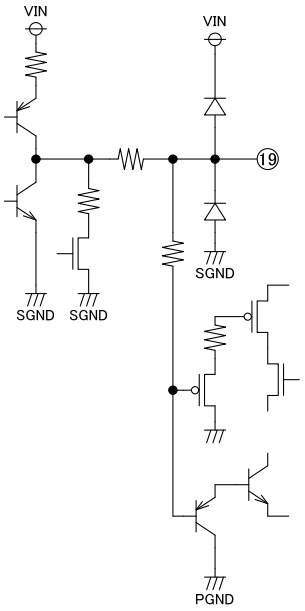
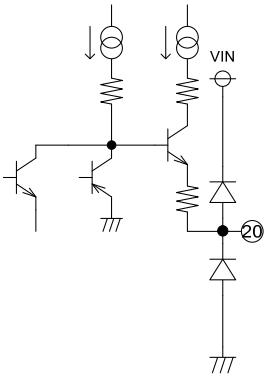
● Pin Description

No.	Symbol	Description	Explanation
1	SGND	Signal GND terminal	Small signal system GND
2	FB	Feed back terminal	Output voltage detection
3	PDET	Off latch signal output	Protecting BUS communication terminal
4	SW	Output terminal	Switching output
5	SW		
6	PGND	Power GND terminal	GND for power MOSFET
7	PGND		
8	PGND		
9	SW	Output terminal	Power Mos output
10	SW		
11	VIN	Power supply input terminal	Power supply input. The decoupling is done to PGND
12	VIN		
13	VIN		
14	VIN		
15	REG	Internal Regulator	Synchronizable switching output terminal frequency with external clock
16	EN	Enable input	ON/OFF control for device operation
17	TEST	Terminal for test	SGND short in the set.
18	SS/DELAY	Soft start adjustment capacity connection terminal	The soft start time is adjusted with the connected capacitor
19	FC	Error amplifier output	Error amplifier phase compensation point
20	RT	Frequency adjustment resistance connection terminal	The switching frequency is set by the connected resistance

● Pin equivalence circuit diagram

No.	Symbol	Explanation	Terminal equivalent circuit diagram
1	SGND	GND (connected 0V)	
2	FB	Output voltage detection terminal	
3	PDET	Protecting BUS I/O terminal	
4,5,9,10	SW	Output terminal	
6,7,8	PGND	Power GND (Same voltage as SGND)	
11,12,13,14	VIN	Power supply input terminal	

No.	Symbol	Explanation	Terminal equivalent circuit diagram
15	REG	Internal Regulator output voltage	
16	EN	Enable terminal	
17	TEST	Using at test mode	

No.	Symbol	Explanation	Terminal equivalent circuit diagram
18	SS /DELAY	Soft start time adjustment terminal	
19	FC	Error amplifier compensation terminal	
20	RT	Oscillator frequency adjustment terminal	

●Operation description

Enable control

The device can be controlled ON/OFF by EN terminal (16 pin) voltage.
An internal circuit starts when VEN reaches 1.1V.

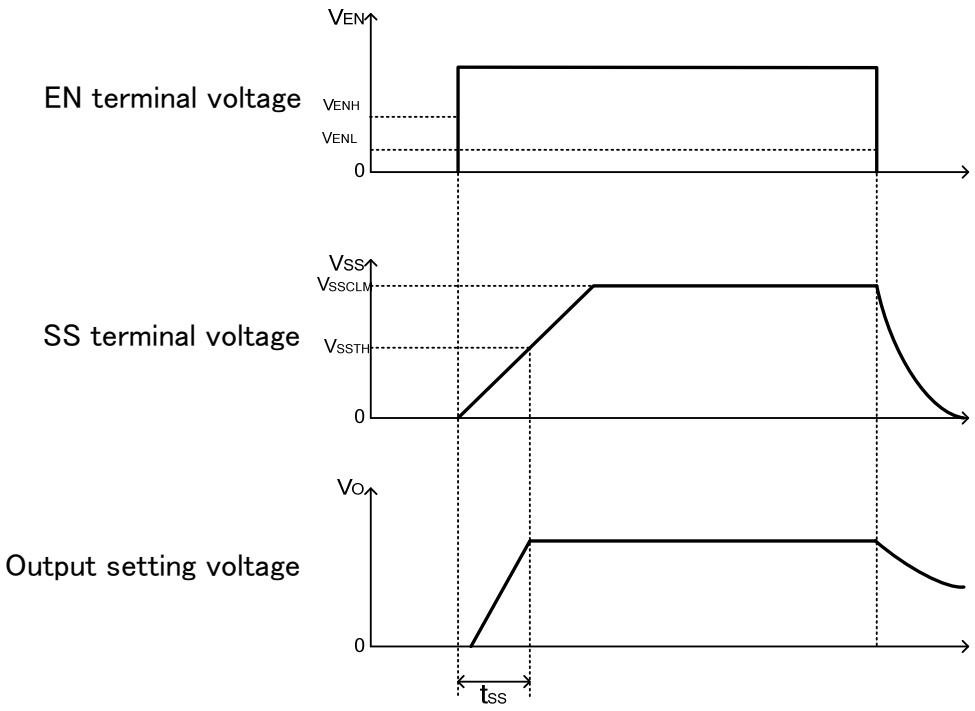


Fig.2 **ON/OFF transition wave form in EN controlling**

Soft start time set function

As for BD8623EFV, output can do soft start without overshoot by charging soft start capacity (CSS) connected between SS and SGND terminal.
Also, soft start time (tss) can be set by setting soft start capacity (CSS) arbitrarily.

OSC oscillation frequency setting function

The output oscillation frequency can be set by connecting resistance between terminal RT (20 pins) and SGND (range = 250kHz - 1MHz)
The relation between RT terminal resistance and the oscillation frequency follows Fig.3.

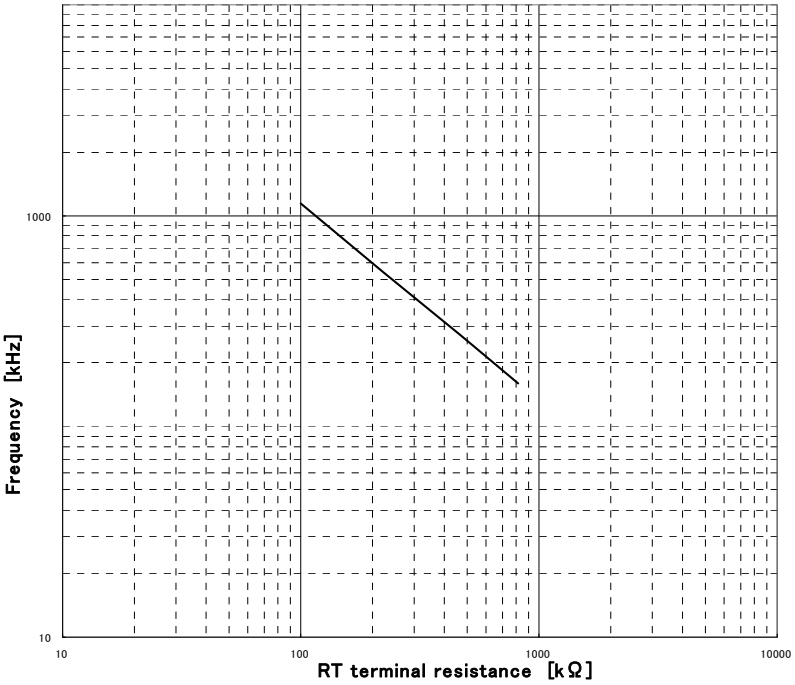


Fig.3 RT resistance-oscillation frequency

Switching frequency synchronization

An internal transmitter of BD8623EFV can be synchronized with the external clock signal connected with the terminal SYNCLK (15 pins).
The frequency of external clock can be set within the range of 250kHz-1MHz. In this case, please set the RT resistance that may become about -20% value of the external clock frequency.

※ Be short-circuited SYNCLK terminal to SGND when a frequency synchronous function is not used.

●Protection function

Protection circuit is effective for destruction prevention due to accident so that avoid using under continuous protection operation.

Low voltage protection function (LVP)

The voltage of the terminal FB (2 pins) is compared with internal reference voltage VREF.
If FB terminal voltage falls below V_{LVP}(= VREF -60mV) and the state continues for 500us, output changes to low voltage and the state is fixed. In that case , PDET (3pin) output changes to L.

Table 4-1 output low voltage protection function

EN terminal	SS terminal	FB terminal	Low voltage protection function	Low voltage protection operation
$>V_{ENH}$	>1.4V(typ)	$<V_{LVP}$	Effective	ON
		$>V_{LVP}$		OFF
	<1.4V(typ)	-	Invalidity	OFF
$<V_{ENL}$	-	-	Invalidity	OFF

＊ Low voltage protection function is available when SS terminal voltage becomes more than 1.4V (typ) in the transition to ON control (during soft start).

Over voltage protection function(OVP)

The voltage of the terminal FB is compared with internal reference voltage VREF.
If FB terminal voltage is over Vovp (=VREF +60mV) and the state is continues for 500usec, output changes to low voltage and the state is fixed.

Table 4-2 output overvoltage protection function

EN terminal	SS terminal	FB terminal	Over voltage protection function	Over voltage protection operation
$>V_{ENH}$	>1.4V(typ)	$>V_{OVP}$	Effective	ON
		$<V_{OVP}$		OFF
	<1.4V(typ)	-	Invalidity	OFF
$<V_{ENL}$	-	-	Invalidity	OFF

＊ Over voltage protection function is available when SS terminal voltage becomes more than 1.4V (typ) in the transition to ON control (during soft start).

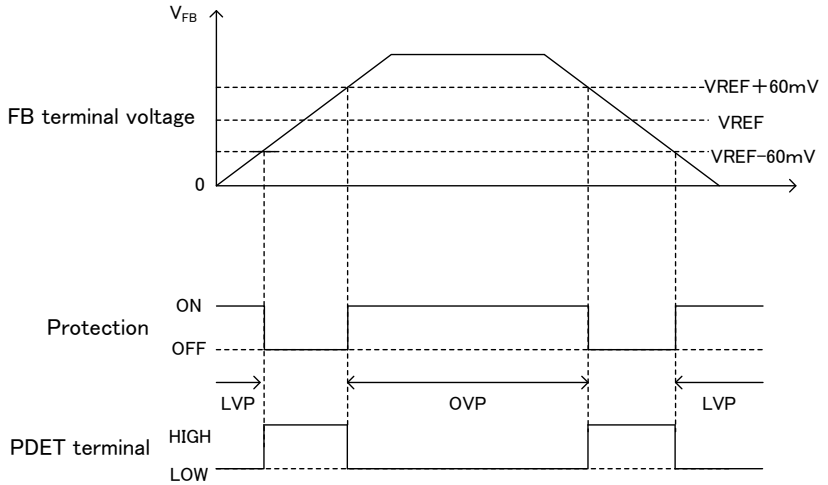


Fig.4 **Output voltage error detection range**

Under voltage lock out protection (UVLO)

As for BD8623EFV, the power-supply voltage decrease detection protection circuit is built in.
It the input voltage decrease below the UVLO voltage (2.5V typ), the device state changes to the standby mode (Moreover, to prevent the chattering of the output) hysteresis width of 100mV(typ) has been installed in the UVLO cancel voltage.

RT terminal open/short protection function (RTO/RTS)

RT terminal opening/short protection function prevent the clock from abnormal oscillation.
If RT terminal open/short protection function is detected, output voltage changes to low level and is fixed.

Terminal RT opening/short protection function is available if the state continue for 500usec, abnormal detection operates when the state continues about 500μsec(typ).

Soft start time-out function

If VSS doesn't exceed VSSTH within 64msec (typ) since a soft start began, BD8629FS controls an off latch.
Vo is fixed in a low level.

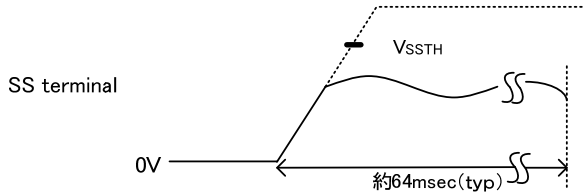


Fig.5 **Soft start time-out**

Thermal shut down function

Thermal shut down circuit (TSD circuit) is built into BD8623EFV. When the temperature of the chip exceeds Tjmax=175, the DC/DC converter is fixed in a low voltage.
TSD function is aimed to shut down IC from thermal reckless driving under an abnormal state to exceed Tjmax=175. It aims at neither protection nor the guarantee of the set. Therefore, please do not use this function to protect the set.

Over current protection function

The over current protection function has been achieved by limiting the current that flows on high side MOSFET.
The current is controlled in every one cycle of the switching frequency. When an abnormal state continues for about 500μsec(typ), the output is fixed in a low level.

Protecting BUS function with terminal PDET

The terminal PDET (3 pins) monitors whether IC is normal or not. When IC becomes abnormal, the PDET output is reduced at "L" level with the output voltage fixed “L” level at the same time. Moreover, it is possible to make the output fix in a low level by compulsorily reducing the terminal PDET at "L" level from the outside.

When two or more BD8623EFV is used in the application, this function prevents the IC from destroying, because one IC error transmits all other ICs by PDET line in the condition that PDET terminals are connected each other.

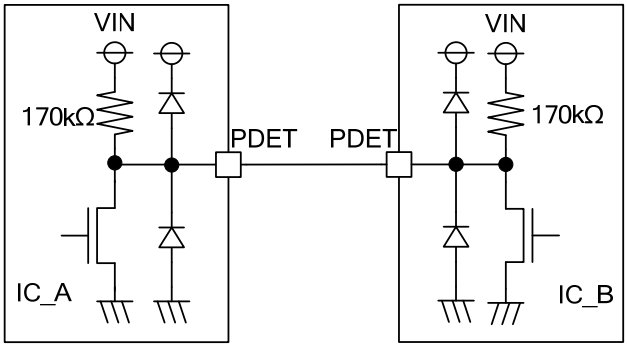


Fig.6 Protecting BUS communication

※Please give the terminal PDET as OPEN when you do not use protecting BUS function.

Error detection (off latch) release method

BD8623EFV enters the state of an off latch when the protection function operates.

To release the off latch state, EN terminal voltage should be changed to low level once time.

●Each characteristic reference data

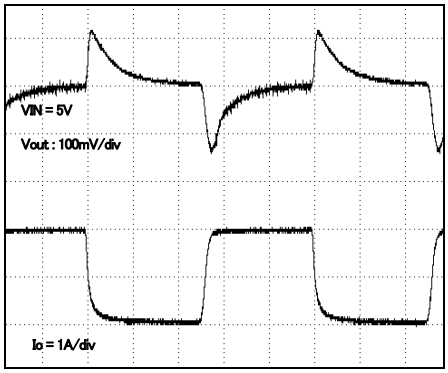


Fig.7 Output load response

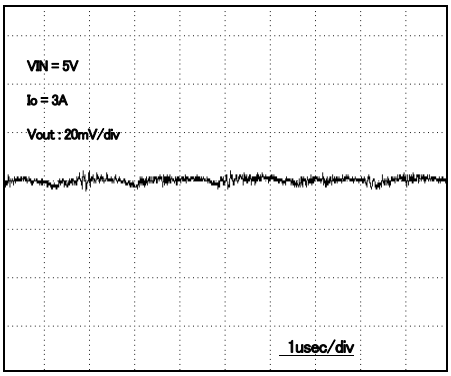


Fig.8 Output ripple

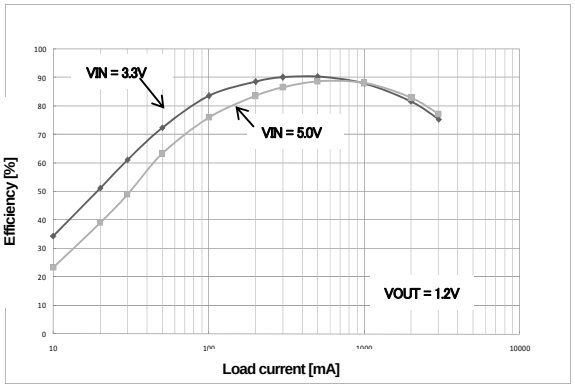


Fig.9 Efficiency

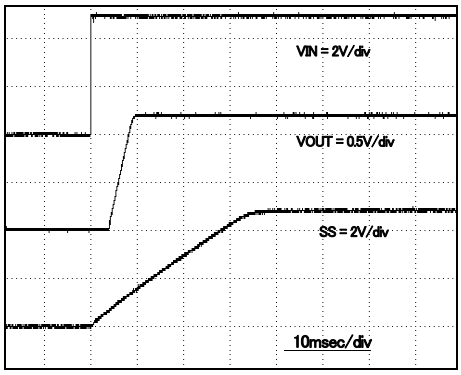


Fig.10 Soft start

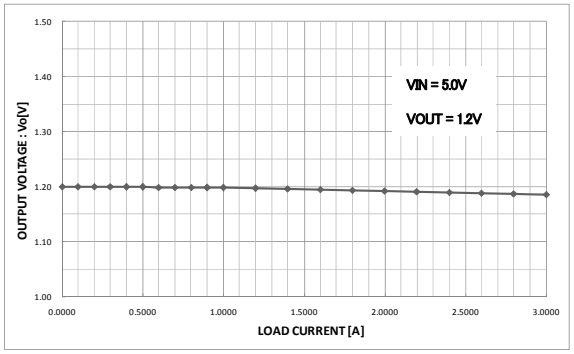


Fig.11 Regulation

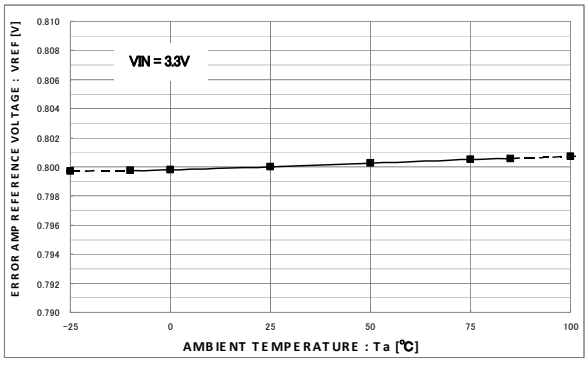


Fig.12 Reference voltage - Temperature characteristic

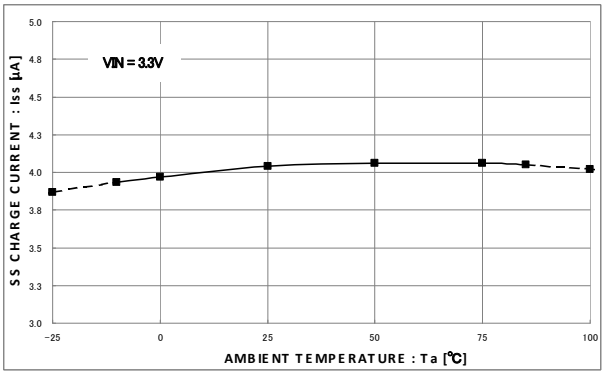


Fig.13 SS Charging current - Temperature characteristic

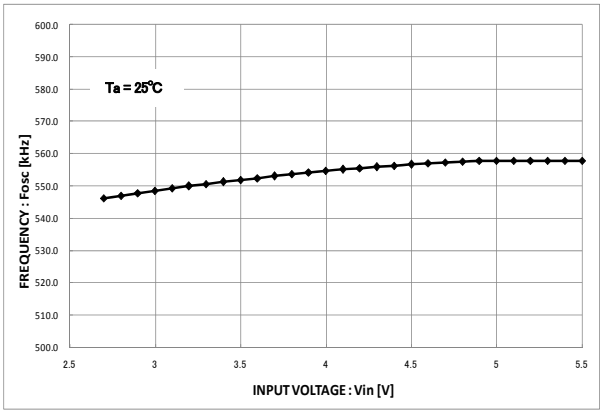


Fig.14 Switching frequency-power-supply voltage characteristic

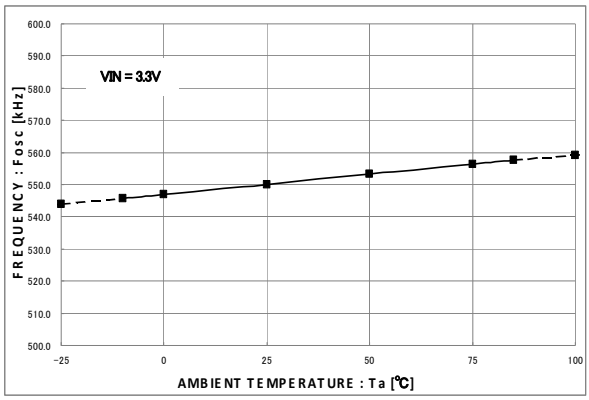


Fig.15 Switching frequency-temperature characteristic

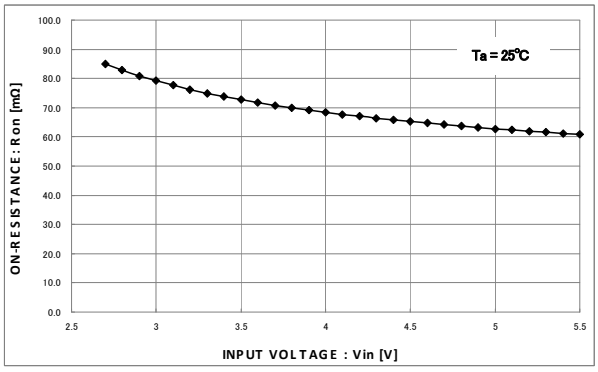


Fig.16 PMOS on resistance-power-supply voltage

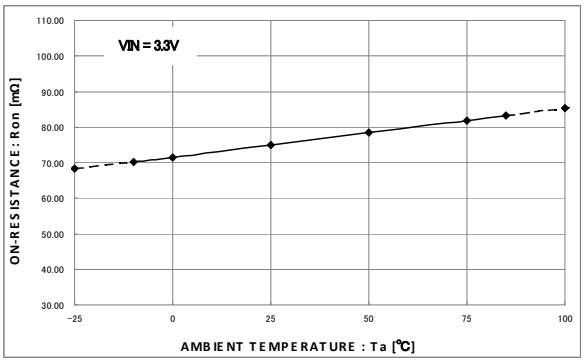


Fig.17 PMOS on resistance-temperature characteristic

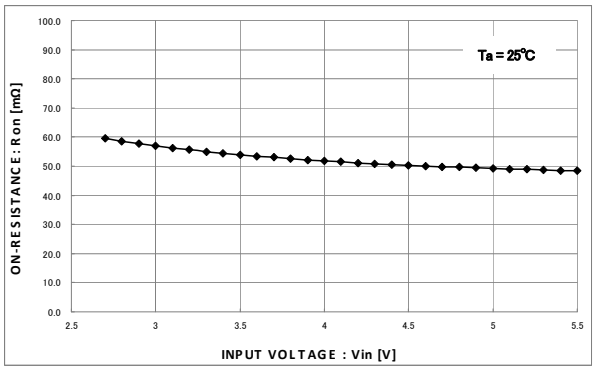


Fig.18 NMOS on resistance-power-supply voltage

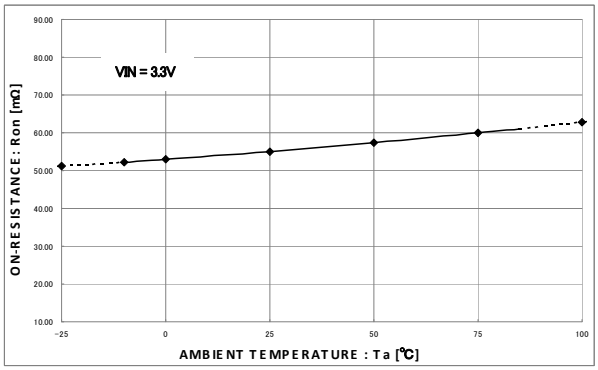


Fig.19 NMOS on resistance-temperature characteristic

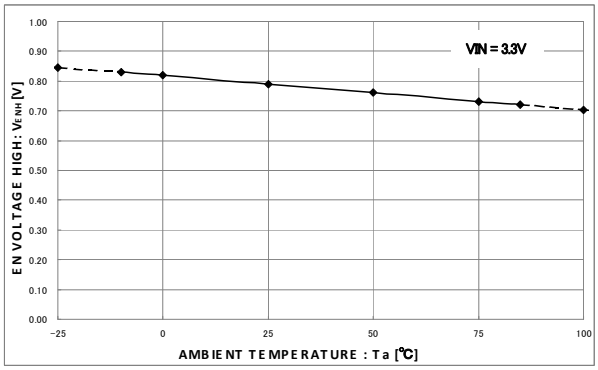


Fig.20 Terminal EN H voltage-temperature characteristic

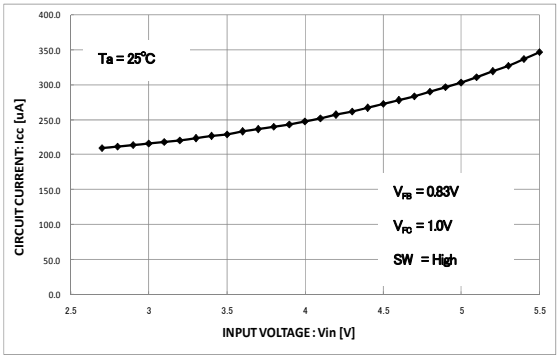
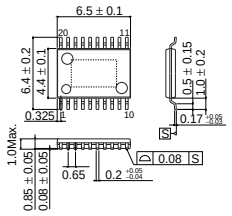


Fig.21 Circuit current-power-supply voltage characteristic

HTSSOP-B20

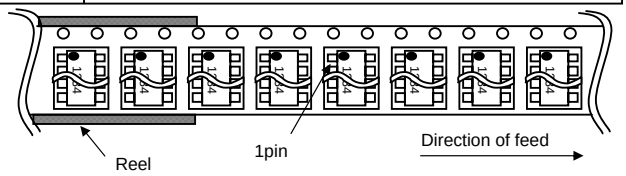
<Dimension>



(Unit:mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※When you order , please order in times the amount of package quantity.

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Espoo	TEL: +358-9725-54491	FAX: +358-9-7255-4499
Salo	TEL: +358-2-7332234	FAX: +358-2-7332237
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Barcelona	TEL: +34-9375-24320	FAX: +34-9375-24410
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