

# Power Supply IC Series for TFT-LCD Panels

## 5V Input Multi-channel System Power Supply IC


**BD9862MUV**

No.10035EAT16

**●Description**

The BD9862MUV is a 3ch system power supply for mobile TFT liquid crystal panels. Operable at VBAT=1.8V, CH2 & CH3 adopts the original PWM/PFM automatic switching control charge pump and realizes high efficiency in full-load range.

**●Features**

- 1) Input voltage range: 1.8V~4.5V (The input voltage can be 5.5V if a double charge pump is not used)
- 2) The step-up switching regulator has a built-in output FET (CH1)
- 3) There is a built-in PWM/PFM automatic switching charge pump circuit with a fixed PWM terminal (CH2,3)
- 4) Switching regulator oscillation frequency: MHz(typ.)
- 5) Charge pump oscillation frequency: 500kHz(typ.)
- 6) There is a built-in circuit to discontinue output (timer latch type) in the event of overload
- 7) Package VQFN024V4040

**●Applications**

Small & medium TFT liquid crystal displays etc.

**●Absolute Maximum Ratings (Ta = 25°C)**

Parameter	Symbol	Ratings	Unit
Maximum adding power supply voltage	VBAT	-0.3 ~ 7	V
Maximum adding voltage	LX	-0.3 ~ 18	V
	FB1, INV1, INV2, UVLOSET, C2N, VIN2A, CN, CP, CPOUT, REGOUT, PWM, RT, VREF, NON3	-0.3~7	
	VIN3, C3P, Vo2, C2P, VIN2B	-0.3~15.5	
Power dissipation	Pd	0.34(*1)	W
		0.70(*2)	
Operating temperature range	Topr	-40 ~ +85	°C
Storage Temperature Range	Tstg	-55 ~ +150	°C
Junction temperature	Tjmax	+150	°C

(\*1) When used as a stand-alone IC (for Ta=25°C and over), the value is reduced by 27mW/°C.

(\*2) When used for Printed Circuit Boards (glass epoxy board of 74.2mm×74.2mm×1.6mm) mounting for Ta=25°C and over, the value is reduced by 5.6mW/°C.

**●Operating Conditions(Ta=25°C)**

Parameter	Symbol	Ratings			Unit	condition
		MIN	TYP	MAX		
Power Supply Voltage	VBAT	1.8	-	4.5 <sup>(※1)</sup>	V	
CH1 Output Voltage	Vo1	-	-	15	V	
CH2 Output Voltage	Vo2	-	-	15	V	
CH3 Output Voltage	Vo3	-15	-	-	V	
Starting capacity, adding charge pump flying capacitor	Cflys, Cflya	0.1	0.22	-	μF	
Reversing capacity charge pump flying capacitor	Cflyi	0.022	0.047	-	μF	
Starting charge pump Output capacitance	CCPOUT	1.0	2.0	-	μF	CCPOUT ≥ Cfly*10
Switching regulator oscillation frequency	fOSC1	700	1.0	1.4	MHz	RRT=82kΩ~180kΩ
Charge pump oscillation frequency	fOSC2	350	500	700	kHz	RRT=82kΩ~180kΩ
CH1 PowerNMOS Drain current	lidn1	-	-	1.0	A	

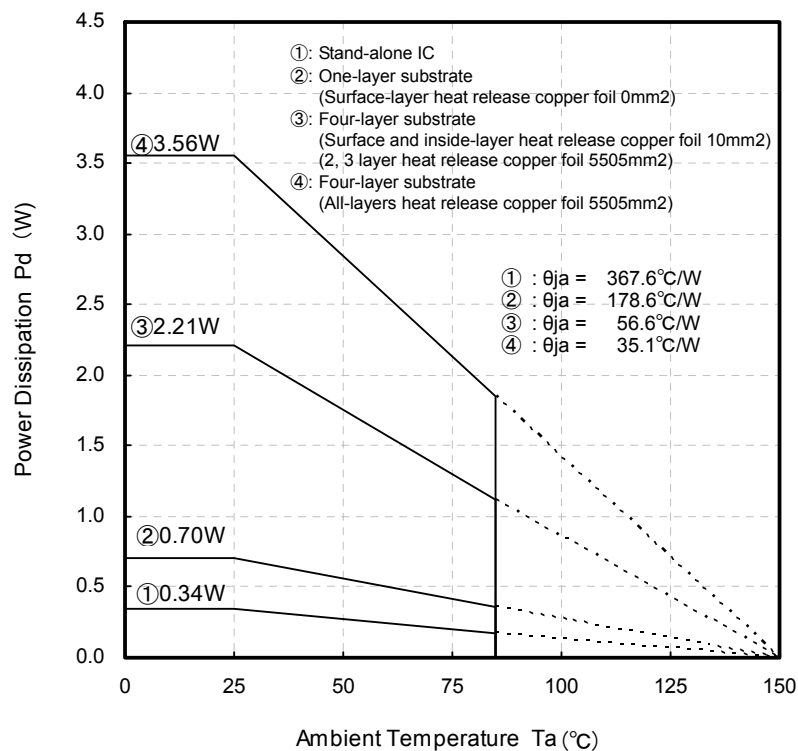
(※1) When using a double charge pump for starting. 5.5V when not using a double charge pump

**●Electrical Characteristics (unless otherwise specified, Ta=25°C, VBAT=2.5V)**

Parameter	Symbol	Limits			Unit	Condition	
		MIN	TYP	MAX			
<b>【Starting circuit part】</b>							
Output voltage	Vcpout	3.7	4.2	4.7	V	Iout=0~10mA	
VBAT Voltage to start operation	Vst	-	-	1.8	V		
<b>【Soft start part】</b>							
CH1 Soft start time	Tss1	0.5	1.0	2.0	ms	R <sub>RT</sub> =120kΩ	
CH2 Soft start time	Tss2	3.5	5.0	6.5	ms	R <sub>RT</sub> =120kΩ	
CH3 Soft start time	Tss3	3.5	5.0	6.5	ms	R <sub>RT</sub> =120kΩ	
<b>【Oscillation circuit】</b>							
Switching regulator frequency	fosc1	0.9	1.0	1.1	MHz	R <sub>RT</sub> =120kΩ	
Charge Pump Frequency	fosc2	450	500	550	kHz	R <sub>RT</sub> =120kΩ	
<b>【Regulator】</b>							
Output Voltage	VREGOUT	3.4	3.5	3.6	V	Iout=0~10mA, VBAT=2.0V~4.5V	
<b>【PWM Comparator】</b>							
MAX Duty1	Dmax1	85	90	95	%		
MAX Duty2	Dmax2	40	45	50	%		
MAX Duty3	Dmax3	40	45	50	%		
<b>【Error amplifier】</b>							
INV1 Threshold Voltage	VINV1	0.985	1.0	1.015	V		
INV2 Threshold Voltage	VINV2	0.985	1.0	1.015	V		
NON3 Threshold Voltage	VNON3	0.985	1.0	1.015	V	Making VREF as absolute value	
CH3 Error amplifier off set voltage	Voffset	-50	0	50	mV		
<b>【Output part(Switching Regulator)】</b>							
NMOSFET ON Resistance	RonN1	0.2	0.45	0.7	Ω	REGOUT=3.5V	
Leak current when NMOSFET OFF	IreakN1	-	-	10	μA	UVLOSET=0V	
<b>【Adding step-up charge pump】</b>							
Output impedance	R2	-	53	90	Ω	I <sub>o</sub> =0~10mA, VIN2A=3.5V, VIN2B=10V, INV2=GND	
<b>【Inverted charge pump】</b>							
Output FET ON resistance	PMOS	RonP3	-	20	40	Ω	VIN3=10V
	NMOS	RonN3	-	10	20		
<b>【Control Terminal Part】</b>							
PWM Terminal pull down resistance	RPWM	0.5	1	2	MΩ		
PWM Terminal control voltage	Operation	VPWMH	1.2	-	VBAT	V	PWM Fixed mode
	Non-operation	VPWML	0	-	0.3	V	PWM/PFM Auto shift mode
<b>【Short circuit protection circuit】</b>							
Timer Latch Time	Latch	110	131	150	ms	R <sub>RT</sub> =120kΩ	
<b>【UVLO】</b>							
Relief voltage threshold	UVth	0.97	1.0	1.03	V		
Hysteresis	UVhy	50	75	100	mV		
<b>【Circuit current】</b>							
Circuit current during operation (VBAT terminal inflow current)	IVBAT	0.4	0.8	1.6	mA	VBAT=5V, UVLOSET=INV1=INV2=5V, NON3=-0.2V	

©It is not the radiation-proof design for this product.

● Power Dissipation Reduction



●Reference Data(Unless specified Ta=25°C,VCC=2.5V,R<sub>RT</sub>=120kΩ)

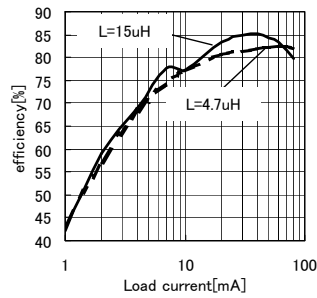


Fig.1 CH1 Current Load to Efficiency (Vo1=10V)

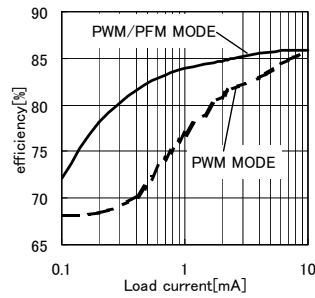


Fig.2 CH2 Current Load to Efficiency (VIN2A=3.5V, VIN2B=10V, Vo2=12V)

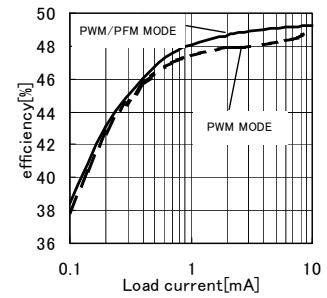


Fig.3 CH3 Current Load to Efficiency (VIN3=10V, Vo3=-5V)

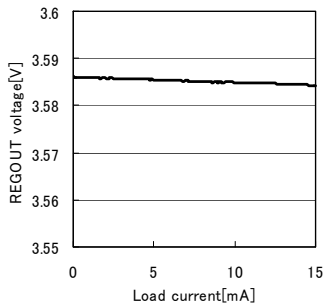


Fig.4 REGOUT Output Load Regulation

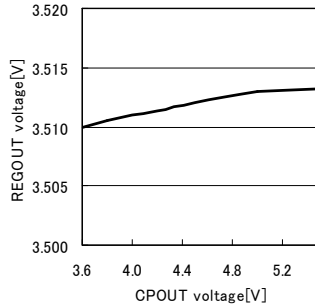


Fig.5 REGOUT Output Line Regulation

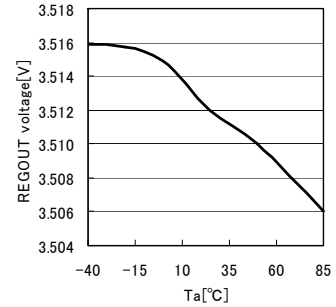


Fig.6 REGOUT Output Voltage Temperature Feature

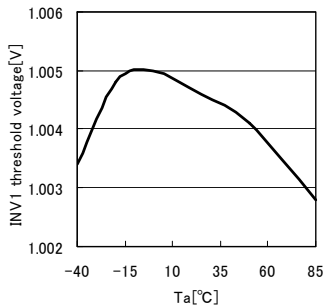


Fig.7 INV1 Threshold Voltage Temperature Feature

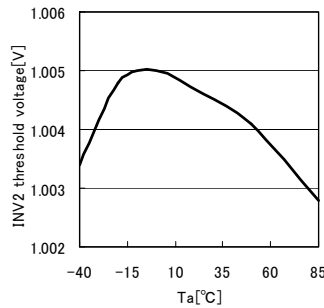


Fig.8 INV2 Threshold Voltage Temperature Feature

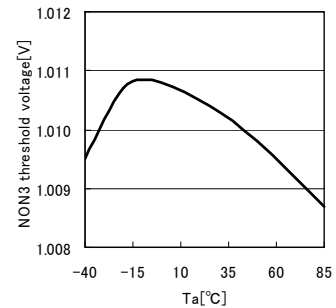


Fig.8 NON3 Threshold Voltage Temperature Feature

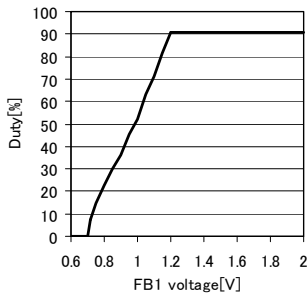


Fig.10 CH1 FB1 Voltage-On Duty Feature

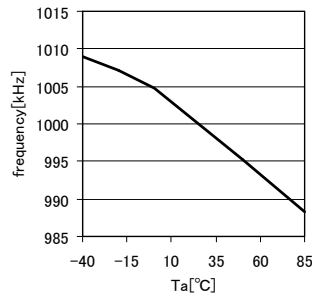


Fig.11 CH1 Switching Frequency Temperature Feature

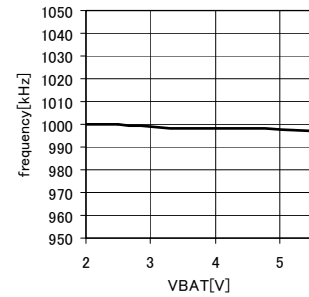


Fig.12 CH1 Switching Frequency to VBAT Voltage Feature

●Reference data(Unless specified Ta=25°C,VCC=2.5V)

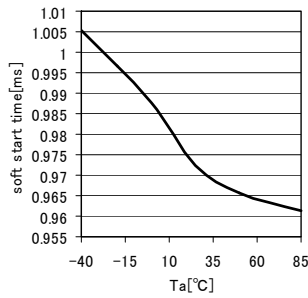


Fig.13 CH1  
Soft Start Temperature Feature

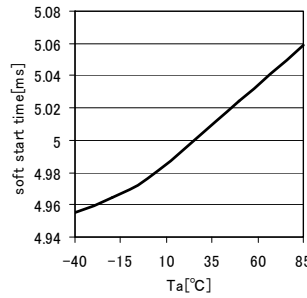


Fig.14 CH2,CH3  
Soft Start Temperature Feature

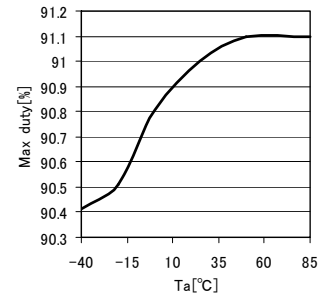


Fig.15 CH1  
Max Duty Temperature Feature

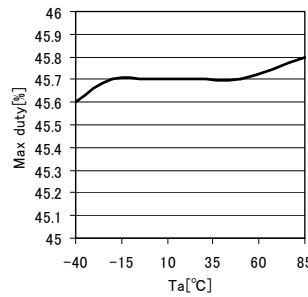


Fig.16 CH2,CH3  
Max Duty Temperature Feature

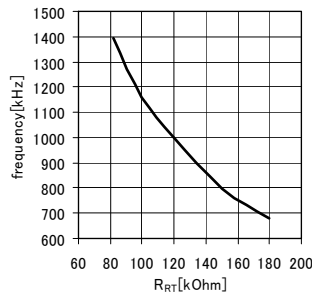


Fig.17 RT Resistance to CH1  
Switching Frequency Feature

●Block Diagram

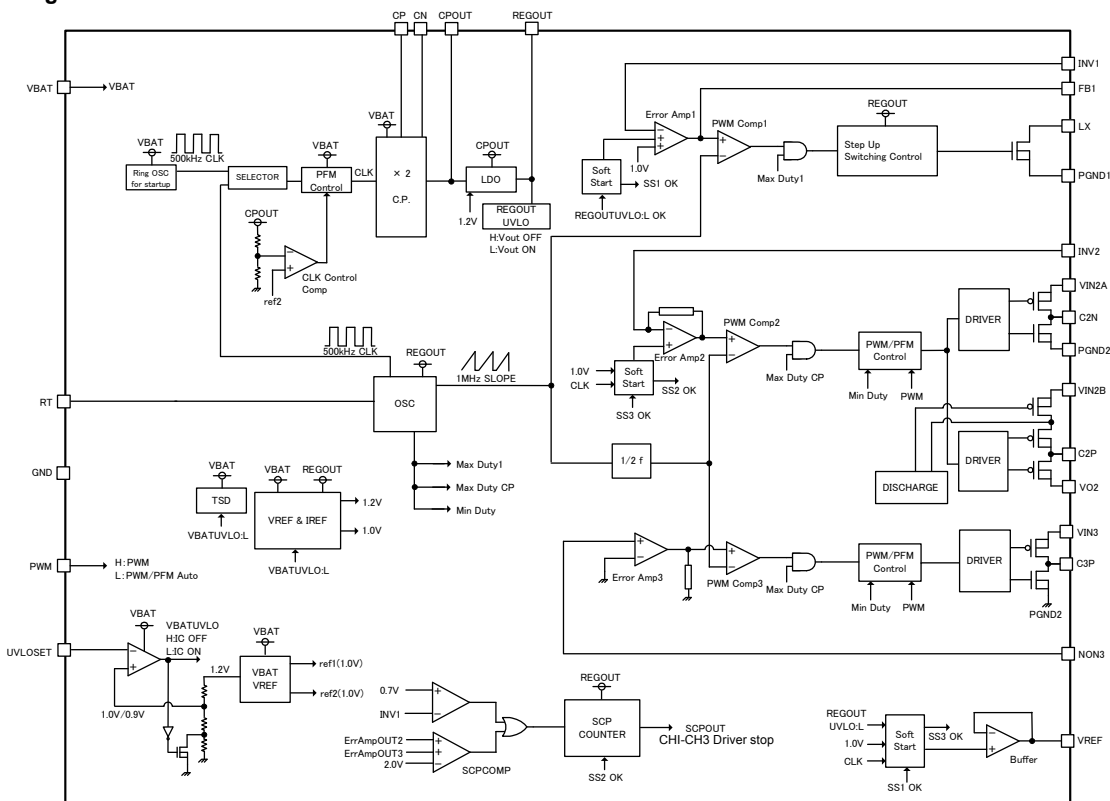


Fig.18

### ●Terminal Location Diagram

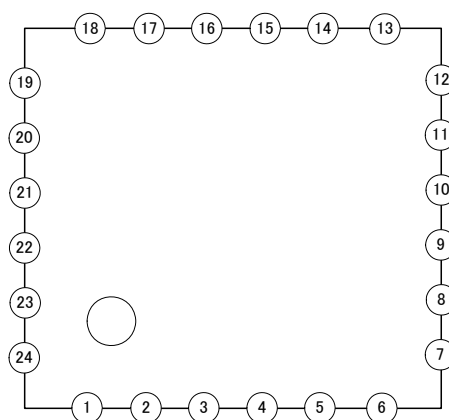


Fig.19

### ●Terminal Number and Terminal Name and Function

Terminal Number	Terminal Name	Function
1	FB1	Error amplifier output terminal for CH1
2	INV2	Error amplifier inverted input terminal for CH1
3	UVLOSET	UVLO Standard voltage terminal
4	VIN3	Reversing charge pump input terminal
5	C3P	Reversing charge pump. Flying capacitor H-side input terminal
6	PGND2	Built-in EFT grounding terminal for CH2,3
7	C2N	Adding step-up charge pump. Flying capacitor L-side input terminal
8	VIN2A	Adding step-up charge pump input terminal
9	VO2	Adding step-up charge pump output terminal
10	C2P	Adding step-up charge pump. Flying capacitor H-side input terminal
11	VIN2B	Adding step-up charge pump input terminal
12	LX	Inductor connecting terminal
13	PGND1	Built-in FET grounding terminal for CH1
14	CN	Start-up charge pump. Flying capacitor L-side input terminal
15	CP	Start-up charge pump. Flying capacitor H-side input terminal
16	VBAT	Power supply input terminal
17	CPOUT	Start-up charge pump output terminal
18	REGOUT	Regulator output terminal
19	PWM	Charge pump block PWM/PFM switching terminal
20	GND	Grounding terminal
21	RT	Connecting terminal of resistor for frequency timing setting
22	VREF	Standard voltage output terminal
23	NON3	Non-reversing input terminal of error amplifier for CH3
24	INV1	Reversing input terminal of error amplifier for CH1

## ●System Description

BD9862MUV is a 3ch system power supply optimized for TFT liquid crystal displays.

Features of each channel are explained as follows

### ○CH1

This is a voltage mode switching regulator with a built-in high voltage-resistant output FET. Capable of high-speed operation at the maximum switching frequency of 1.4MHz, and compatible with a high step-up ratio with Max Duty of 90%(typ.).

### ○CH2

It's a PWM/PFM automatic switching control with a variable-voltage adding charge pump. Due to intermittent switching at the time of PFM mode, the switching loss is reduced, so high efficiency is realized even in light load conditions. Moreover, it is capable of operating at the maximum switching frequency of 700KHz because of a built-in high voltage resistant, high-speed FET driver. In addition, it is equipped with an On Duty prediction function, so the output voltage ripple is lowered considerably even at the time of PFM operation. Due to the built-in output discharge resistor (1kΩ typ.) and FET phase compensation circuit, it can operate with two capacitors and two resistors.

### ○CH3

It includes a PWM/PFM automatic switching control, variable-voltage reversing charge pump controller. The control method is the same as CH2.

## ●Block functional descriptions

### • Error amplifier block

Detects the output voltage with INV terminal (NON3 terminal in case of CH3), amplifies the error between it and standard voltage, and outputs from the FB terminal. The accuracy is  $\pm 1\%$  (1.5% in case of CH2 & CH3).

### • PWM(Pulse Width Modulation)Convertor block

The PWM convertor inputs the error detected by the error amplifier and outputs the PWM signal by comparing with a saw-tooth wave.

### • PWM/PFM Control Block

Due to the input of the PWM terminal, this block switches the CH2 & CH3 between the fixed PWM mode and the automatic switching mode of PFM(Pulse Frequency Modulation)/PWM. At the time of PFM mode, the efficiency under a light load is raised by controlling and making the lowest On Duty of PWM signal to be 7%(typ.) and reducing the number of switching times.

### • LDO Block

This is a power supply to operate the internal circuit. In addition, it can be used as input of VIN2B. The output voltage is 3.5V(typ.), and the maximum load is 10mA. Moreover, due to a built-in UVLO, the release voltage is 2.5V(typ) and the protective voltage is 2.4V(typ).

### • Start-up Charge Pump Block

If REGOUT is  $\leq 2.5V$ (typ.), then the ring oscillator, which operates at 500kHz or so, is started and the double charge pump is operated. The clock pulse is controlled in such a way that the output voltage of this charge pump becomes 4.2V(typ.). Moreover, if REGOUT becomes more than 2.5V(typ.) (i.e.  $REGOUT > 2.5V$ (typ.)), then the clock is supplied from the main OSC that creates a saw tooth wave. If the input voltage is usually more than 4.5V, then it is possible to bypass the start-up circuit. (refer to the application example)

### • OSC Block

It generates a saw-tooth wave and inputs it into the PWM comparator. It is possible to change the oscillating frequency by means of the resistor RT. Due to  $RRT=120k\Omega$ , the CH1 operates at 1MHz(typ.). The double charge pump, CH2 and CH3 operate at 1/2 of CH1 frequency.

### • VREF Block

Generate the constant voltage that is standard inside the IC.

### • UVLO Block

Performs the under voltage lockout by detecting the VBAT voltage with the UVLOSET terminal. The UVLO voltage can be set by an external resistor.

### • Soft Start Block

Due to sweep-starting of the standard voltage of the error amplifier at the time of start-up, the excess input current & output voltage is reduced. Moreover, only at the time of soft start, the CH2 is regarded as the resistance value of 150Ωtyp between VIN2B & C2P and the CH3 is regarded as the resistance value of 60Ωtyp between VIN3 & C3P therefore the input current is limited.

### • Short-circuit protection of timer latch (SCP) block

Monitors the INV1 terminal and the error amplifier outputs of CH2 & CH3, and turns off the drivers of CH1~CH3 if a short-circuit condition continues for more than a certain period of time. The timer latch time is counted by the CH1 internal switching pulse. The counting is started when a short-circuit condition begins, and the drivers are turned off when 131,072 is reached.

Example) if  $RRT=120k\Omega$ , then  $131072 \times (1/1[\text{MHz}])=131.072\text{ms}$

### • Thermal shutdown (TSD) block

Detects abnormal heat generation of the IC, stops the switching operation of all Ch and prevents the IC from thermal overload. The detecting temperature is 175°C(typ), and the hysteresis is 10°C(typ).

●Timing Chart

1) When Starting

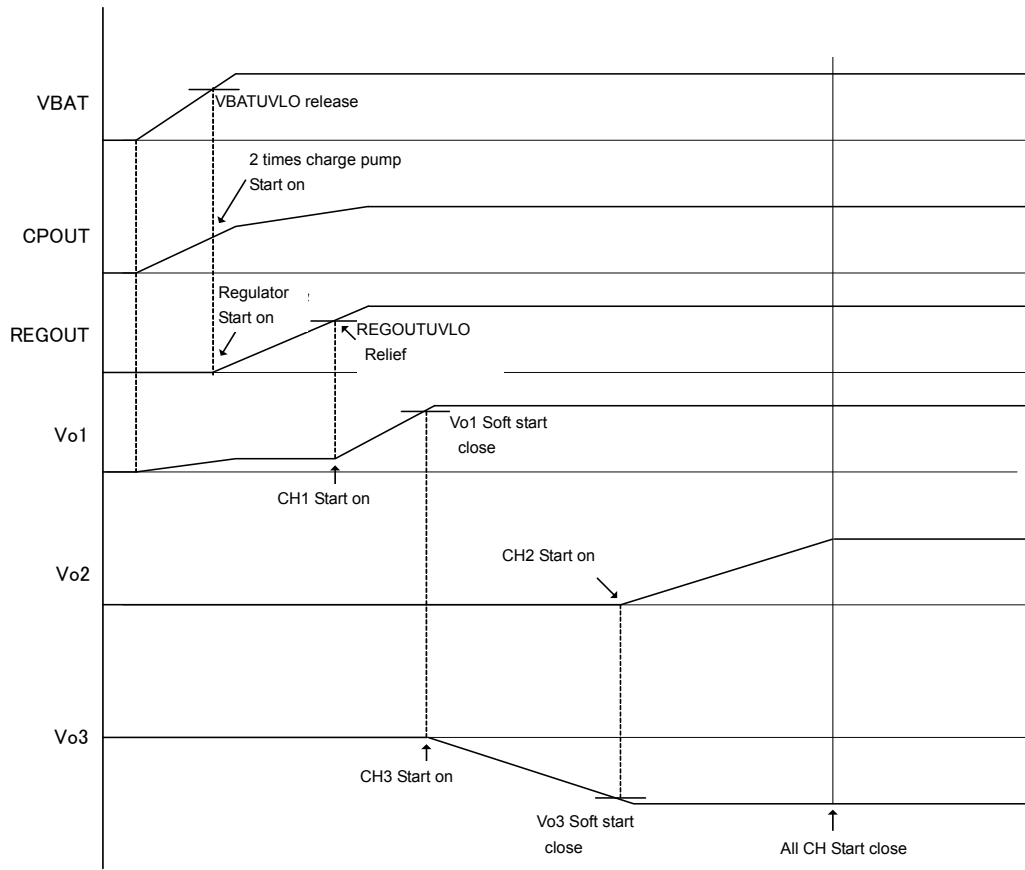


Fig.20

2) Sample SCP Operation When CH1 is short

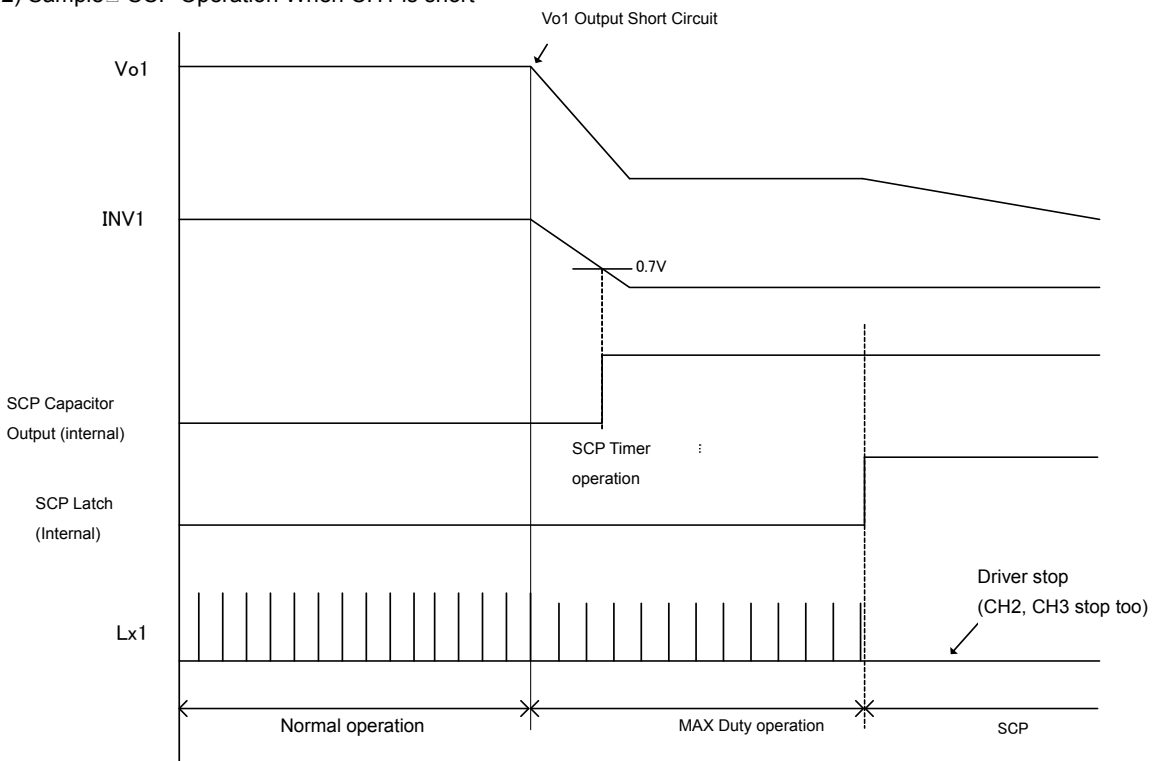
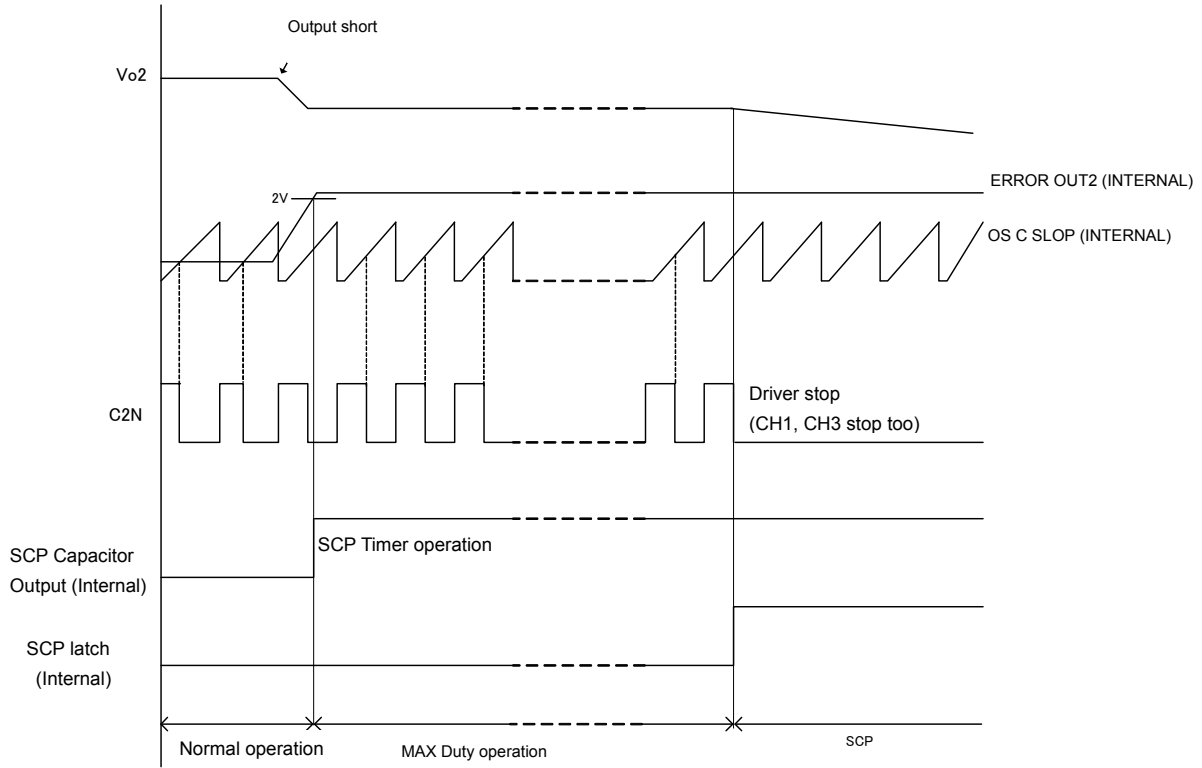


Fig.21



3) Sample② SCP Operation When CH2 is Short



※Operates similarly at the time of CH3 short-circuit.

Fig.22

### ●Method to select the application parts

#### 1) Setting of output voltage

The output voltage VOUT is set by dividing the resistance of the external resistor.

$$\text{CH1,CH2:VOUT}=1+R2/R1$$

$$\text{CH3:VOUT}=-((R4/R3)+V\text{offset})$$

R1: Feedback resistor (GND side), R2: Feedback resistor (VOUT side), R3: Feedback resistor (VREF side),

R4: Feedback resistor (VOUT side)

#### 2) Setting of the output inductor

The maximum current  $I_{L\text{peak}}$  that flows in the inductor is calculated by the sum of the average current  $\bar{I}_L$  and the maximum value of ripple current  $\Delta I_L$ .

$$I_{L\text{peak}} = \bar{I}_L + \Delta I_L$$

Generally  $\Delta I_L$  is set to about 30% of  $\bar{I}_L$ .

The average current  $\bar{I}_L$  and the ripple current  $\Delta I_L$  are calculated according to the following formulas.

$$\bar{I}_{L\text{max}} = \frac{V_{\text{out}}}{V_{\text{inmin}}} I_{\text{outmax}} \quad \Delta I_L = \frac{V_{\text{inmin}} \times (V_{\text{out}} - V_{\text{in}})}{2 \times f_{\text{osc}} \times L \times V_{\text{out}}}$$

L: value of inductance  $f_{\text{osc}}$ : switching frequency  $V_{\text{inmax}}$ : maximum input voltage  $V_{\text{inmin}}$ : minimum input voltage

Vout: set value of output voltage

Please set in such a way that  $I_{L\text{peak}}$  (the rated value of inductor current) is not exceeded. If  $I_{L\text{peak}}$  exceeded, then the efficiency is lowered extremely and damage to the inductor is caused. Please set in such a way that a good margin is left because the inductance varies in value.

#### 3) Setting of output capacitor

The capacitance & ESR of the output capacitor is influenced a great deal by output voltage ripple. Moreover, PFM mode intentionally makes the switching intermittent, so the output voltage ripple becomes larger compared with PWM mode. Please use an appropriate capacitor according to the service condition. In addition, please be sure to connect a ceramic capacitor of 1 $\mu$ F to REGOUT terminal.

It is assumed that this IC uses a multilayer ceramic capacitor. For small multilayer ceramic capacitors such as Size 1608 etc., its actual capacitance may be lower than its nominal one because of the voltage that is bypassed. Please check to confirm various characteristics such as DC bypass etc. before use.

#### 4) Setting of flying capacitor

Please set the capacitance of the flying capacitor of the start-up charge pump not to exceed 1/10 of the capacitance of the CPOUT output capacitor. If it is more than 1/10 of the capacitance, damage may be caused.

#### 5) Setting of the input capacitor

A bypass capacitor for input is necessary to the VBAT terminal. Due to input & output voltage, load and wiring pattern etc., the actual capacitance is different from the necessary one, so please carefully check to confirm.

#### 6) Setting of CR for phase compensation

The CR for phase compensation is varied due to the characteristics of the capacitor & inductor, which are used in the output part, the input & output voltage and the load current etc. The phase-compensation CR constant in a recommended circuit diagram is set according to the service conditions, but applications under other conditions than the various conditions mentioned will cause oscillation instability etc. Please contact our technical service department if any conditions are changed.

#### 7) Setting of schottky diode in the output part

Please use a schottky diode with an allowable current more than  $I_{L\text{peak}}$  for the output part. Furthermore, it is necessary that the maximum reverse voltage is more than output voltage. Generally speaking, more lower the forward voltage, the higher the efficiency.

#### 8) Setting of UVLO voltage

The VULO release voltage VUVLO can be set according to the following formula:

$$VUVLO=1+R2/R1(R1=\text{GND-side resistance} \quad R2=\text{VBAT-side resistance})$$

If you want to make the start-up of the IC to lag behind the rising edge of VBAT, connect a capacitor to the UVLOSET terminal and set the time constant.

#### 9) Setting of oscillating frequency

Oscillating frequency can be adjusted by a resistor connected to the RT terminal.

The CH1 oscillating frequency  $f_{\text{osc1}}$  is determined by the formula shown below:

$$f_{\text{osc1}}=1/(8 \times 10^{-12} \times R_{RT} + 4 \times 10^{-8})$$

The frequency calculated by the formula shown above is a theoretical value, so please refer to the above-mentioned reference data 「RT resistance vs. CH1 switching frequency characteristic」 for actual frequency.

**●Operating Guidelines**

## • PWM terminal

At Low the PFM mode skips the pulse of less than 7% On Duty. It is also switched over to the PWM mode if a certain amount of load is reached or exceeded while in PFM mode. Moreover, it is switched to PFM mode if the load becomes light. Please set the PWM terminal to High and use as the forced PWM mode if there is an influence of noise created by modulation of the switching frequency.

## • SCP Function

In case of circuit stoppage due to SCP, the protection is released by setting the UVLOSET voltage to L and the VBATT to OFF.

## • CH2 adding charge pump

Please set the Vo2 so that the VIN2A+VIN2B become not more than 15V because the voltage that is the sum of the VIN2A voltage plus the VIN2B voltage is applied.

● Sample of Recommended Circuit

1) Sample of Input voltage 1.8V~4.5V application

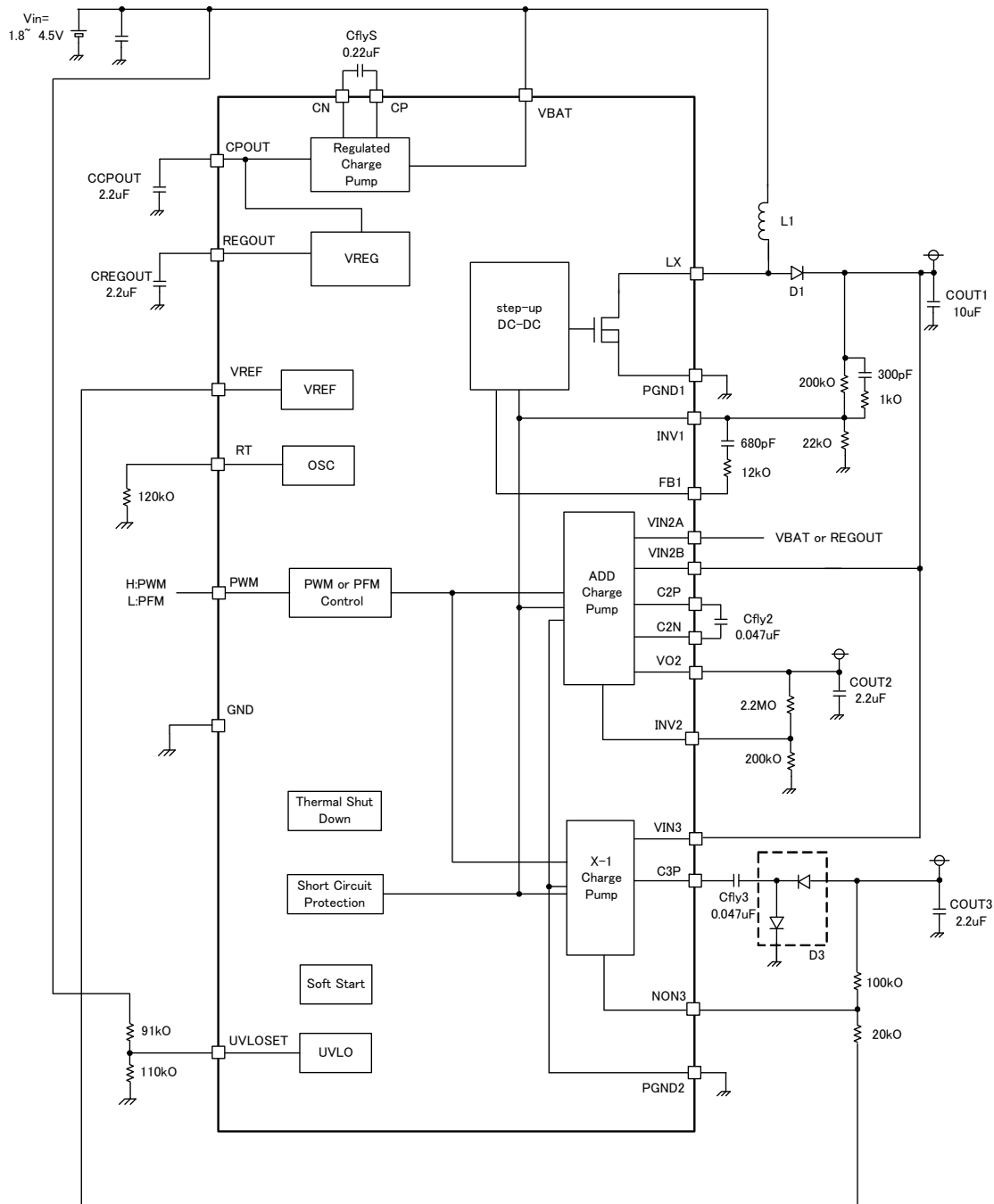


Fig.23

• Recommended Parts

L1	: NR4010T4R7M(TAIYO YUDEN)	CCPOUT	: GRM188B30J225KE18(MURATA)
D1	: RB161VA-20(ROHM)	CREGOUT	: GRM155B30J105KE18 (MURATA)
D3	: DAN217U(ROHM)	COUT2, COUT3	: GRM188B31C225KE14D(MURATA)
COUT1	: GRM31CB31C106KA88(MURATA)	CflyS	: GRM155B10J224KE01(MURATA)
CIN	: GRM219B30J106KE18(MURATA)	Cfly2, Cfly3	: GRM155B11C473KA01(MURATA)

2) Sample of Input voltage 4.5V~5.5V application

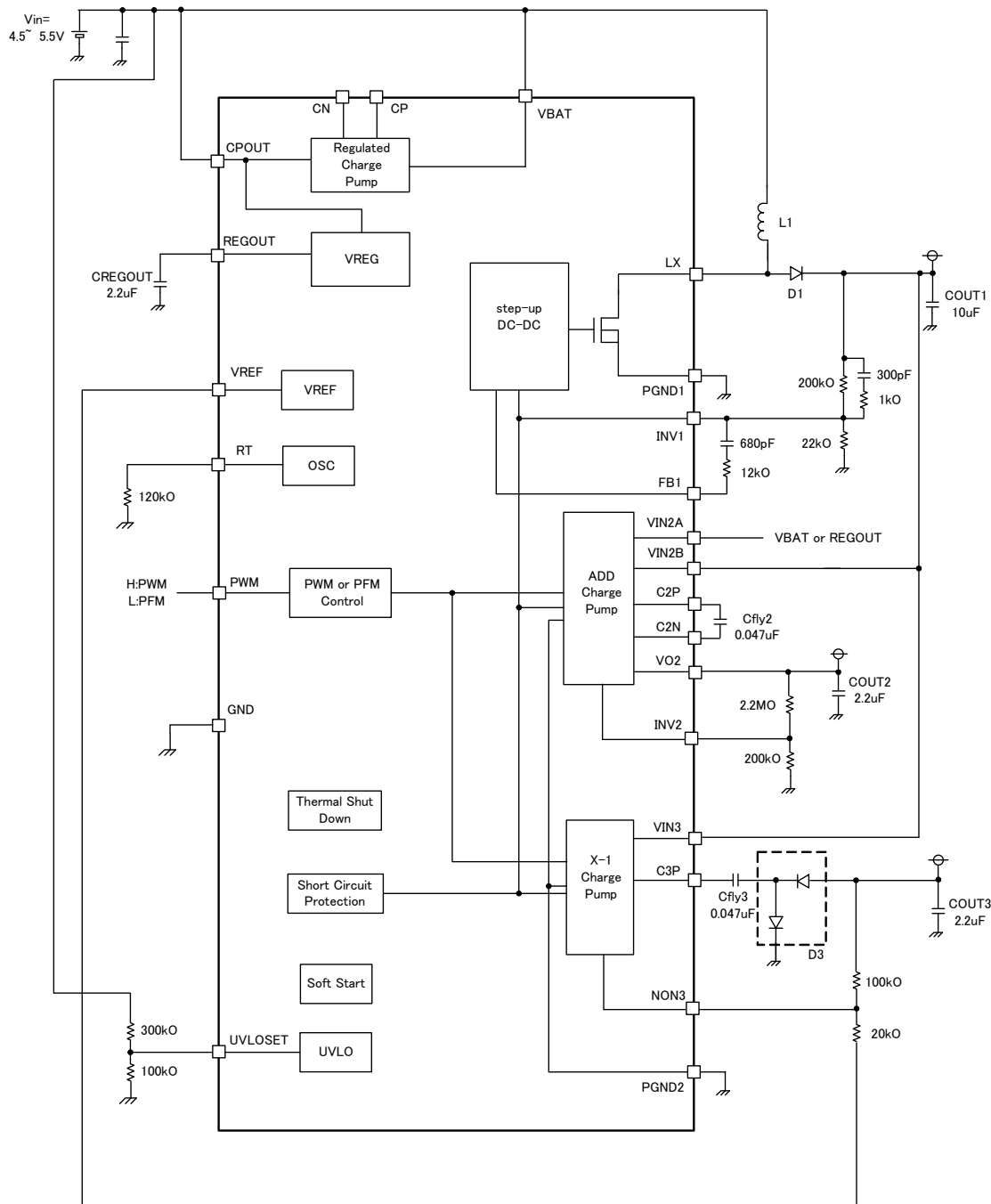


Fig.24

• Recommended Parts

L1	: NR4010T4R7M(TAIYO YUDEN)	CCPOUT	: GRM188B30J225KE18(MURATA)
D1	: RB161VA-20(ROHM)	CREGOUT	: GRM155B30J105KE18(MURATA)
D3	: DAN217U(ROHM)	COUT2, COUT3	: GRM188B31C225KE14D(MURATA)
COUT1	: GRM31CB31C106KA88(MURATA)	Cflys	: GRM155B10J224KE01(MURATA)
CIN	: GRM219B30J106KE18(MURATA)	Cfly2, Cfly3	: GRM155B11C473KA01(MURATA)

●Input / Output Equivalent Circuit

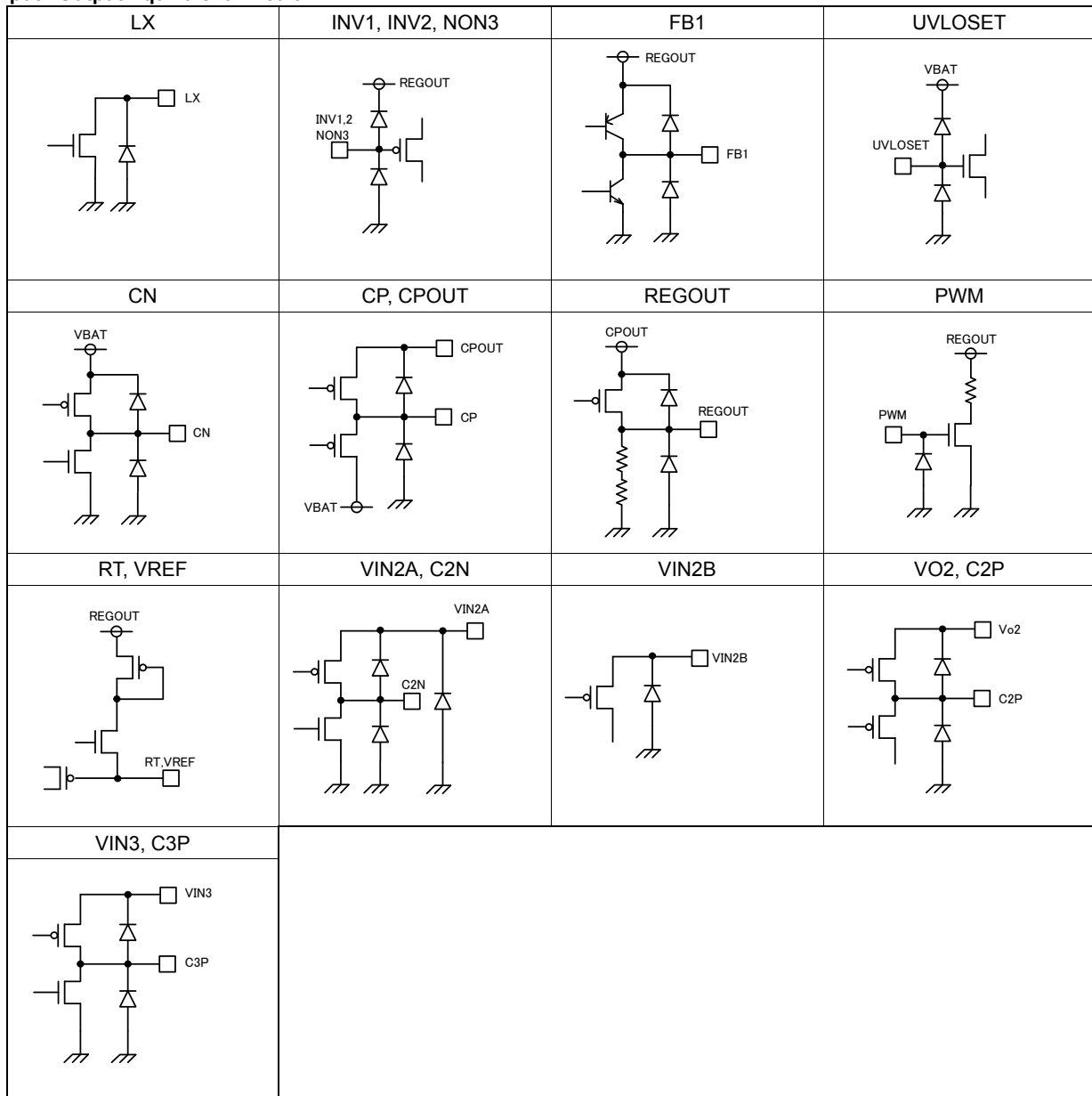


Fig.25 Input / Output Equivalent Circuit

●Points for attention on PCB layout

- ①Place the resistors and capacitors, that are connected to RT, INV1, FB1, INV2, NON3 and VREF, close to the terminals to avoid being affected by the wirings, where switching is large, such as LX1 wiring and flying capacitor wiring etc.
- ②Place the inductor, schottky diode and flying capacitor close to the IC.
- ③Mount in such a way that the back side of the package serves as the GND potential which covers the largest space in the PCB. Heat dissipation performance is improved.

### ●Notes for Use

#### 1.) Absolute maximum ratings

This is a high quality product, but if absolute maximum rating such as applied voltage and operating temperature range is exceeded, then deterioration or breakdown may result. Moreover, such destructive conditions as short mode or open mode can not be assumed. If a particular mode such as exceeding the absolute maximum rating is assumed, consideration should be given to using physical safety measures such as a fuse.

#### 2.) CND Potential

The electric potential of the GND pin should be the lowest electric potential under any operating state.

In addition, (including transient phenomenon), do not make the electrical potential of any pin lower than the GND's.

#### 3.) Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

#### 4.) Inter-pin shorts and mounting errors

Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC.

In addition, shorts between output pins or between output pins and the power supply GND pin caused by the presence of a foreign object may result in damage to the IC.

#### 5.) Operation in a strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

#### 6.) Common impedance

Power supply and GND wiring should reflect consideration of the need to minimize ripples as much as possible., (which lower common impedance), by making wiring as short and thick as possible or incorporating inductance and capacitance.

#### 7.) Thermal shutdown circuit (TSD circuit)

This IC incorporates a built-in thermal shutdown circuit (TSD circuit). The TSD circuit is designed not for the purpose of protection & guarantee of the IC, but only to shut the IC off to prevent thermal overload. Therefore, do not use the IC on the premise that this TSD circuit will be operated to shut the IC off (or the IC will be continued to be used after this TSD circuit is operated to shut the IC off).

#### 8.) IC pin input

This monolithic IC contains the P+ isolation between adjacent elements in order to keep them isolated from the P substrate. Due to this P layer and the N layer of each element, the P/N junctions are formed and various kinds of elements are created.

For example, if a resistor and a transistor are connected with pins as shown in the Fig., then:

- the P/N junction functions as a parasitic diode when

GND > (Pin A) for the resistor or GND > (Pin B) for the transistor (NPN).

- Moreover, when GND > (Pin B) for the transistor (NPN),

the parasitic NPN transistor is operated by N layer of other elements adjacent to the above-mentioned parasitic diode.

The formation of parasitic elements as a result of the relationships of electric potentials is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with the circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements, such as by the application of voltages lower than the GND (P substrate) voltage to input pins.

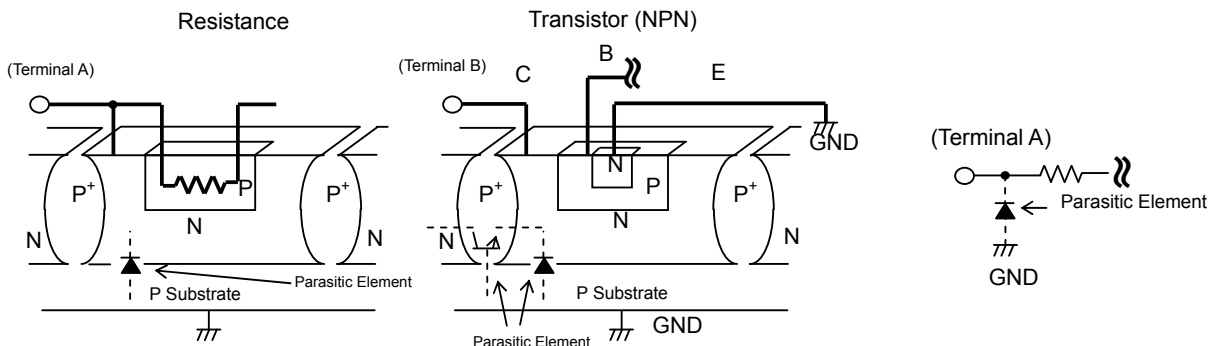
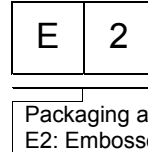
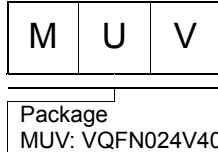
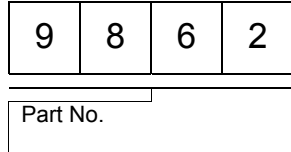
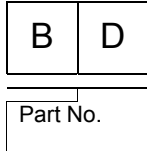
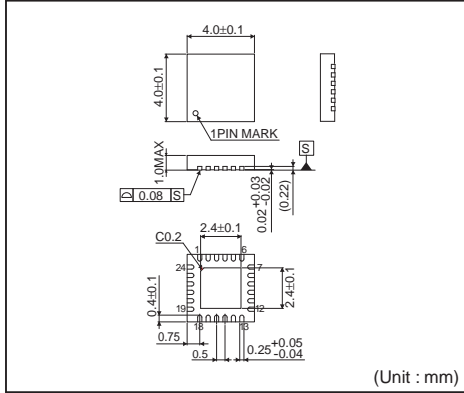


Fig.26 Simple Structure of monolithic IC (Sample)

● Ordering Part Number



VQFN024V4040



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 ( The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand )

\*Order quantity needs to be multiple of the minimum quantity.



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