STURUCTURE Silicon Monolithic Integrated Circuit

Type 4 Channel Switching Regulator control system for DSC

PRODUCUT SERIES BD9855MWV

THYSICAL DIMENSIONS Package(Plastic Mold) Fig.1、Block Diagram Fig.2、Pin Description Fig.3

FEATURES ●Include step-down 2ch,Cross converter 1ch,step down/inverting 1ch.
●Short Circuit Protection (SCP), Under Voltage Lockout Function (UVLO),
Include external synchronous rectification operation
●Independent ON/OFF Function Each Channel、UQFN044V6060 Package（0.4mm pitch）

○Absolute Maximum Ratings（Ta=25℃）

Parameter	Symbol	Limits	Units
Power Supply Voltage	VCC,PVCC	−0.3～15	V
Input Voltage	BST1-LX1、BST2-LX2	−0.3～7	V
	LX31	−0.3～15	V
	Vo3,LX32	−0.3～8.4	V
	PG,SYNC, CTL1,2,3,4	−0.3～15	V
	SEL	−0.3～7	V
Power Dissipation	Pd	540(*1),1000(*2)	mW
Operating Temperature	Topr	−25～+85	℃
Storage Temperature	Tstg	−55～+150	℃
Junction Temperature	Tjmax	150	℃

(*1) Without external heat sink, the power dissipation degrades by 4.2mW/℃ above 25℃.
(*2)Power dissipation degrades by 8.0mW/℃ above 25℃, when mounted on a PCB (70mm×70mm×1.6mm).

○Operating Conditions

Parameter	Symbol	Spec.			Unit	Condition
		MIN	TYP	MAX		
【Input Voltage】						
Power Supply Voltage	VCC,PVCC	4	6	14	V	
【Reference Output】						
VREG,VREGA terminal capacitor	CVR*	0.47	1.0	2.2	μF	
VREF terminal capacitor	CVREF	0.047	0.1	2.2	μF	
【Protect Circuit】						
SCP terminal capacitor	CSCP	0.001	−	2.2	μF	
【Oscillator】						
Oscillator frequency	Fosc	0.6	1.0	1.5	MHz	
OSC timming resistor	RT	47	82	120	kΩ	
RTSS terminal capacitor	CRTSS	1000	10000	−	pF	
SYNC terminal input H	VSYNCH	3.0	-	VCC	V	
SYNC terminal input L	VSYNCL	-0.3	-	0.5	V	
SYNC terminal input Duty	Dsync	40	50	60	%	
【Driver】						
BST-Lx voltage	Vbst	3.5	−	5.5	V	
BST-Lx capacitor	Cbst	0.047	0.1	0.22	μF	
LX31terminal input voltage	VLX31	−	−	14	V	
CH3 output range	VVOUT3	4.0	−	7.0	V	
PVCC1,2,4 terminal input voltage	PVCC1,2,4	−	−	14	V	
CH1,2,3output current	Ioutch1,2,3	−	−	1	A	

※)Please connect capacitor at input/output terminal (VCC,PVCC,VREF,VREG etc.) to operate IC stabilize.

Status of this document

The Japanese language version of this document shall be the official specification.

Any translation of this document shall be for reference only.

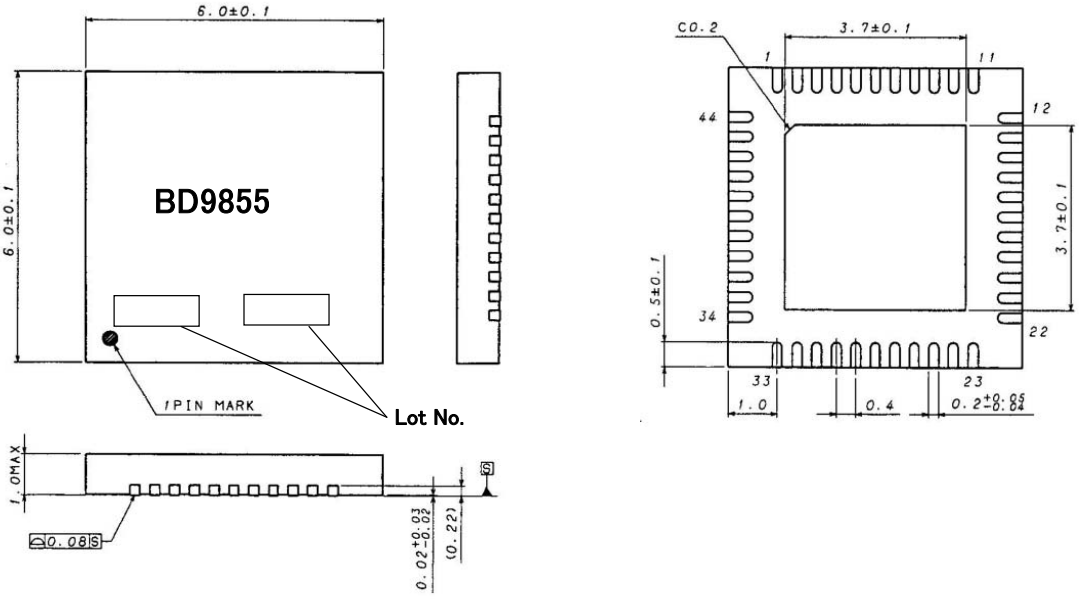
○Electrical Characteristics（Ta=25℃, VCC=PVCC=6V, RT=82kohm, CTL1～4=3V with no designation）

Parameter	Symbol	Standard value MIN	TYP	MAX	Units	Conditions	Test circuit
【Internal Regulator】							
Regulator Output voltage for Boost terminal	VREG	4.8	5	5.2	V	Ireg=1mA	
Regulator Output Voltage for inside standard	VREGA	2.4	2.5	2.6	V	Ireg=1mA	
【Under Voltage Lock Function】							
Threshold Voltage1,2	Vstd1,2	3.4	3.6	3.8	V	VCCMonitor,VREGMonitor	
Hysterisis voltage width	Vhys1,2	—	0.1	0.2	V	VCC cancel ,VREG cancel	
【Short Circuit Protection】							
Timer Start Threshold Voltage	Vtc	2.1	2.2	2.3	V	FB Pin Monitor	
SCP Out Source Voltage	Iscp1	2.5	5	7.5	μA	VSCP=0.1V	
SCP Threshold Voltage	Vtsc	0.45	0.5	0.55	V		
Stand by Voltage	Vssc	—	10	100	mV		
【Oscillator】							
Frequency CH1～3	fosc123	0.8	1	1.2	MHz	RT=82kΩ、SEL=GND	
Frequency CH4	Fosc4	0.4	0.5	0.6	MHz	RT=82kΩ、SEL=VREGA	
Max duty 1,2(Step Down)	Dmax1,2	–	–	100	%	Vscp=0V ※	
Max duty CH3 Lx31	Dmax31	–	–	100	%		
Max duty CH3 Lx32	Dmax32	78	84	90	%		
Max duty 4	Dmax4	86	92	96	%	SEL=VREGA	
RTSS Pin Standby Voltage	RTSSF	–	1	20	mV	CTL1～4=0V	
RTSS Pin smk Current	IRTSSI	−7	−5	−3	μA		
RTSS Pin source Current	IRTSSO	3	5	7	μA		
【Error AMP】							
Input Bias Current	IINV	–	30	100	nA	INV1～4, NON4=0V	
INV Threshold Voltage 1	VINV1	0.79	0.8	0.81	V	CH1～3	
NON_INVoffset Voltage	Voff	–	–	5	mV	NON4=1V, INV4=FB4	
【Reference Voltage VREF】							
VREF Output Voltage	VOREF	0.99	1	1.01	V		
Line Regulation	DVLi	–	1	7.5	mV	VCC=4.8～8.4V	
Load Regulation	DVLo	–	1	7.5	mV	Iref=10μA～100μA	
Output Current when shorted	Ios	2	10	–	mA	Vref=0V	
【Soft Start】							
SS1,2,3,4 source current	Iss	1	2	3	μA	VSCP=0.1V	
SS Discharge Resistance	RdisSS	–	500	1000	Ω	Vss=0.2V	
【Output Driver】							
CH1,2 Highside SW ON Resistance	RON12p	–	200	350	mΩ	ILX=50mA	
CH1,2 Highside SW ON Resistance	RON12N	–	150	300	mΩ	ILX=−50mA	
CH3 Driver Output Voltage H	Vout3H	PVCC−1.0	PVCC −0.5	–	V	IOUT3=50mA	
CH3 Driver Output Voltage L	Vout3L	–	0.5	1	V	IOUT3=−50mA	
CH3 Lx31Pin Lowside SW ON Resistance	RON31N	–	250	400	mΩ	ILX=−50mA	
CH3 Lx32Pin Highside SW ON Resistance	RON32p	–	200	350	mΩ	Vo3=6.0V, ILX=50mA	
CH3 Lx32Pin Lowside SW ON Resistance	RON32N	–	150	300	mΩ	ILX=−50mA	
CH4 Driver Output Voltage H	Vout4H	PVCC−1.0	PVCC −0.5	–	V	IOUT4=50mA,INV4=1.1V	
CH4 Driver Output Voltage L	Vout4L	–	0.5	1	V	IOUT4=−50mA,INV4=0.9V	
【PG Output Pin】							
PG Pin ON Resistance	RonPG	–	0.5	1	kΩ	PG=1V	
PG Pin Leak Current	IlkPG	–	0	1	uA	PG=15V	
【Control terminal】							
CTL terminal voltage(ON),	VCTLH	2	–	Vcc	V		
CTL terminal voltage (OFF),	VCTLL	−0.3	–	0.8	V		
SEL terminal voltage (? frequency)	VSELH	2	–	7	V		
SEL terminal voltage (same frequency)	VSELL	−0.3	–	0.8	V		
CTL,SEL Pull down Resistance	RCTL,RSEL	250	400	700	kΩ		
【Circuit Current】							
STAND-by Current	ISTB	–	0	5	μA	CTL1～4=0V	
Circuit Current（VCC,PVCC Pin Input Current）	Icc	–	4	8	mA	INV=2.5V,NON=1V	
Circuit Current（Application Io=none）	Iccapl	–	25	35	mA	All CH ON	

※The protective circuit start working when circuit is operated by 100% duty. So it is possible to use only for transition time shorter than charge time for SCP.

◎This product is not designed for normal operation with in a radioactive environment.

○ Package



Plastic Mold

(UNIT : mm)

Fig.1

○ Block Diagram

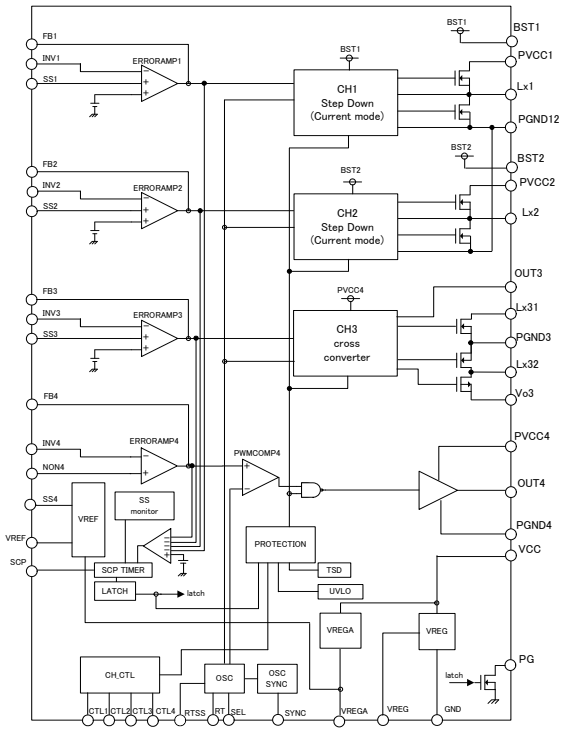


Fig.2

○ Pin Description

Pin No.	Pin Name	Input /Output	Pin Descriptions	Memo
29	VCC	–	Input Supply Voltage	Active over 4.0V
35,40,11	PVCC1,2,4	–	Power Supply for CH1,2,4 output circuit	Active over 4.0V
37,38,6,9	PGND12,3,4	–	Ground Pin for CH1～4 Output	
31	GND	–	Ground terminal	
42	VREG	O	Regulator Output for Boost terminal	5.0V Output
30	VREGA	O	VREGA output	2.5V Output
4,10	OUT3,OUT4	O	Terminal for connecting gate of OUT3, OUT4 PMOS	
12	VREF	O	Reference output voltage	1.0V Output
8	Vo3	O	CH3 Output Voltage	
36,39	Lx1,2	O	Pin for Connecting to Inductor	
5	Lx31	O	Pin for Connecting to Inductor	CH3 input
7	Lx32	O	Pin for Connecting to Inductor	CH3 output
27,24,18,15	INV1,2,3,4	I	CH1～4 Error Amplifier Negative Input Pin	
14	NON4	I	Error AMP non inverted input	CH4 only
28,25,19,16	FB1,2,3,4,	O	CH1～4. Error Amplifier Output Pin	
3	SYNC	I	Synchronous Rectification Timing Adjust Pin	
21	RT	–	For connecting a register to set the OSC freqency	0.5V Output
33	SEL	I	Oscillator Frequency Cotrol Pin	SEL=VREGA ・・・1/2fosc(CH4)
20	SCP	–	For connecting a capacitor to set up the delay time of the SCP	Charge until 0.5V with 5uA
43,44,1,2	CTL1,2,3,4	I	CH1～CH4 ON/OFF Control Pin	CTL=L Standby
32	PG	O	Power Good Output terminal	Low output at only abnormally state
26,23,19,16	SS1,2,3,4	I	SS Delay Time Setting Pin	Charge until 0.8V or 1.0V with 2uA
34,41	BST1,2	I	For Highside Driver supply voltage Pin	Lx+VREG Voltage
22	RTSS	I	Oscillator Frequency Adjustment Pin with external resistor	

Fig.3

○Operation Notes

1.) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC deterioration or damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

2.) GND potential

Ensure a minimum GND pin potential in all operating conditions. In addition, ensure that no pins other than the GND pin carry a voltage lower than or equal to the GND pin(except INV4 terminal), including during actual transient phenomena.

3.) Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4.) Inter-pin shorts and mounting errors

Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pin caused by the presence of a foreign object may result in damage to the IC.

5.) Operation in a strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

6.) Common impedance

Power supply and ground wiring should reflect consideration of the need to lower common impedance and minimize ripple as much as possible (by making wiring as short and thick as possible or rejecting ripple by incorporating inductance and capacitance).

7.) Voltage of CTL pin

The threshold voltages of CTL pin are 0.8V and 2.0V. STB state is set below 0.8V while action state is set beyond 2.0V.
The region between 0.8V and 2.0V is not recommended and may cause improper operation.
The rise and fall time must be under 10msec. In case to put capacitor to STB pin, it is recommended to use under 0.01μF.

8.) Thermal shutdown circuit (TSD circuit)

This IC incorporates a built-in thermal shutdown circuit (TSD circuit). The TSD circuit is designed only to shut the IC off to prevent runaway thermal operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of the thermal shutdown circuit is assumed.

9.) IC pin input

This monolithic IC contains P+ isolation and PCB layers between adjacent elements in order to keep them isolated.
P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements.
For example, when a resistor and transistor are connected to pins as shown in following chart,

- ○ the P/N junction functions as a parasitic diode when GND > (Pin A) for the resistor or GND > (Pin B) for the transistor (NPN).
- ○ Similarly, when GND > (Pin B) for the transistor (NPN), the parasitic diode described above combines with the N layer of other adjacent elements to operate as a parasitic NPN transistor.

The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements, such as by the application of voltages lower than the GND (PCB) voltage to input and output pins.

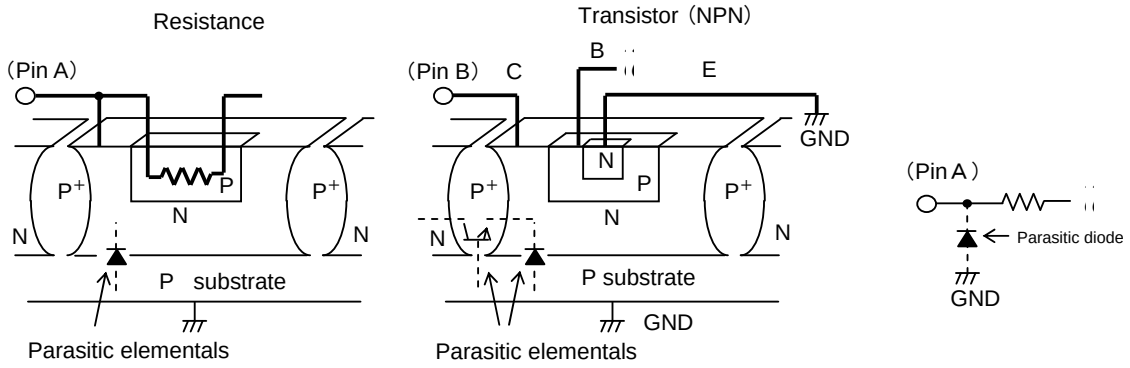


Fig.4 Simplified structure of a Bipolar IC

Notes

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