

### n FEATURES

- Ψ Wide  $V_{CC}$  low operation voltage : 1.65V ~ 3.6V
- Ψ Ultra low power consumption :
  - $V_{CC} = 3.6V$     Operation current : 12mA (Max.) at 55ns  
2mA (Max.) at 1MHz
  - Standby current : 2.5uA (Typ.) at 3.0V/25°C
  - $V_{CC} = 1.2V$     Data retention current : 1.2uA (Typ.) at 25°C
- Ψ High speed access time :
  - 55            55ns (Max.) at  $V_{CC}=1.65\sim 3.6V$
  - 70            70ns (Max.) at  $V_{CC}=1.65\sim 3.6V$
- Ψ Automatic power down when chip is deselected
- Ψ Easy expansion with  $\overline{CE1}$ , CE2 and  $\overline{OE}$  options
- Ψ I/O Configuration x8/x16 selectable by  $\overline{LB}$  and  $\overline{UB}$  pin.
- Ψ Three state outputs and TTL compatible
- Ψ Fully static operation, no clock, no refresh
- Ψ Data retention supply voltage as low as 1.0V

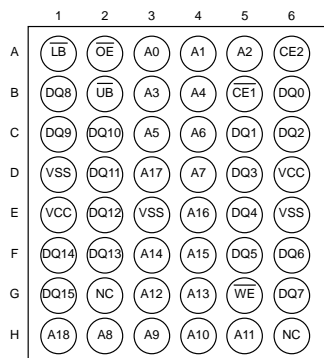
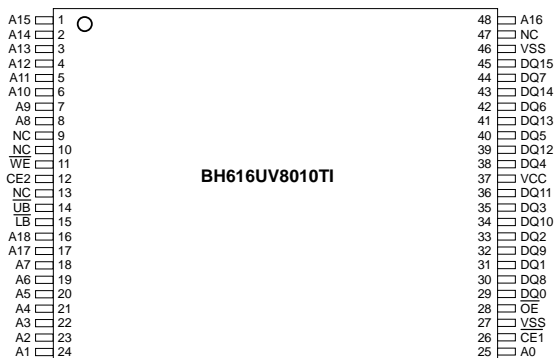
### n DESCRIPTION

The BH616UV8010 is a high performance, ultra low power CMOS Static Random Access Memory organized as 524,288 by 16 bits and operates in a wide range of 1.65V to 3.6V supply voltage. Advanced CMOS technology and circuit techniques provide both high speed and low power features with typical operating current of 1.5mA at 1MHz at 3.6V/25°C and maximum access time of 55ns at 1.65V/85°C. Easy memory expansion is provided by an active LOW chip enable ( $\overline{CE1}$ ), an active HIGH chip enable (CE2) and active LOW output enable ( $\overline{OE}$ ) and three-state output drivers. The BH616UV8010 has an automatic power down feature, reducing the power consumption significantly when chip is deselected. The BH616UV8010 is available in DICE form, JEDEC standard 48-pin TSOP-I and 48-ball BGA package.

### n POWER CONSUMPTION

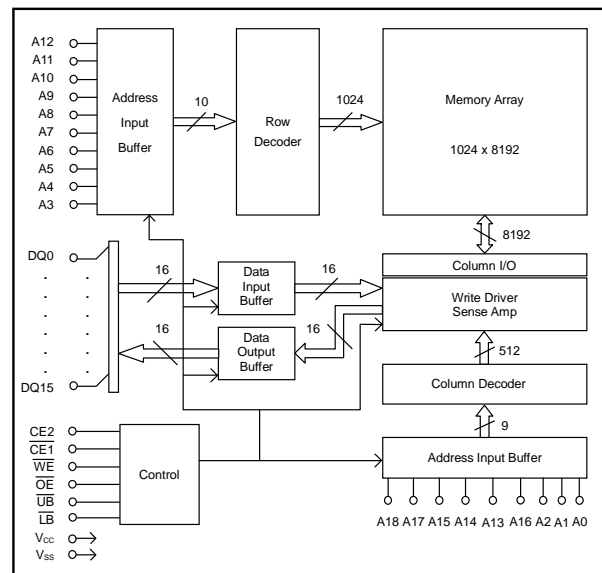
PRODUCT FAMILY	OPERATING TEMPERATURE	POWER DISSIPATION								PKG TYPE
		STANDBY ( $I_{CCSB1, Max}$ )		Operating ( $I_{CC, Max}$ )						
		$V_{CC}=3.6V$	$V_{CC}=1.8V$	$V_{CC}=3.6V$			$V_{CC}=1.8V$			
				1MHz	10MHz	$f_{Max}$	1MHz	10MHz	$f_{Max}$	
BH616UV8010DI	Industrial -40°C to +85°C	15uA	12uA	2mA	6mA	12mA	1.5mA	5mA	8mA	DICE
BH616UV8010AI										BGA-48-0608
BH616UV8010TI										TSOP I-48

### n PIN CONFIGURATIONS



48-ball BGA top view

### n BLOCK DIAGRAM



**Brilliance Semiconductor, Inc.** reserves the right to change products and specifications without notice. Detailed product characteristic test report is available upon request and being accepted.

**n PIN DESCRIPTIONS**

Name	Function
<b>A0-A18 Address Input</b>	These 19 address inputs select one of the 524,288 x 16 bit in the RAM
<b>CE1 Chip Enable 1 Input CE2 Chip Enable 2 Input</b>	CE1 is active LOW and CE2 is active HIGH. Both chip enables must be active when data read from or write to the device. If either chip enable is not active, the device is deselected and is in standby power mode. The DQ pins will be in the high impedance state when the device is deselected.
<b>WE Write Enable Input</b>	The write enable input is active LOW and controls read and write operations. With the chip selected, when WE is HIGH and OE is LOW, output data will be present on the DQ pins; when WE is LOW, the data present on the DQ pins will be written into the selected memory location.
<b>OE Output Enable Input</b>	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when OE is inactive.
<b>LB and UB Data Byte Control Input</b>	Lower byte and upper byte data input/output control pins.
<b>DQ0-DQ15 Data Input/Output Ports</b>	16 bi-directional ports are used to read data from or write data into the RAM.
<b>V<sub>CC</sub></b>	Power Supply
<b>V<sub>SS</sub></b>	Ground

**n TRUTH TABLE**

MODE	CE1	CE2	WE	OE	LB	UB	DQ0~DQ7	DQ8~DQ15	V <sub>CC</sub> CURRENT
Chip De-selected (Power Down)	H	X	X	X	X	X	High Z	High Z	I <sub>CCSB</sub> , I <sub>CCSB1</sub>
	X	L	X	X	X	X	High Z	High Z	I <sub>CCSB</sub> , I <sub>CCSB1</sub>
	X	X	X	X	H	H	High Z	High Z	I <sub>CCSB</sub> , I <sub>CCSB1</sub>
Output Disabled	L	H	H	H	L	X	High Z	High Z	I <sub>CC</sub>
	L	H	H	H	X	L	High Z	High Z	I <sub>CC</sub>
Read	L	H	H	L	L	L	D <sub>OUT</sub>	D <sub>OUT</sub>	I <sub>CC</sub>
					H	L	High Z	D <sub>OUT</sub>	I <sub>CC</sub>
					L	H	D <sub>OUT</sub>	High Z	I <sub>CC</sub>
Write	L	H	L	X	L	L	D <sub>IN</sub>	D <sub>IN</sub>	I <sub>CC</sub>
					H	L	X	D <sub>IN</sub>	I <sub>CC</sub>
					L	H	D <sub>IN</sub>	X	I <sub>CC</sub>

NOTES: H means V<sub>IH</sub>; L means V<sub>IL</sub>; X means don't care (Must be V<sub>IH</sub> or V<sub>IL</sub> state)

**n ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>**

SYMBOL	PARAMETER	RATING	UNITS
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 <sup>(2)</sup> to 4.6V	V
T <sub>BIAS</sub>	Temperature Under Bias	-40 to +125	°C
T <sub>STG</sub>	Storage Temperature	-60 to +150	°C
P <sub>T</sub>	Power Dissipation	1.0	W
I <sub>OUT</sub>	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. -2.0V in case of AC pulse width less than 30 ns

**n OPERATING RANGE**

RANG	AMBIENT TEMPERATURE	V <sub>CC</sub>
Industrial	-40°C to + 85°C	1.65V ~ 3.6V

**n CAPACITANCE <sup>(1)</sup> (T<sub>A</sub> = 25°C, f = 1.0MHz)**

SYMBOL	PAMAMETER	CONDITIONS	MAX.	UNITS
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	pF
C <sub>IO</sub>	Input/Output Capacitance	V <sub>IO</sub> = 0V	8	pF

1. This parameter is guaranteed and not 100% tested.

**n DC ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = -40°C to +85°C)**

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MIN.	TYP. <sup>(1)</sup>	MAX.	UNITS	
V <sub>CC</sub>	Power Supply		1.65	--	3.6	V	
V <sub>IL</sub>	Input Low Voltage	V <sub>CC</sub> =1.8V V <sub>CC</sub> =3.6V	-0.3 <sup>(2)</sup>	--	0.4 0.6	V	
V <sub>IH</sub>	Input High Voltage	V <sub>CC</sub> =1.8V V <sub>CC</sub> =3.6V	1.4 2.2	--	V <sub>CC</sub> +0.3 <sup>(3)</sup>	V	
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> = 0V to V <sub>CC</sub> , CE1 = V <sub>IH</sub> or CE2 = V <sub>IL</sub>	--	--	1	uA	
I <sub>LO</sub>	Output Leakage Current	V <sub>IO</sub> = 0V to V <sub>CC</sub> , CE1 = V <sub>IH</sub> or CE2 = V <sub>IL</sub> or OE = V <sub>IH</sub> or UB = LB = V <sub>IH</sub>	--	--	1	uA	
V <sub>OL</sub>	Output Low Voltage	V <sub>CC</sub> = Max, I <sub>OL</sub> = 0.2mA V <sub>CC</sub> = Max, I <sub>OL</sub> = 2.0mA	V <sub>CC</sub> =1.8V V <sub>CC</sub> =3.6V	--	0.2 0.4	V	
V <sub>OH</sub>	Output High Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = -0.1mA V <sub>CC</sub> = Min, I <sub>OH</sub> = -1.0mA	V <sub>CC</sub> =1.8V V <sub>CC</sub> =3.6V	V <sub>CC</sub> -0.2 2.4	--	V	
I <sub>CC</sub>	Operating Power Supply Current	CE1 = V <sub>IL</sub> and CE2 = V <sub>IH</sub> , I <sub>DD</sub> = 0mA, f = F <sub>MAX</sub> <sup>(4)</sup>	V <sub>CC</sub> =1.8V V <sub>CC</sub> =3.6V	--	6 8	12	mA
I <sub>CC1</sub>	Operating Power Supply Current	CE1 = V <sub>IL</sub> and CE2 = V <sub>IH</sub> , I <sub>DD</sub> = 0mA, f = 1MHz	V <sub>CC</sub> =1.8V V <sub>CC</sub> =3.6V	--	1.0 1.5	2.0	mA
I <sub>CCSB</sub>	Standby Current – TTL	CE1 = V <sub>IH</sub> , or CE2 = V <sub>IL</sub> , I <sub>DD</sub> = 0mA	V <sub>CC</sub> =1.8V V <sub>CC</sub> =3.6V	--	--	0.5 1.0	mA
I <sub>CCSB1</sub>	Standby Current – CMOS	CE1 ≥ V <sub>CC</sub> -0.2V or CE2 ≤ 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> -0.2V or V <sub>IN</sub> ≤ 0.2V	V <sub>CC</sub> =1.8V V <sub>CC</sub> =3.6V	--	2.0 2.5 <sup>(5)</sup>	12 15	uA

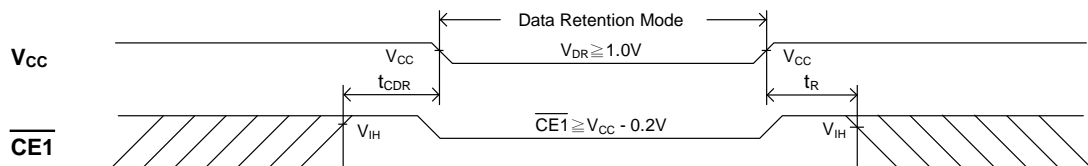
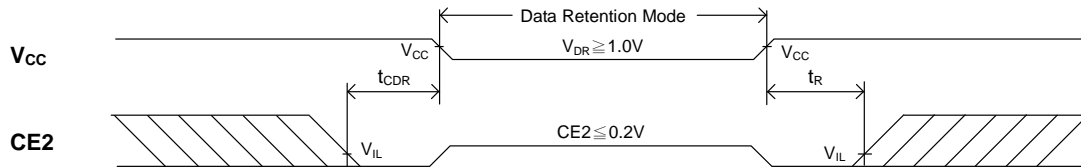
1. Typical characteristics are at T<sub>A</sub>=25°C and not 100% tested.
2. Undershoot: -1.0V in case of pulse width less than 20 ns.
3. Overshoot: V<sub>CC</sub>+1.0V in case of pulse width less than 20 ns.
4. F<sub>MAX</sub>=1/t<sub>RC</sub>.
5. V<sub>CC</sub>=3.0V

**n DATA RETENTION CHARACTERISTICS (T<sub>A</sub> = -40°C to +85°C)**

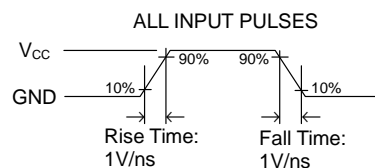
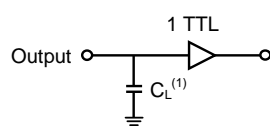
SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP. <sup>(1)</sup>	MAX.	UNITS
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention	CE1 ≥ V <sub>CC</sub> -0.2V or CE2 ≤ 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> -0.2V or V <sub>IN</sub> ≤ 0.2V	1.0	--	--	V
I <sub>CCDR</sub>	Data Retention Current	CE1 ≥ V <sub>CC</sub> -0.2V or CE2 ≤ 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> -0.2V or V <sub>IN</sub> ≤ 0.2V	--	1.2	7.0	uA
t <sub>CDR</sub>	Chip Deselect to Data Retention Time	See Retention Waveform	0	--	--	ns
t <sub>R</sub>	Operation Recovery Time		t <sub>RC</sub> <sup>(2)</sup>	--	--	ns

1. Typical characteristics are at T<sub>A</sub>=25°C and not 100% tested.

2. t<sub>RC</sub> = Read Cycle Time.



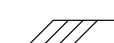


**n LOW V<sub>CC</sub> DATA RETENTION WAVEFORM (1) (CE1 Controlled)**

**n LOW V<sub>CC</sub> DATA RETENTION WAVEFORM (2) (CE2 Controlled)**

**n AC TEST CONDITIONS  
(Test Load and Input/Output Reference)**

Input Pulse Levels	V <sub>CC</sub> / 0V
Input Rise and Fall Times	1V/ns
Input and Output Timing Reference Level	0.5V <sub>CC</sub>
Output Load	t <sub>CLZ1</sub> , t <sub>CLZ2</sub> , t <sub>BE</sub> , t <sub>OLZ</sub> , t <sub>CHZ1</sub> , t <sub>CHZ2</sub> , t <sub>BDO</sub> , t <sub>OHZ</sub> , t <sub>WHZ</sub> , t <sub>OW</sub>
	Others



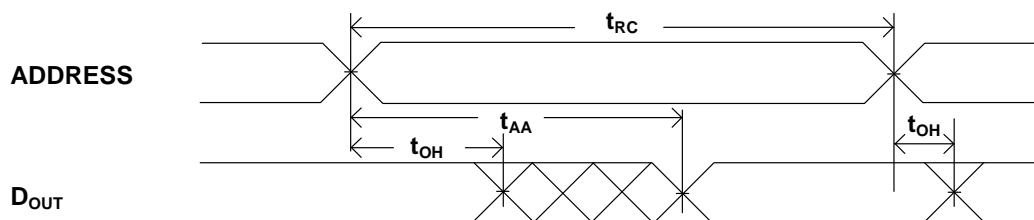
1. Including jig and scope capacitance.

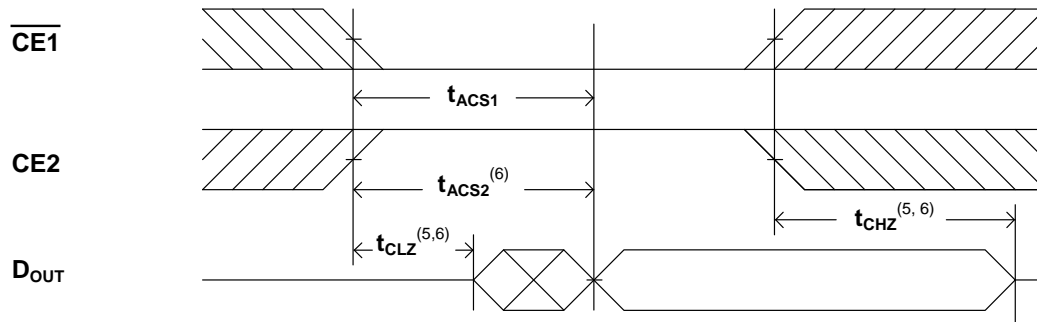
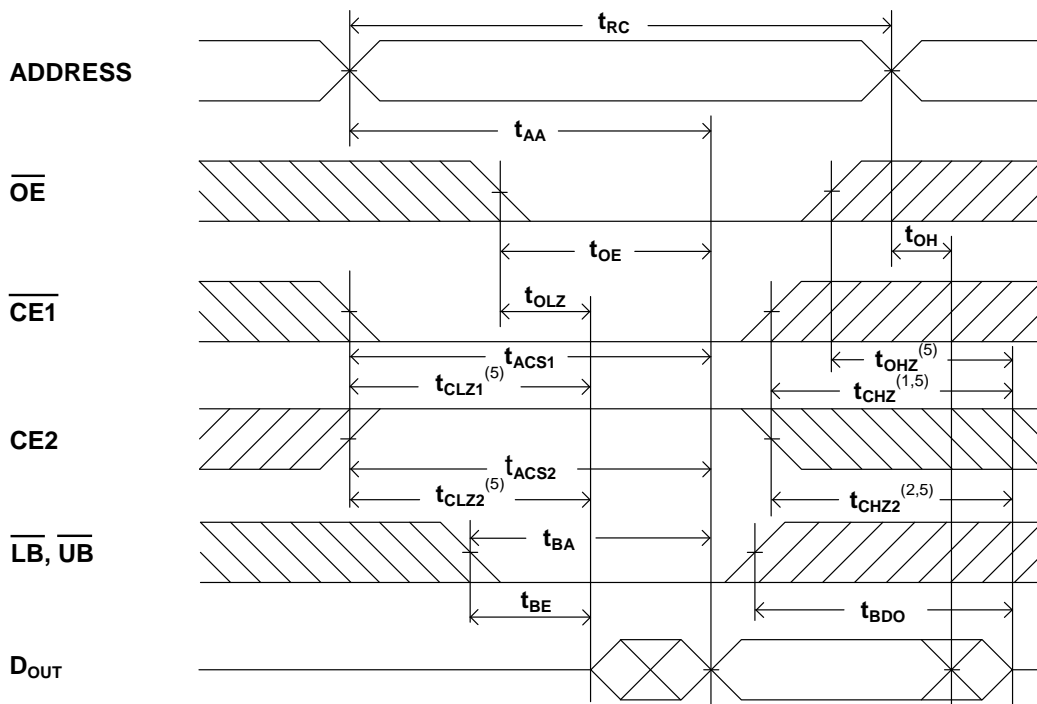
**n KEY TO SWITCHING WAVEFORMS**

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM "H" TO "L"	WILL BE CHANGE FROM "H" TO "L"
	MAY CHANGE FROM "L" TO "H"	WILL BE CHANGE FROM "L" TO "H"
	DON'T CARE ANY CHANGE PERMITTED	CHANGE : STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

**n AC ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = -40°C to +85°C)**
**READ CYCLE**

JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	CYCLE TIME : 55ns			CYCLE TIME : 70ns			UNITS
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
t <sub>AVAX</sub>	t <sub>RC</sub>	Read Cycle Time	55	--	--	70	--	--	ns
t <sub>AVQX</sub>	t <sub>AA</sub>	Address Access Time	--	--	55	--	--	70	ns
t <sub>E1LQV</sub>	t <sub>ACS1</sub>	Chip Select Access Time (CE1)	--	--	55	--	--	70	ns
t <sub>E2LQV</sub>	t <sub>ACS2</sub>	Chip Select Access Time (CE2)	--	--	55	--	--	70	ns
t <sub>BLQV</sub>	t <sub>BA</sub>	Data Byte Control Access Time (LB, UB)	--	--	55	--	--	70	ns
t <sub>GLQV</sub>	t <sub>OE</sub>	Output Enable to Output Valid	--	--	30	--	--	35	ns
t <sub>E1LQX</sub>	t <sub>CLZ1</sub>	Chip Select to Output Low Z (CE1)	10	--	--	10	--	--	ns
t <sub>E2LQX</sub>	t <sub>CLZ2</sub>	Chip Select to Output Low Z (CE2)	10	--	--	10	--	--	ns
t <sub>BLQX</sub>	t <sub>BE</sub>	Data Byte Control to Output Low Z (LB, UB)	10	--	--	10	--	--	ns
t <sub>GLQX</sub>	t <sub>OLZ</sub>	Output Enable to Output Low Z	5	--	--	5	--	--	ns
t <sub>E1HQZ</sub>	t <sub>CHZ1</sub>	Chip Select to Output High Z (CE1)	--	--	25	--	--	30	ns
t <sub>E2HQZ</sub>	t <sub>CHZ2</sub>	Chip Select to Output High Z (CE2)	--	--	25	--	--	30	ns
t <sub>BHQZ</sub>	t <sub>BDO</sub>	Data Byte Control to Output High Z (LB, UB)	--	--	25	--	--	30	ns
t <sub>GHQZ</sub>	t <sub>OHZ</sub>	Output Enable to Output High Z	--	--	25	--	--	30	ns
t <sub>AVQX</sub>	t <sub>OH</sub>	Data Hold from Address Change	10	--	--	10	--	--	ns

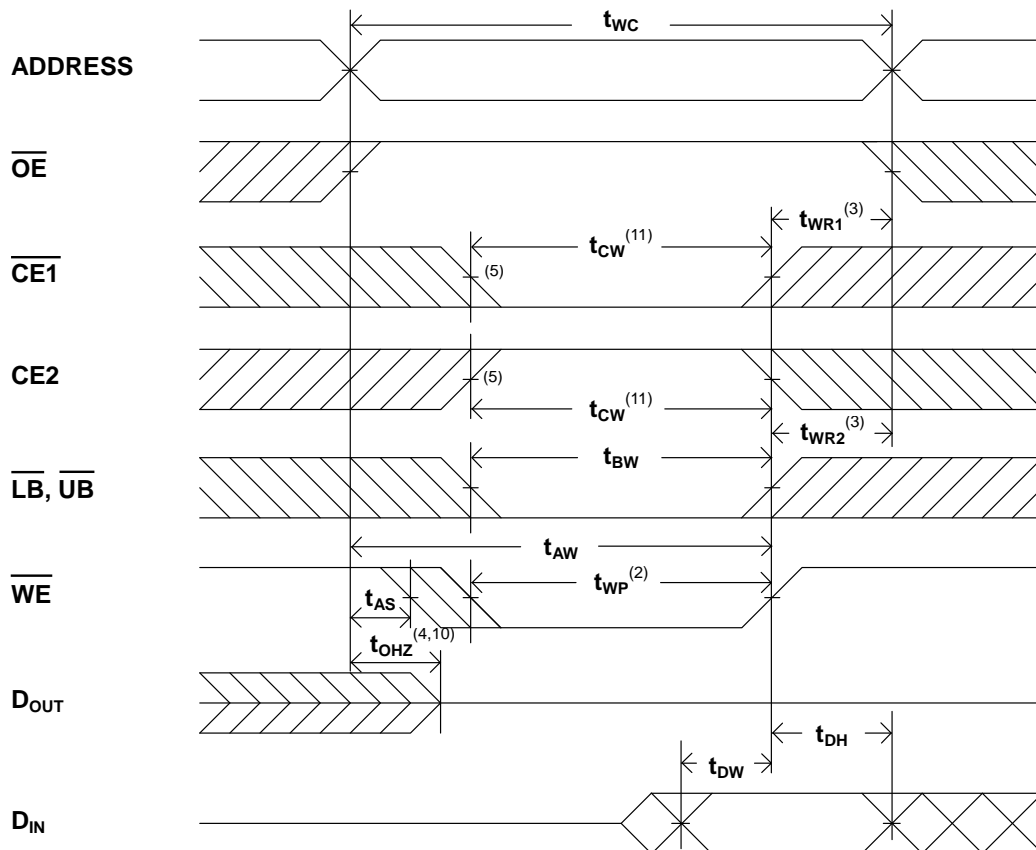
**n SWITCHING WAVEFORMS (READ CYCLE)**
**READ CYCLE 1<sup>(1,2,4)</sup>**


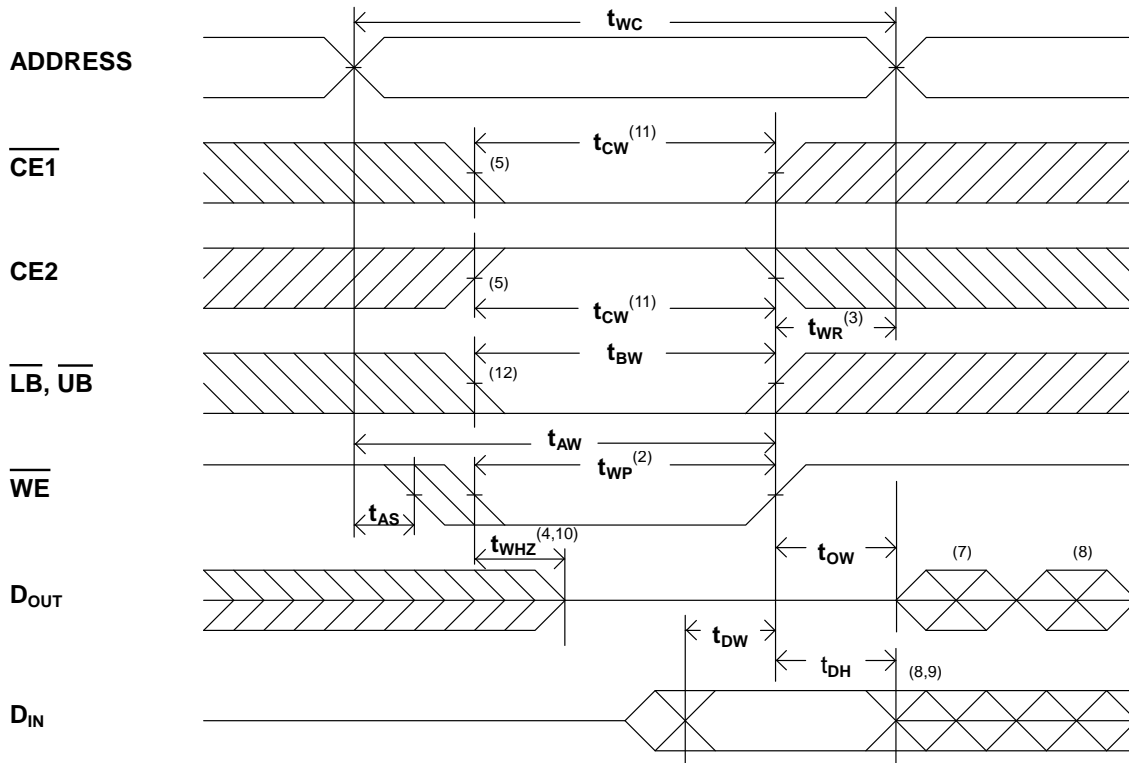
**READ CYCLE 2** <sup>(1,3,4)</sup>

**READ CYCLE 3** <sup>(1,4)</sup>

**NOTES:**

1.  $\overline{WE}$  is high in read Cycle.
2. Device is continuously selected when  $\overline{CE1} = V_{IL}$  and  $CE2 = V_{IH}$ .
3. Address valid prior to or coincident with  $\overline{CE1}$  transition low and/or  $CE2$  transition high.
4.  $\overline{OE} = V_{IL}$ .
5. Transition is measured  $\pm 500\text{mV}$  from steady state with  $C_L = 5\text{pF}$ .  
The parameter is guaranteed but not 100% tested.

**n AC ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = -40°C to +85°C)  
WRITE CYCLE**

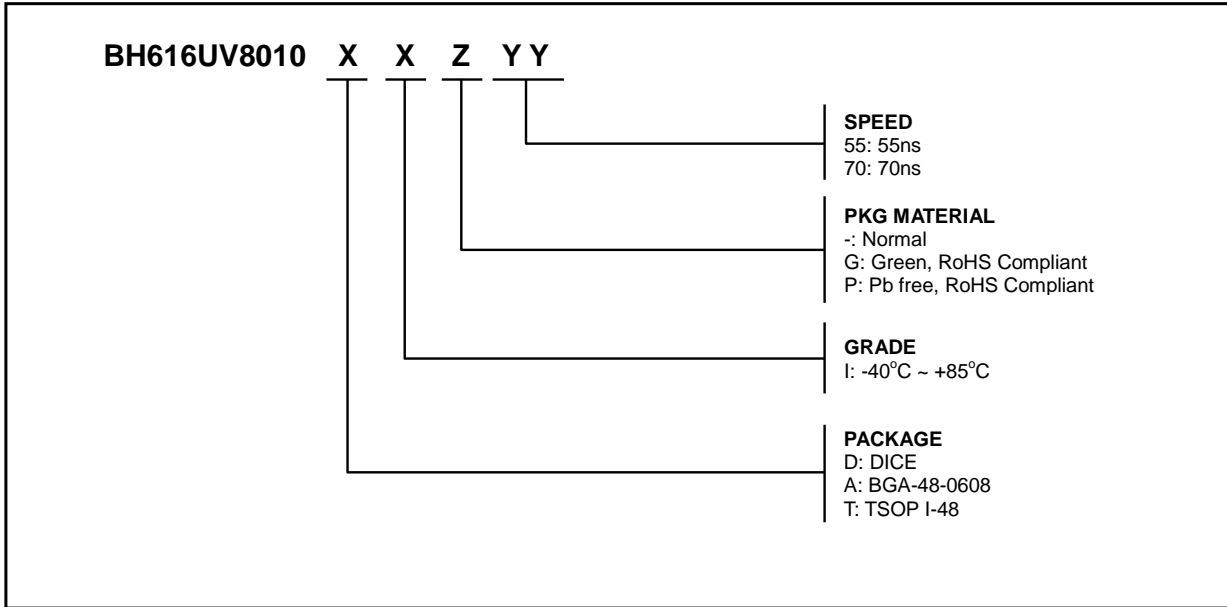
JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	CYCLE TIME : 55ns			CYCLE TIME : 70ns			UNITS
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
t <sub>AVAX</sub>	t <sub>wc</sub>	Write Cycle Time	55	--	--	70	--	--	ns
t <sub>AVWL</sub>	t <sub>AS</sub>	Address Set up Time	0	--	--	0	--	--	ns
t <sub>AVWH</sub>	t <sub>AW</sub>	Address Valid to End of Write	45	--	--	60	--	--	ns
t <sub>ELWH</sub>	t <sub>cw</sub>	Chip Select to End of Write	45	--	--	60	--	--	ns
t <sub>BLWH</sub>	t <sub>BW</sub>	Data Byte Control to End of Write (LB, UB)	45	--	--	60	--	--	ns
t <sub>WLWH</sub>	t <sub>WP</sub>	Write Pulse Width	35	--	--	35	--	--	ns
t <sub>WHAX</sub>	t <sub>WR1</sub>	Write Recovery Time (CE1, WE)	0	--	--	0	--	--	ns
t <sub>E2LAX</sub>	t <sub>WR2</sub>	Write Recovery Time (CE2)	0	--	--	0	--	--	ns
t <sub>WLQZ</sub>	t <sub>WHZ</sub>	Write to Output High Z	--	--	20	--	--	25	ns
t <sub>DVWH</sub>	t <sub>DW</sub>	Data to Write Time Overlap	25	--	--	30	--	--	ns
t <sub>WHDX</sub>	t <sub>DH</sub>	Data Hold from Write Time	0	--	--	0	--	--	ns
t <sub>GHQZ</sub>	t <sub>OHZ</sub>	Output Disable to Output in High Z	--	--	25	--	--	30	ns
t <sub>WHQX</sub>	t <sub>OW</sub>	End of Write to Output Active	5	--	--	5	--	--	ns

**n SWITCHING WAVEFORMS (WRITE CYCLE)**
**WRITE CYCLE 1<sup>(1)</sup>**


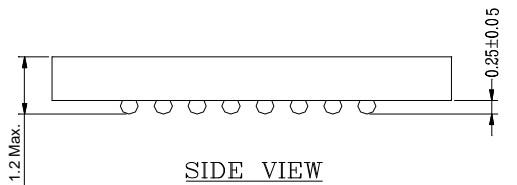
**WRITE CYCLE 2** <sup>(1,6)</sup>

**NOTES:**

1.  $\overline{WE}$  must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of  $\overline{CE1}$  and CE2 active and  $\overline{WE}$  low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3.  $t_{WR}$  is measured from the earlier of  $\overline{CE1}$  or  $\overline{WE}$  going high or CE2 going low at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the  $\overline{CE1}$  low transition or the CE2 high transition occurs simultaneously with the  $\overline{WE}$  low transitions or after the  $\overline{WE}$  transition, output remain in a high impedance state.
6.  $\overline{OE}$  is continuously low ( $\overline{OE} = V_{IL}$ ).
7.  $D_{OUT}$  is the same phase of write data of this write cycle.
8.  $D_{OUT}$  is the read data of next address.
9. If CE1 is low and CE2 is high during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured  $\pm 500\text{mV}$  from steady state with  $C_L = 5\text{pF}$ .  
The parameter is guaranteed but not 100% tested.
11.  $t_{CW}$  is measured from the later of CE1 going low or CE2 going high to the end of write.



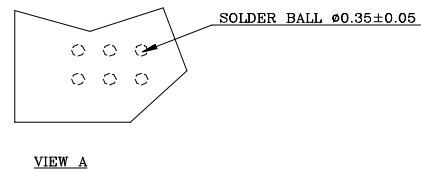
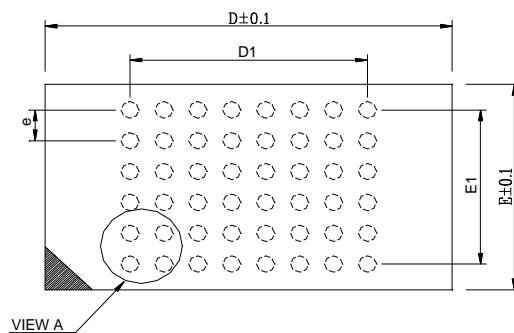
**n ORDERING INFORMATION**

**Note:**

Brilliance Semiconductor Inc. (BSI) assumes no responsibility for the application or use of any product or circuit described herein. BSI does not authorize its products for use as critical components in any application in which the failure of the BSI product may be expected to result in significant injury or death, including life-support systems and critical medical instruments.

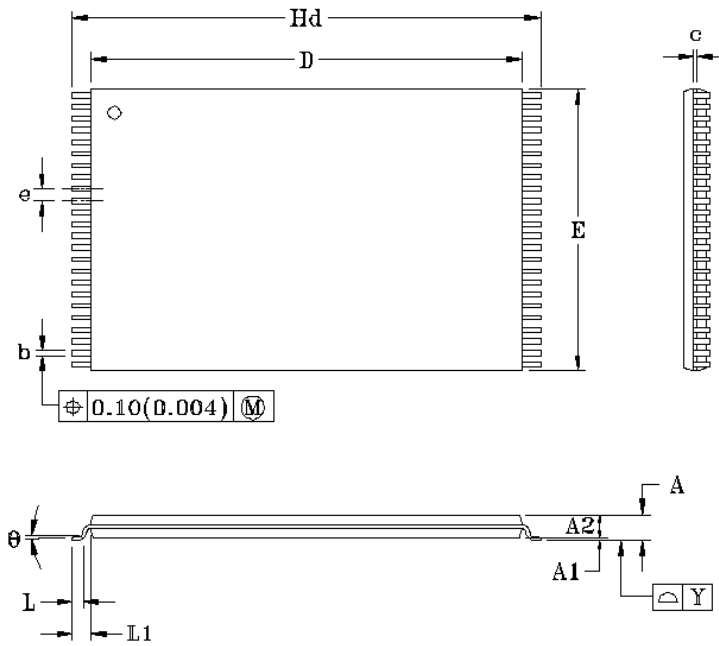
**n PACKAGE DIMENSIONS**

**NOTES:**

- 1: CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
- 2: PIN#1 DOT MARKING BY LASER OR PAD PRINT.
- 3: SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.

BALL PITCH e = 0.75				
D	E	N	D1	E1
8.0	6.0	48	5.25	3.75



**48 mini-BGA (6 x 8)**

**n PACKAGE DIMENSIONS**


SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.20			0.047
A1	0.05		0.15	0.002		0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.17	0.20	0.23	0.007	0.008	0.009
c	0.10	0.125	0.18	0.004	0.005	0.008
D	18.30	18.40	18.50	0.720	0.724	0.728
E	11.90	12.00	12.10	0.468	0.472	0.476
Hd	19.80	20.00	20.20	0.780	0.787	0.795
e		0.50			0.020	
L	0.40	0.50	0.60	0.016	0.020	0.024
L1		0.80			0.031	
Y	0.00		0.10	0.000		0.004
θ	1°	3°	5°	1°	3°	5°

*TSOP I-48 Pin (12mm x 20mm)*

**n Revision History**

<u>Revision No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
1.0	Initial Production Version	July 15,2005	Initial
1.1	To improve access speed - from 70ns to 55ns	Dec. 23, 2005	
1.2	Change I-grade operation temperature range - from -25°C to -40°C	May. 25, 2006	