DATA SHEET

TDA3681

Multiple voltage regulator with switch and ignition buffer

Product specification
Supersedes data of 2002 Apr 10

2004 Mar 31

Philips
Semiconductors

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FEATURES

General

- Extremely low noise behaviour and good stability with very small output capacitors
- Second supply pin for regulators 3 and 4 to reduce power dissipation (e.g. via a DC-to-DC converter)
- Three V_P-state controlled regulators (regulators 1, 3 and 4) and a power switch
- Regulator 2, reset and ignition buffer operational during load dump and thermal shutdown
- Combined control pin for switching regulators 1 and 3
- Separate control pins for switching regulator 4 and the power switch
- Supply voltage range from –18 to +50 V
- Low quiescent current in standby mode (when regulators 1, 3 and 4 and power switch are switched off and ignition input is low)
- Hold output (open-collector output stage) for low V_P (regulators 1, 3 and 4 and power switch off)
- Hold output when one of regulators 1 and 3 and/or 4 is out of regulation
- Hold output for foldback mode of power switch and regulators 1, 3 and 4
- Hold output for load dump and temperature protection
- Reset (push-pull output stage) for regulator 2
- Adjustable reset delay time
- High supply voltage ripple rejection
- Backup capacitor for regulator 2
- One independent ignition buffer (active HIGH).

Protections

- Reverse polarity safe (down to –18 V without high reverse current)
- Able to withstand voltages up to 18 V at the outputs (supply line may be short-circuited)
- ESD protection on all pins
- Thermal protections
- Load dump protection
- Foldback current limit protection for regulators 1, 2, 3 and 4
- Delayed second current limit protection for the power switch (at short-circuit)
- The regulator outputs and the power switch are DC short-circuit safe to ground and supply (V_P).

GENERAL DESCRIPTION

The TDA3681 is a multiple output voltage regulator with a power switch and an ignition buffer. It is intended for use in car radios with or without a microcontroller. The TDA3681 contains the following:

- Four fixed voltage regulators with a foldback current protection (regulators 1, 2, 3 and 4). Regulator 2, which is intended to supply a microcontroller, also operates during load dump and thermal shutdown
- Regulators 3 and 4 have a second supply pin that can be connected to a lower supply voltage (>6.5 V) to reduce the power dissipation
- A power switch with protection, operated by a control input
- Reset and hold outputs that can be used to interface with the microcontroller; the reset signal can be used to call up the microcontroller
- Both supply pins can withstand load dump pulses and negative supply voltages
- Regulator 2, which is in regulation at a backup voltage above 6.5 V
- A provision for the use of a reserve supply capacitor that will hold enough energy for regulator 2 (5 V continuous) to allow a microcontroller to prepare for loss of voltage
- An ignition input Schmitt trigger with push-pull output stage.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA3681J	DBS17P	plastic DIL-bent-SIL power package; 17 leads (lead length 7.7 mm)	SOT243-3
TDA3681JR	DBS17P	plastic DIL-bent-SIL (special bent) power package; 17 leads (lead length 12 mm)	SOT475-1
TDA3681TH	HSOP20	plastic, heatsink small outline package; 20 leads; low stand-off height	SOT418-3

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{P1}	supply voltage 1					
	operating		9.5	14.4	18	V
	reverse polarity	non-operating	–	–	18	V
	regulator 2 on		4	14.4	50	V
	jump start	$t \leq 10$ minutes	–	–	30	V
	load dump protection	$t \leq 50$ ms; $t_r \geq 2.5$ ms	–	–	50	V
V_{P2}	supply voltage 2					
	operating		6.5	14.4	18	V
	reverse polarity	non-operating	–	–	18	V
	regulator 2 on		0	–	50	V
	jump start	$t \leq 10$ minutes	–	–	30	V
	load dump protection	$t \leq 50$ ms; $t_r \geq 2.5$ ms	–	–	50	V
$I_{q(tot)}$	total quiescent supply current	standby mode	–	110	150	μA
T_j	junction temperature		–	–	150	°C
Voltage regulators						
$V_{o(REG1)}$	output voltage of regulator 1	1 mA ≤ I_{REG1} ≤ 600 mA; V_P = 14.4 V	8.0	8.5	9.0	V
$V_{o(REG2)}$	output voltage of regulator 2	1 mA ≤ I_{REG2} ≤ 300 mA; V_P = 14.4 V	4.75	5.0	5.25	V
$V_{o(REG3)}$	output voltage of regulator 3	1 mA ≤ I_{REG3} ≤ 1400 mA; V_P = 14.4 V	4.75	5.0	5.25	V
$V_{o(REG4)}$	output voltage of regulator 4	1 mA ≤ I_{REG4} ≤ 1 A; V_P = 14.4 V	3.14	3.3	3.46	V
Power switch						
$V_{drop(SW)}$	drop-out voltage	I_{SW} = 1 A; V_{P1} = 13.5 V	–	0.45	0.65	V
		I_{SW} = 1.8 A; V_{P1} = 13.5 V	–	1.0	1.8	V
$I_{M(SW)}$	peak current		3	–	–	A

BLOCK DIAGRAMS

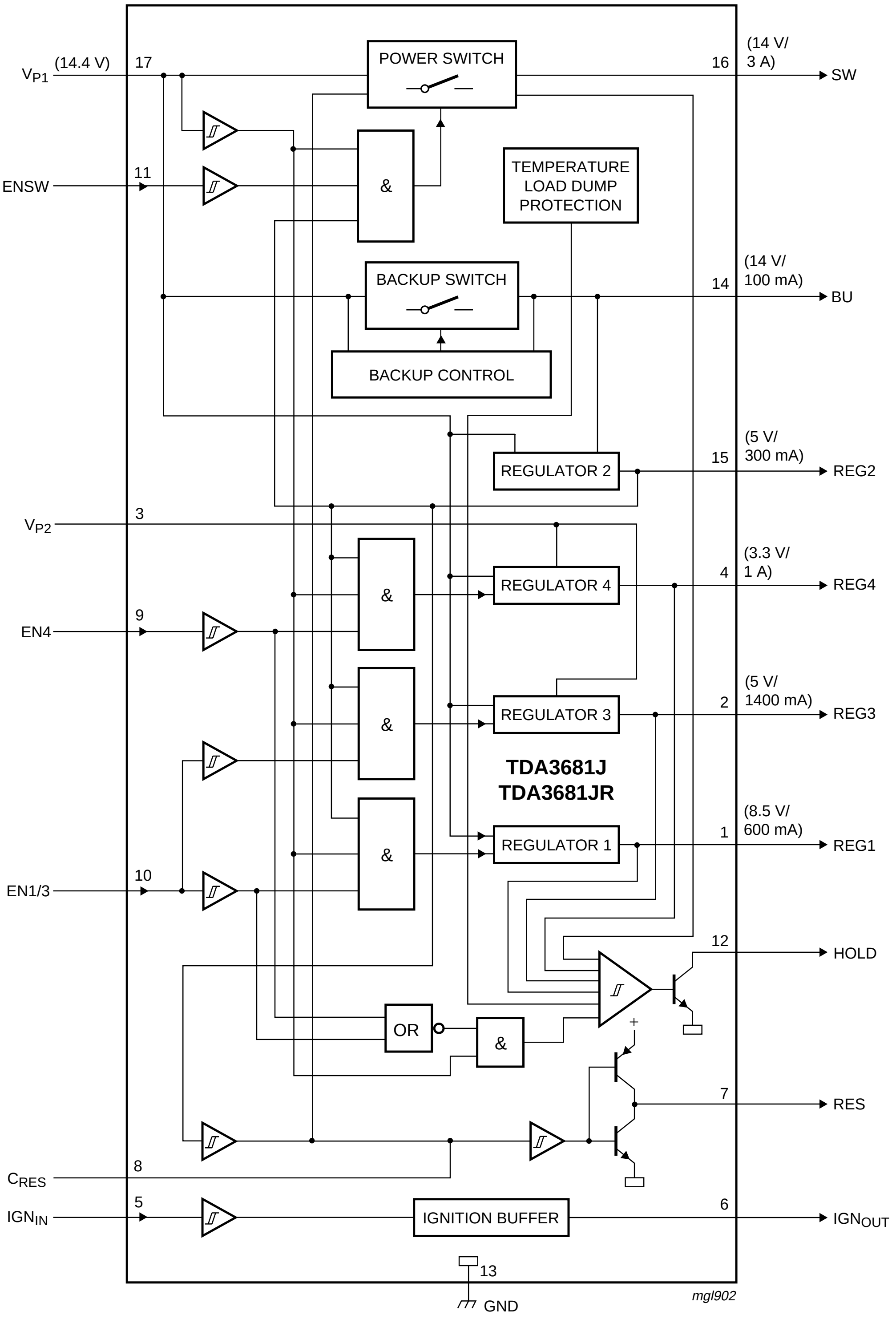


Fig.1 Block diagram of TDA3681J and TDA3681JR.

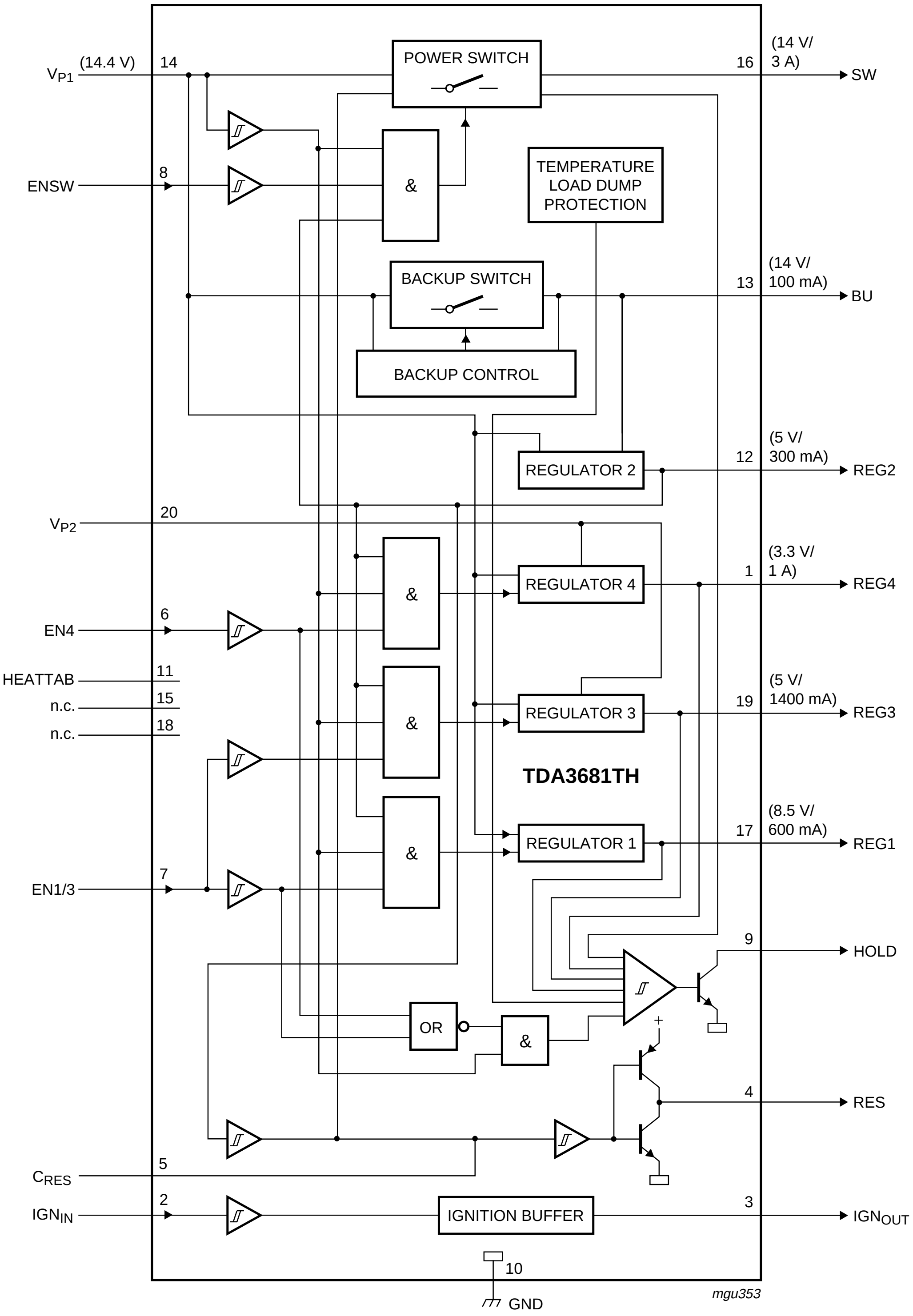


Fig.2 Block diagram of TDA3681TH.

PINNING

Pin description of TDA3681J and TDA3681JR

SYMBOL	PIN	DESCRIPTION
REG1	1	regulator 1 output
REG3	2	regulator 3 output
V_{P2}	3	second supply voltage
REG4	4	regulator 4 output
IGN_{IN}	5	ignition input
IGN_{OUT}	6	ignition output (active HIGH)
RES	7	reset output (active LOW)
C_{RES}	8	reset delay capacitor
EN4	9	enable input for regulator 4
EN1/3	10	enable input for regulators 1 and 3
ENSW	11	enable input for power switch
HOLD	12	hold output (active LOW)
GND	13	ground; note 1
BU	14	backup switch output
REG2	15	regulator 2 output
SW	16	power switch output
V_{P1}	17	supply voltage

Note

1. The heat tab is internally connected to pin GND.

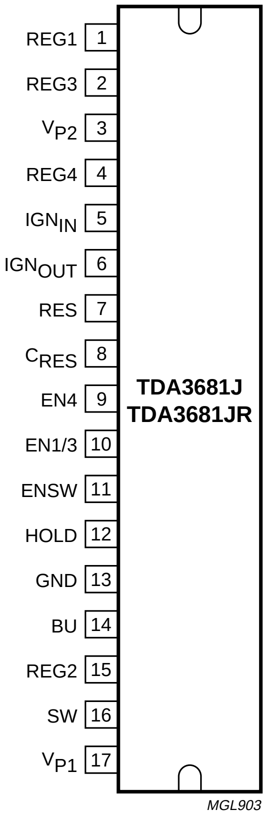


Fig.3 Pin configuration for TDA3681J and TDA3681JR.

Pin description of TDA3681TH

SYMBOL	PIN	DESCRIPTION
REG4	1	regulator 4 output
IGN_{IN}	2	ignition input
IGN_{OUT}	3	ignition output (active HIGH)
RES	4	reset output (active LOW)
C_{RES}	5	reset delay capacitor
EN4	6	enable input for regulator 4
EN1/3	7	enable input for regulators 1 and 3
ENSW	8	enable input for power switch
HOLD	9	hold output (active LOW)
GND	10	ground
HEATTAB	11	heat tab connection; note 1
REG2	12	regulator 2 output
BU	13	backup switch output
V_{P1}	14	supply voltage
n.c.	15	not connected
SW	16	power switch output
REG1	17	regulator 1 output
n.c.	18	not connected
REG3	19	regulator 3 output
V_{P2}	20	second supply voltage

Note

1. The pin is used for final test purposes. In the application it should be connected directly to ground.

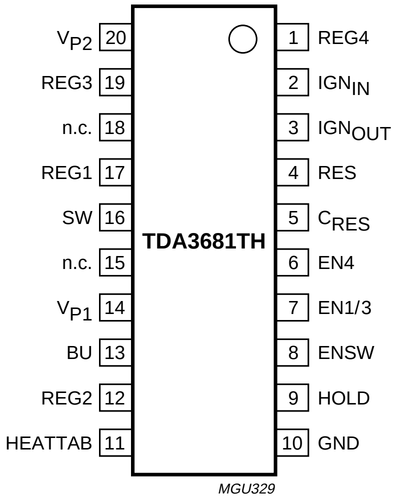


Fig.4 Pin configuration for TDA3681TH.

FUNCTIONAL DESCRIPTION

The TDA3681 is a multiple output voltage regulator with a power switch, intended for use in car radios with or without a microcontroller. Because of the low voltage operation of the car radio, low voltage drop regulators are used.

Regulator 2 is in regulation when the backup voltage exceeds 6.5 V for the first time. When regulator 2 is switched on and its output voltage is within its voltage range, the reset output is disabled to release the microcontroller. The reset delay time before release can be extended by an external capacitor (C_{RES}). This start-up feature is included to secure a smooth start-up of the microcontroller at first connection, without uncontrolled switching of regulator 2 during the start-up sequence.

The charge on the backup capacitor can be used to supply regulator 2 for a short period when the external supply voltage drops to 0 V (the time depends on the value of the backup capacitor).

The output stages of all switchable regulators have an extremely low noise behaviour and good stability, even for small values of the output capacitors.

When both regulator 2 and the supply voltages (V_{P1} and V_{P2} > 4.5 V) are available, regulators 1 and 3 can be operated by means of one enable input.

Regulator 4 and the power switch have a separate enable input.

Pin HOLD is normally HIGH but is active LOW. Pin HOLD is connected to an open-collector NPN transistor and must have an external pull-up resistor to operate. The hold output is controlled by a low voltage detection circuit which, when activated, pulls the hold output LOW (enabled). The hold outputs of the regulators are connected to an OR gate inside the IC so that the hold circuit is activated when one or more regulators (1, 3 or 4) are out of regulation for any reason. Each regulator enable input controls its own hold triggering circuit, so that if a regulator is disabled or switched off, the hold circuit for that regulator is disabled.

The hold circuit is also controlled by the temperature and load dump protection. Activating the temperature or load dump protection causes a hold (LOW) during the time that the protection is activated. When all regulators are switched off, the hold output is controlled by the battery line V_{P1}, temperature protection and load dump protection.

The hold circuit is enabled at low battery voltages. This indicates that it is not possible to get regulator 1 into regulation when switching it on: regulator 1 has the highest output voltage (8.5 V) of all switchable regulators. Therefore, regulator 1 is the most critical regulator with respect to an out of regulation condition caused by a low battery voltage.

The hold function includes hysteresis to avoid oscillations when the regulator voltage crosses the hold threshold level. The hold output also becomes active when the power switch is in foldback protection mode; see Fig.8. The block diagram of the hold function is illustrated in Fig.5.

All output pins are fully protected. The regulators are protected against load dump (regulators 1, 3 and 4 switch off at supply voltages >18 V) and short-circuit (foldback current protection).

The power switch contains a current protection. However, this protection is delayed at short-circuit by the reset delay capacitor (it should be noted that this is the second function of the reset delay capacitor C_{RES}). During this time, the output current is limited to a peak value of at least 3 A (after a delay, the power switch can deliver 1.8 A continuous if $V_P \leq 18$ V).

In a normal situation, the voltage on the reset delay capacitor is approximately 3.5 V (depending on the temperature). The power switch output is approximately $V_P - 0.4$ V. At operating temperature, the power switch can deliver at least 3 A. At high temperature, the switch can deliver approximately 2 A.

During an overload condition or a short circuit ($V_{SW} < V_P - 3.7$ V), the voltage on the reset delay capacitor rises 0.6 V above the voltage of regulator 2. This rise time depends on the capacitor connected to pin C_{RES}. During this time, the power switch can deliver more than 3 A. When regulator 2 is out of regulation and generates a reset, the power switch can only deliver 2 A and will immediately go into foldback protection.

At supply voltages >17 V, the power switch is clamped at 16 V maximum (to avoid externally connected circuits being damaged by an overvoltage) and the power switch will switch off at load dump.

Interfacing with the microcontroller (simple full or semi on/off logic applications) can be realized with an independent ignition Schmitt trigger and ignition output buffer (push-pull output).

The timing diagrams are illustrated in Figs 6 and 7.

The second supply voltage V_{P2} is used for the switchable regulators 3 and 4. This input can be connected to a lower supply voltage of ≥6 V to reduce the power dissipation of the TDA3681. A DC-to-DC converter could be used for this purpose.

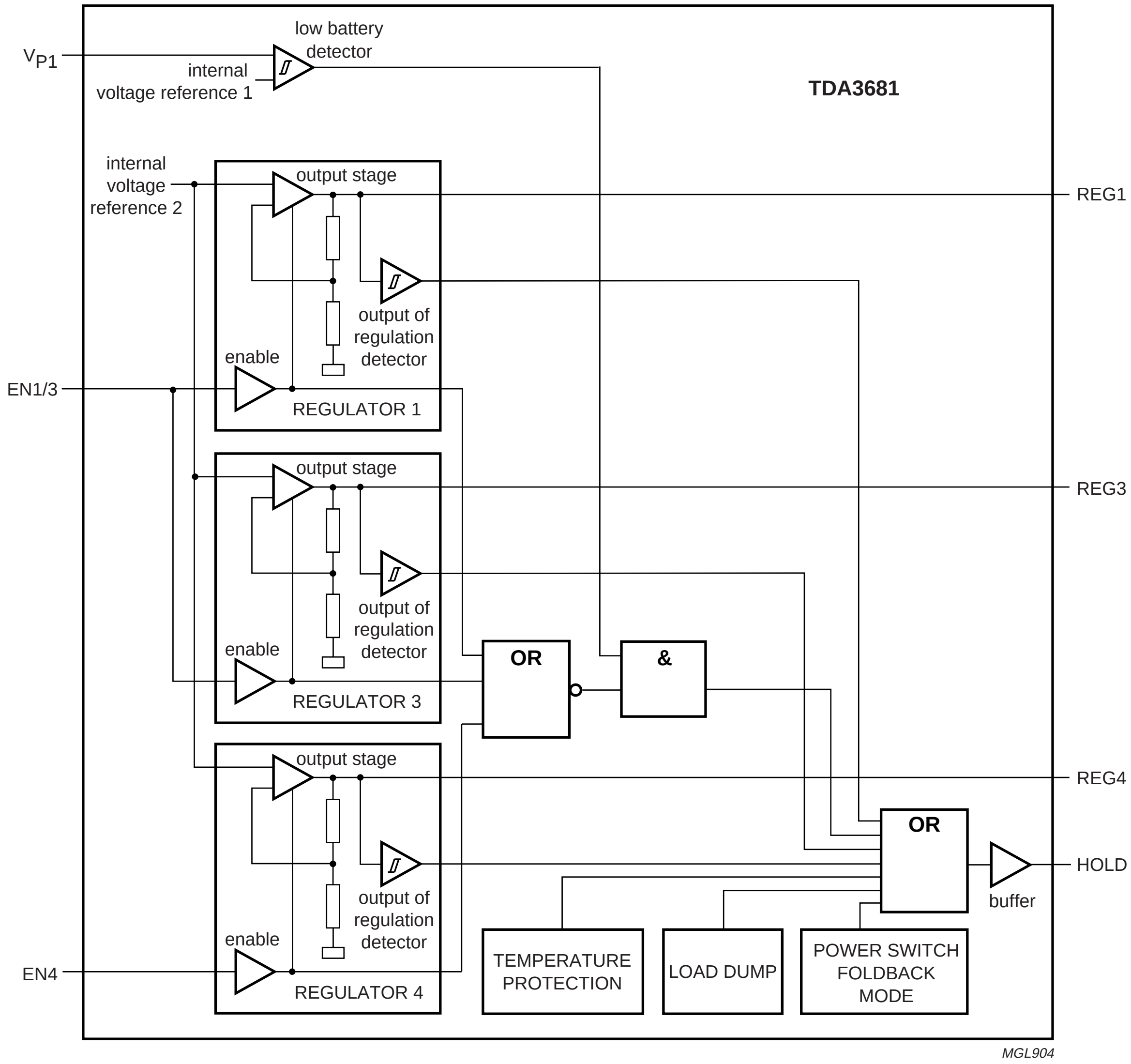
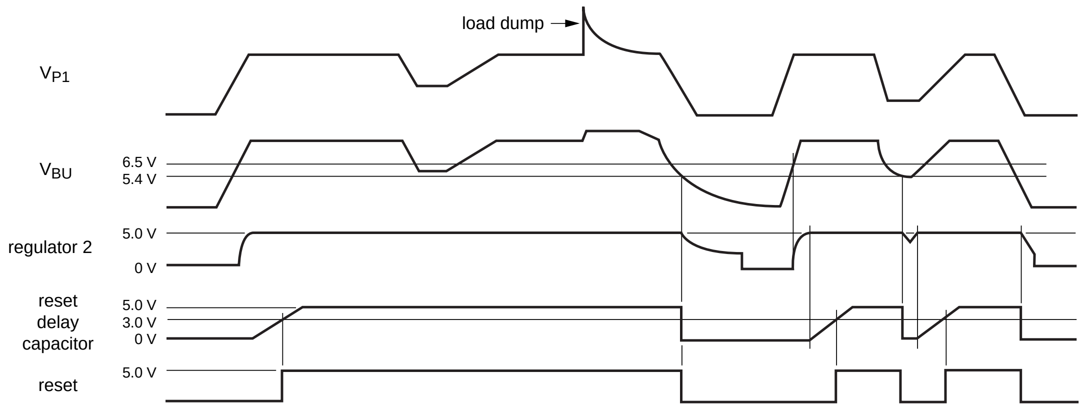
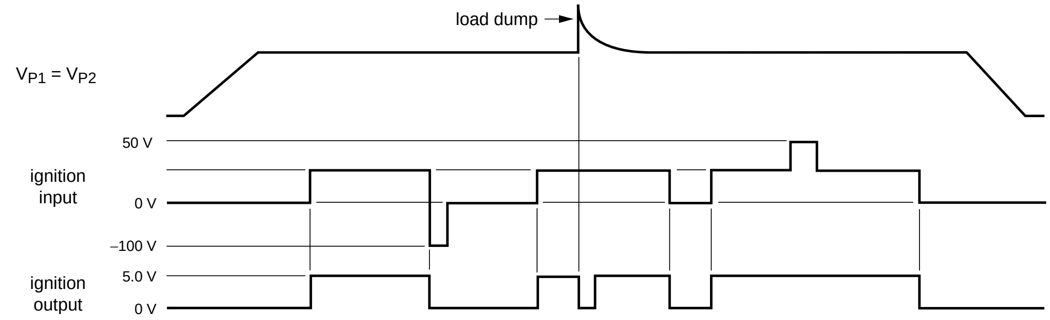


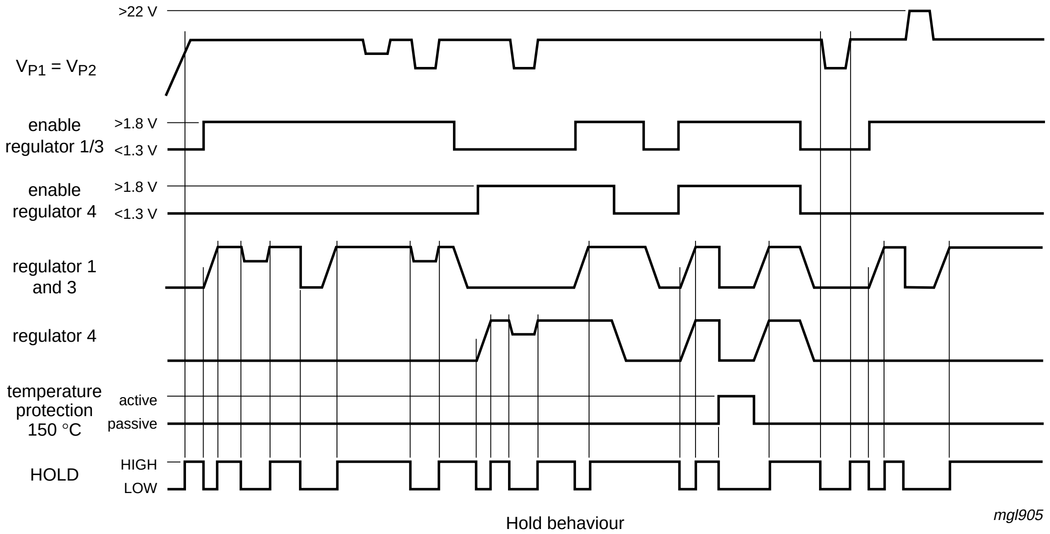
Fig.5 Block diagram of the hold circuit.



Back-up Schmitt trigger and reset behaviour

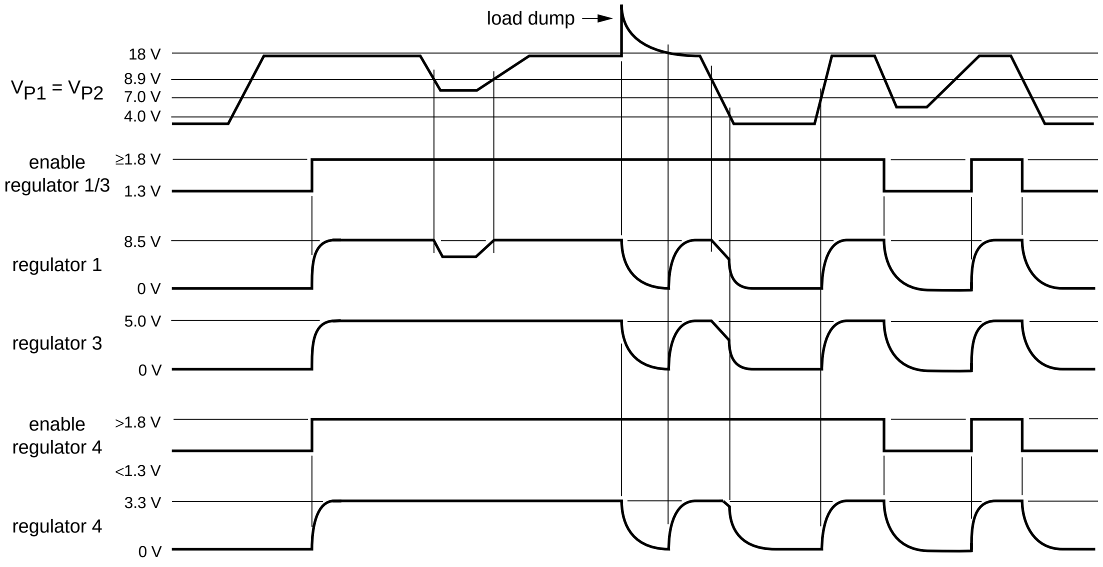


Enable Schmitt trigger ignition

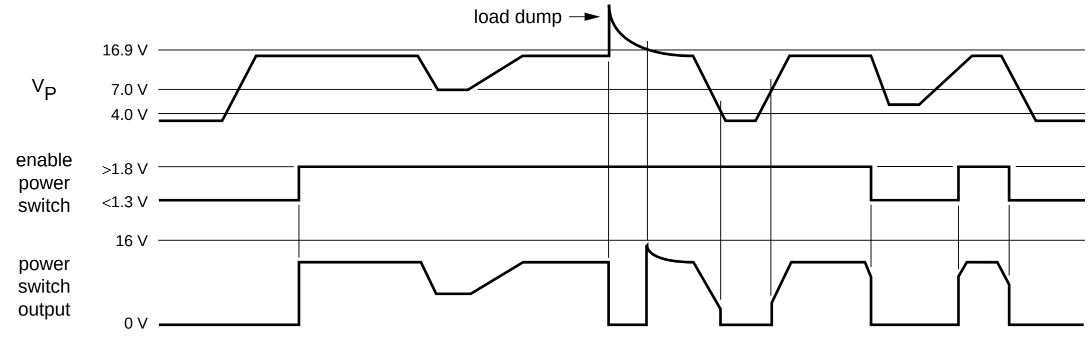


Hold behaviour

Fig.6 Timing diagram of ignition Schmitt triggers and hold circuit.



V_P and enable Schmitt trigger



Power switch behaviour

Fig.7 Timing diagram of regulators and power switch.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{P1}	supply voltage 1				
	operating		–	18	V
	reverse polarity	non-operating	–	18	V
	jump start	$t \leq 10$ minutes	–	30	V
	load dump protection	$t \leq 50$ ms; $t_r \geq 2.5$ ms	–	50	V
V_{P2}	supply voltage 2				
	operating		–	18	V
	reverse polarity	non-operating	–	18	V
	jump start	$t \leq 10$ minutes	–	30	V
	load dump protection	$t \leq 50$ ms; $t_r \geq 2.5$ ms	–	50	V
P_{tot}	total power dissipation		–	62	W
T_{stg}	storage temperature	non-operating	–55	+150	°C
T_{amb}	ambient temperature	operating	–40	+85	°C
T_j	junction temperature	operating	–40	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-c)}$	thermal resistance from junction to case		1.3	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	50	K/W

QUALITY SPECIFICATION

In accordance with *“General Quality Specification For Integrated Circuits (SNW-FQ-611D)”*.

CHARACTERISTICS

$V_P = V_{P1} = V_{P2} = 14.4$ V; $T_{amb} = 25$ °C; measured in test circuits of Figs 10 and 11; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{P1}	supply voltage 1					
	operating		9.5	14.4	18	V
	reverse polarity	non-operating	–	–	18	V
	regulator 2 on	note 1	4	14.4	50	V
	jump start	$t \leq 10$ minutes	–	–	30	V
	load dump protection	$t \leq 50$ ms; $t_r \geq 2.5$ ms	–	–	50	V
V_{P2}	supply voltage 2					
	operating		6.5	14.4	18	V
	reverse polarity	non-operating	–	–	18	V
	regulator 2 on		0	–	50	V
	jump start	$t \leq 10$ minutes	–	–	30	V
	load dump protection	$t \leq 50$ ms; $t_r \geq 2.5$ ms	–	–	50	V
$V_{bat(loaddump)}$	battery overvoltage shutdown	V_{P1} and/or V_{P2}	18	20	22	V
$I_{q(tot)}$	total quiescent supply current	$V_P = 12.4$ V; note 2	–	105	145	µA
		$V_P = 14.4$ V; note 2	–	110	150	µA
Schmitt trigger for power supply (regulators 1, 3 and 4)						
$V_{th(r)}$	rising threshold voltage	V_{P1} rising	6.5	7.0	7.5	V
$V_{th(f)}$	falling threshold voltage	V_{P1} falling	4.0	4.5	5.0	V
V_{hys}	hysteresis voltage		–	2.5	–	V
Schmitt trigger for enable input (regulators 1, 3, 4 and power switch)						
$V_{th(r)}$	rising threshold voltage		1.4	1.8	2.4	V
$V_{th(f)}$	falling threshold voltage		0.9	1.3	1.9	V
V_{hys}	hysteresis voltage	$I_{REG} = I_{SW} = 1$ mA	–	0.5	–	V
I_{LI}	input leakage current	$V_{EN} = 5$ V	1	5	20	µA
Reset trigger level of regulator 2						
$V_{th(r)}$	rising threshold voltage	V_{P1} rising; $I_{REG2} = 50$ mA; note 3	4.43	$V_{REG2} - 0.15$	$V_{REG2} - 0.1$	V
$V_{th(f)}$	falling threshold voltage	V_{P1} falling; $I_{REG2} = 50$ mA; note 3	4.4	$V_{REG2} - 0.25$	$V_{REG2} - 0.13$	V
Schmitt triggers for hold circuit output						
$V_{th(r)(REG1)}$	rising threshold voltage of regulator 1	V_{P1} rising; note 3	–	$V_{REG1} - 0.15$	$V_{REG1} - 0.075$	V
$V_{th(f)(REG1)}$	falling threshold voltage of regulator 1	V_{P1} falling; note 3	7.67	$V_{REG1} - 0.35$	–	V
$V_{hys(REG1)}$	hysteresis voltage due to regulator 1		–	0.2	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{th(r)(REG3)}$	rising threshold voltage of regulator 3	V_{P2} rising; note 3	–	V_{REG3} – 0.15	V_{REG3} – 0.075	V
$V_{th(f)(REG3)}$	falling threshold voltage of regulator 3	V_{P2} falling; note 3	4.3	V_{REG3} – 0.35	–	V
$V_{hys(REG3)}$	hysteresis voltage due to regulator 3		–	0.2	–	V
$V_{th(r)(REG4)}$	rising threshold voltage of regulator 4	V_{P2} rising; note 3	–	V_{REG4} – 0.15	V_{REG4} – 0.075	V
$V_{th(f)(REG4)}$	falling threshold voltage of regulator 4	V_{P2} falling; note 3	2.7	V_{REG4} – 0.3	–	V
$V_{hys(REG4)}$	hysteresis voltage due to regulator 4		–	0.15	–	V
$V_{th(r)(VP)}$	rising threshold voltage of supply voltage	V_{EN} = 0 V	9.1	9.7	10.3	V
$V_{th(f)(VP)}$	falling threshold voltage of supply voltage	V_{EN} = 0 V	9.0	9.4	9.8	V
$V_{hys(VP)}$	hysteresis voltage of supply voltage	V_{EN} = 0 V	–	0.3	–	V
Reset and hold buffer						
$I_{sink(L)}$	LOW-level sink current	$V_{RES} \leq 0.8$ V; $V_{HOLD} \leq 0.8$ V	2	–	–	mA
I_{LO}	output leakage current	V_{P2} = 14.4 V; V_{HOLD} = 5 V	–	0.1	5	μA
$I_{source(H)}$	HIGH-level source current	V_{P2} = 14.4 V; $V_{RES} \geq 4.5$ V	240	400	900	μA
t_r	rise time	note 4	–	7	50	μs
t_f	fall time	note 4	–	1	50	μs
Reset delay						
I_{ch}	reset delay capacitor charge current	V_{CRES} = 0 V	2	4	8	μA
I_{dch}	reset delay capacitor discharge current	V_{CRES} = 3 V; $V_{P1} = V_{P2}$ = 4.3 V	1.0	1.6	–	mA
$V_{th(r)(RES)}$	rising voltage threshold reset signal		2.5	3.0	3.5	V
$V_{th(f)(RES)}$	falling voltage threshold reset signal		1.0	1.2	1.4	V
$t_{d(RES)}$	delay reset signal	C_{RES} = 47 nF; note 5	20	35	70	ms
$t_{d(SW)}$	delay power switch foldback protection	C_{RES} = 47 nF; note 6	8	17.6	40	ms
Regulator 1 (I_{REG1} = 5 mA; unless otherwise specified)						
$V_{o(off)}$	output voltage off		–	1	400	mV
$V_{o(REG1)}$	output voltage	1 mA $\leq I_{REG1} \leq$ 600 mA	8.0	8.5	9.0	V
		9.5 V $\leq V_{P1} \leq$ 18 V	8.0	8.5	9.0	V
ΔV_{line}	line regulation	9.5 V $\leq V_{P1} \leq$ 18 V	–	2	75	mV
ΔV_{load}	load regulation	1 mA $\leq I_{REG1} \leq$ 600 mA	–	20	85	mV

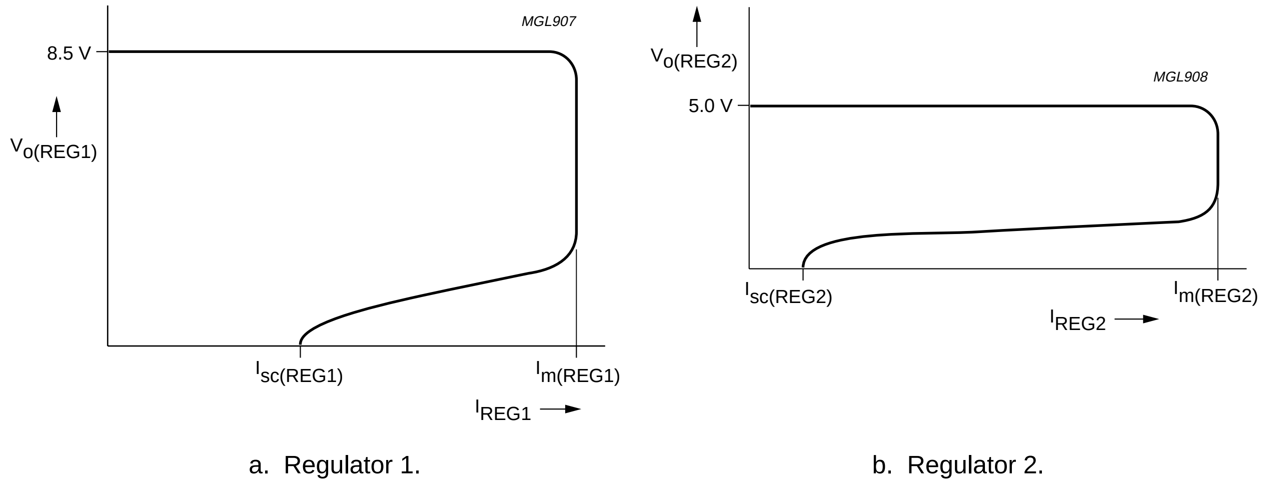
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_q	quiescent current	I_{REG1} = 600 mA	–	25	60	mA
SVRR	supply voltage ripple rejection	f_i = 3 kHz; V_i = 2 V (p-p)	60	70	–	dB
$V_{drop(REG1)}$	drop-out voltage	I_{REG1} = 550 mA; V_{P1} = 8.55 V; note 7	–	0.4	0.7	V
$I_{m(REG1)}$	current limit	V_{REG1} > 7 V; note 8	0.65	1.2	–	A
$I_{sc(REG1)}$	short-circuit current	$R_L \leq 0.5\ \Omega$; note 9	250	800	–	mA
Regulator 2 (I_{REG2} = 5 mA; unless otherwise specified)						
$V_{o(REG2)}$	output voltage	0.5 mA ≤ I_{REG2} ≤ 300 mA	4.75	5.0	5.25	V
		7 V ≤ V_{P1} ≤ 18 V	4.75	5.0	5.25	V
		18 V ≤ V_{P1} ≤ 50 V; I_{REG2} ≤ 150 mA	4.75	5.0	5.25	V
ΔV_{line}	line regulation	6 V ≤ V_{P1} ≤ 18 V	–	2	50	mV
		6 V ≤ V_{P1} ≤ 50 V	–	15	75	mV
ΔV_{load}	load regulation	1 mA ≤ I_{REG2} ≤ 150 mA	–	20	50	mV
		1 mA ≤ I_{REG2} ≤ 300 mA	–	–	100	mV
SVRR	supply voltage ripple rejection	f_i = 3 kHz; V_i = 2 V (p-p)	50	55	–	dB
$V_{drop(REG2)}$	drop-out voltage	I_{REG2} = 100 mA; V_{P1} = 4.75 V; note 7	–	0.4	0.6	V
		I_{REG2} = 200 mA; V_{P1} = 5.75 V; note 7	–	0.8	1.2	V
		I_{REG2} = 100 mA; V_{BU} = 4.75 V; note 10	–	0.2	0.5	V
		I_{REG2} = 200 mA; V_{BU} = 5.75 V; note 10	–	0.8	1.0	V
$I_{m(REG2)}$	current limit	V_{REG2} > 4.5 V; note 8	0.32	0.37	–	A
$I_{sc(REG2)}$	short-circuit current	$R_L \leq 0.5\ \Omega$; note 9	95	120	–	mA
Regulator 3 (I_{REG3} = 5 mA; unless otherwise specified)						
$V_{o(off)}$	output voltage off		–	1	400	mV
$V_{o(REG3)}$	output voltage	1 mA ≤ I_{REG3} ≤ 1400 mA	4.75	5.0	5.25	V
		7 V ≤ V_{P1} and/or V_{P2} ≤ 18 V	4.75	5.0	5.25	V
ΔV_{line}	line regulation	7 V ≤ V_{P1} and/or V_{P2} ≤ 18 V	–	2	50	mV
ΔV_{load}	load regulation	1 mA ≤ I_{REG3} ≤ 1400 mA	–	20	150	mV
I_q	quiescent current	I_{REG3} = 1400 mA	–	19	45	mA
SVRR	supply voltage ripple rejection	f_i = 3 kHz; V_i = 2 V (p-p)	60	70	–	dB
$V_{drop(REG3)}$	drop-out voltage	I_{REG3} = 1400 mA ; V_{P2} = 6 V; note 7	–	1	1.5	V
$I_{m(REG3)}$	current limit	V_{REG3} > 4.5 V; note 8	1.5	1.7	–	A
$I_{sc(REG3)}$	short-circuit current	$R_L \leq 0.5\ \Omega$; note 9	430	750	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Regulator 4 (I_{REG4} = 5 mA; unless otherwise specified)						
$V_{o(off)}$	output voltage off		–	1	400	mV
$V_{o(REG4)}$	output voltage	1 mA ≤ I_{REG4} ≤ 1 A	3.14	3.3	3.46	V
		6.5 V ≤ V_{P1} and/or V_{P2} ≤ 18 V	3.14	3.3	3.46	V
ΔV_{line}	line regulation	6.5 V ≤ V_{P1} and/or V_{P2} ≤ 18 V	–	2	50	mV
ΔV_{load}	load regulation	1 mA ≤ I_{REG4} ≤ 1 A	–	20	50	mV
I_q	quiescent current	I_{REG4} = 1 A	–	15	40	mA
SVRR	supply voltage ripple rejection	f_i = 3 kHz; V_i = 2 V (p-p)	60	70	–	dB
$V_{drop(REG4)}$	drop-out voltage	I_{REG4} = 1 A; V_{P2} = 5 V; note 7	–	1.7	2.4	V
$I_{m(REG4)}$	current limit	V_{REG4} > 3.0 V; note 8	1.1	1.5	–	A
$I_{sc(REG4)}$	short-circuit current	R_L ≤ 0.5 Ω; note 9	470	750	–	mA
Power switch						
$V_{drop(SW)}$	drop-out voltage	I_{SW} = 1 A; V_{P1} = 13.5 V; note 11	–	0.45	0.65	V
		I_{SW} = 1.8 A; V_{P1} = 13.5 V; note 11	–	1.0	1.8	V
$I_{DC(SW)}$	continuous current	V_{P1} = 16 V; V_{SW} = 13.5 V	1.8	2.0	–	A
$V_{clamp(SW)}$	clamping voltage	V_{P1} ≥ 17 V; 1 mA < I_{SW} < 1.8 A	13.5	15.0	16.0	V
$I_{M(SW)}$	peak current	V_{P1} < 17 V; notes 6, 12 and 13	3	–	–	A
$V_{fb(SW)}$	flyback voltage behaviour	I_{SW} = –100 mA	–	V_{P1} + 3	22	V
$I_{sc(SW)}$	short-circuit current	V_{P1} = 14.4 V; V_{SW} < 1.2 V; note 13	0.5	1.7	–	A
Backup switch						
$I_{DC(BU)}$	continuous current	V_{BU} > 5 V	0.3	0.35	–	A
$V_{clamp(BU)}$	clamping voltage	V_{P1} ≥ 16.7 V; I_{REG2} = 100 mA	–	–	16	V
$I_{r(BU)}$	reverse current	V_{P1} = 0 V; V_{BU} = 12.4 V	–	–	900	µA
Schmitt trigger for enable ignition input						
$V_{th(r)(IGNIN)}$	rising threshold voltage of ignition input	V_{P1} > 3.5 V	1.9	2.2	2.5	V
$V_{th(f)(IGNIN)}$	falling threshold voltage of ignition input	V_{P1} > 3.5 V	1.7	2.0	2.3	V
$V_{hys(IGNIN)}$	hysteresis voltage	V_P > 3.5 V	0.1	0.2	0.5	V
I_{LI}	input leakage current	V_{IGNIN} = 5 V	–	–	1.0	µA
$I_{i(clamp)}$	input clamp current	V_{IGNIN} ≤ 50 V	–	–	50	mA
$V_{IH(clamp)}$	HIGH-level input clamping voltage		V_{P1}	–	50	V
$V_{IL(clamp)}$	LOW-level input clamping voltage	V_{IGNIN} ≥ –100 V	–0.6	–	0	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Ignition buffer						
V_{OL}	LOW-level output voltage	I_{IGNOUT} = 0 mA	0	0.2	0.8	V
V_{OH}	HIGH-level output voltage	I_{IGNOUT} = 0 mA	4.5	5.0	5.25	V
I_{OL}	LOW-level sink current	$V_{IGNOUT} \leq 0.8$ V	0.45	0.8	–	mA
I_{OH}	HIGH-level source current	$V_{IGNOUT} \geq 4.5$ V	0.45	2.0	–	mA
t_{PLH}	LOW-to-HIGH propagation time	V_{IGNIN} rising from 1.7 to 2.5 V	–	–	500	µs
t_{PHL}	HIGH-to-LOW propagation time	V_{IGNIN} falling from 2.5 to 1.7 V	–	–	500	µs
Temperature protection						
$T_{j(sd)}$	junction temperature for shutdown		150	160	170	°C
$T_{j(hold)}$	junction temperature for hold trigger		150	160	170	°C

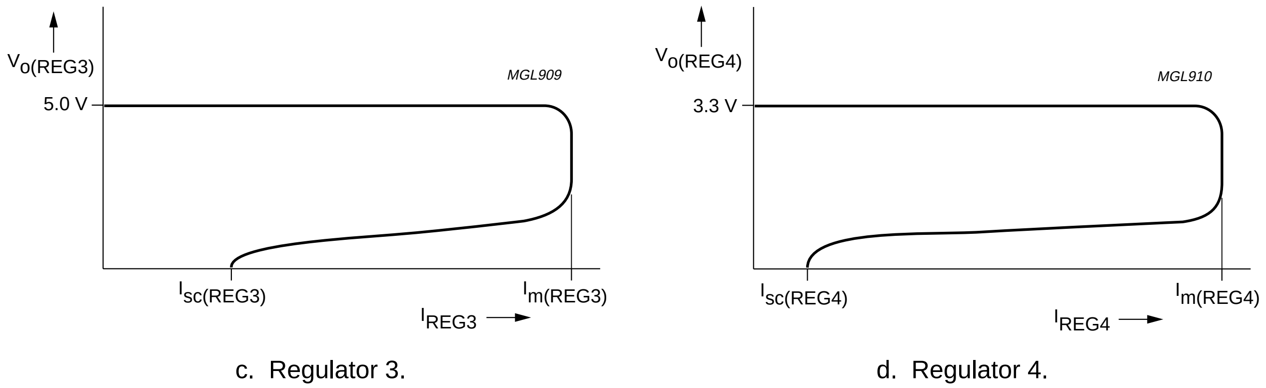
Notes

1. Minimum operating voltage, only if V_{P1} has exceeded 6.5 V.
2. The total quiescent current is measured in the standby mode. Therefore, the enable inputs of regulators 1, 3, 4 and the power switch are grounded and $R_{L(REG2)} = \infty$; see Figs 10 and 11.
3. The voltage of the regulator drops as a result of a V_{P1} drop for regulators 1 and 2. Regulators 3 and 4 drop as a result of V_{P2} drop.
4. The rise and fall times are measured with a 10 kΩ pull-up resistor and a 50 pF load capacitor.
5. The delay time depends on the value of the reset delay capacitor: $t_{d(RES)} = \frac{C}{I_{ch}} \times V_{C(th)} = C \times (750 \times 10^3) [s]$
6. The delay time depends on the value of the reset delay capacitor: $t_{d(SW)} = \frac{C}{I_{ch}} \times V_{C(th)} = C \times (375 \times 10^3) [s]$
7. The drop-out voltage of regulators 1 and 2 is measured between pins V_{P1} and REGn. The drop-out voltage of regulators 3 and 4 is measured between pins V_{P2} and REGn.
8. At current limit, $I_{m(REGn)}$ is held constant (see Fig.8).
9. The foldback current protection limits the dissipated power at short-circuit (see Fig.8).
10. The drop-out voltage is measured between pins BU and REG2.
11. The drop-out voltage of the power switch is measured between pins V_{P1} and SW.
12. The maximum output current of the power switch is limited to 1.8 A when the supply voltage exceeds 18 V.
13. At short-circuit, $I_{sc(SW)}$ of the power switch is held constant to a lower value than the continuous current after a delay of at least 10 ms.



a. Regulator 1.

b. Regulator 2.



c. Regulator 3.

d. Regulator 4.

Fig.8 Foldback current protection of the regulators.

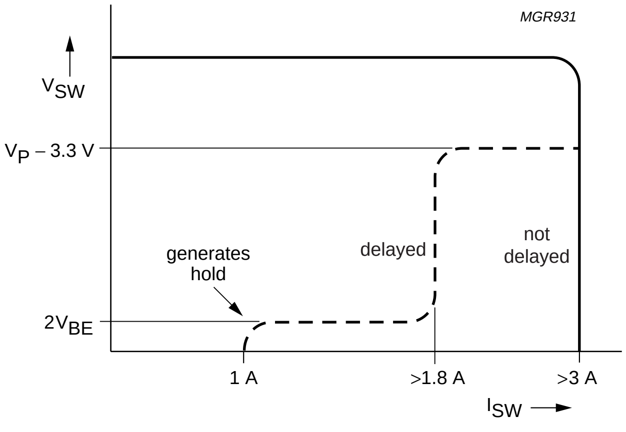
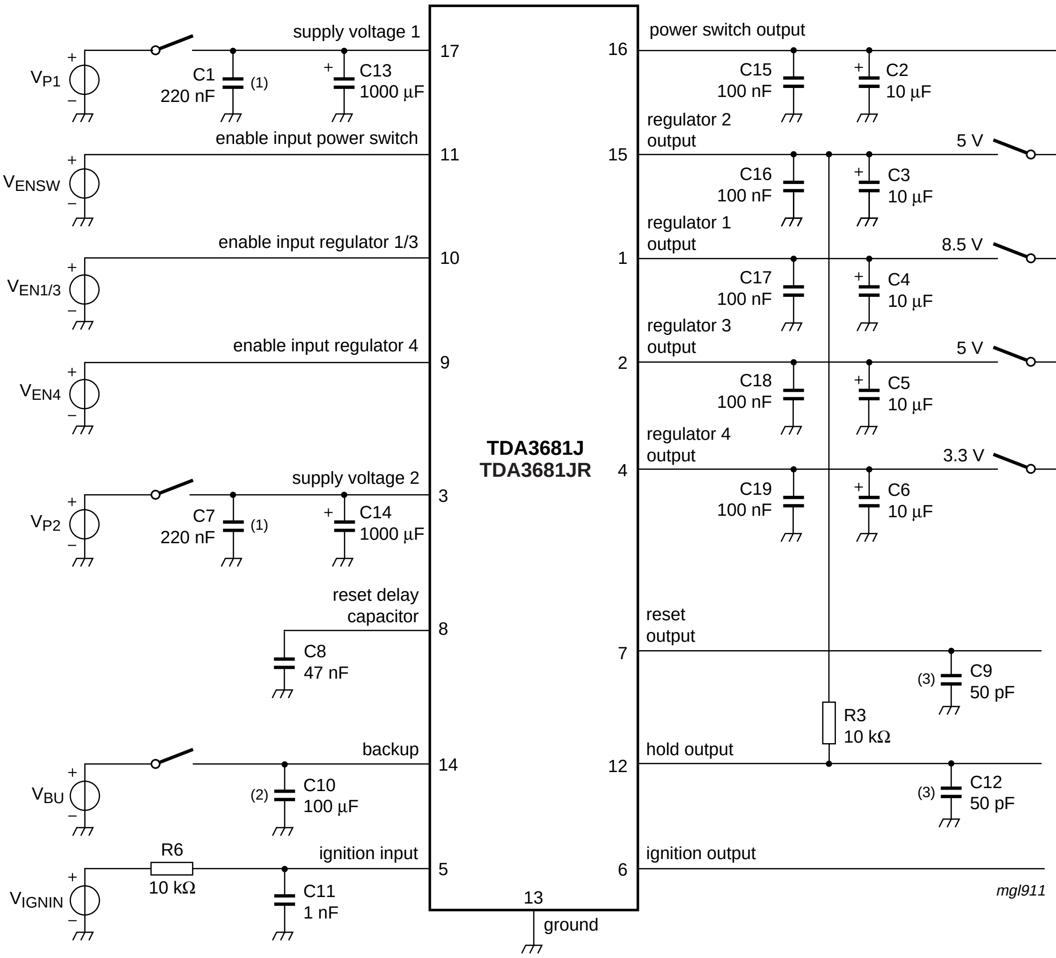


Fig.9 Current protection of the power switch.

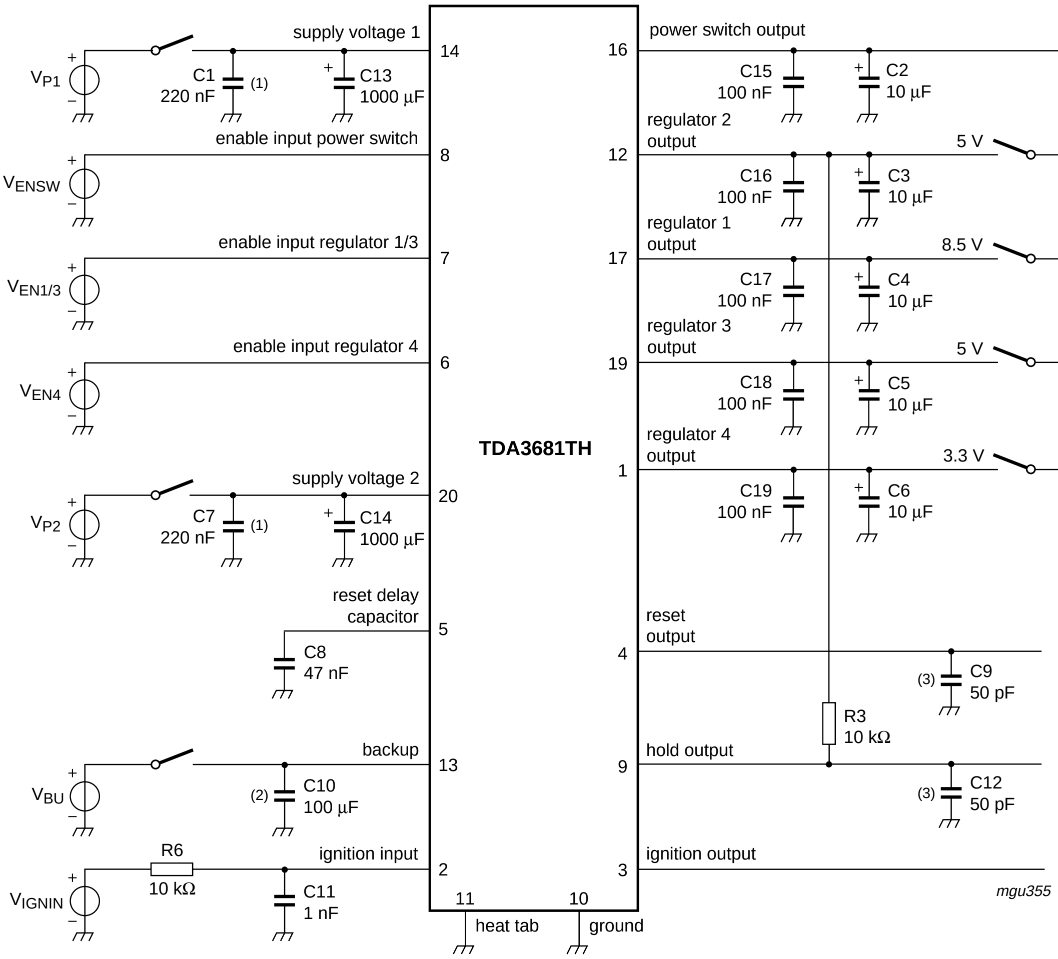
TEST AND APPLICATION INFORMATION

Test information



(1) A minimum capacitor of 220 nF on the supply lines V_{P1} and V_{P2} is required for stability.
(2) A minimum capacitor of 1 µF for backup supply is required for stability.
(3) Capacitor represents the typical input capacitance of CMOS logic connected to the reset and hold outputs.

Fig.10 Test circuit of TDA3681J and TDA3681JR.



(1) A minimum capacitor of 220 nF on the supply lines V_{P1} and V_{P2} is required for stability.

(2) A minimum capacitor of 1 µF for backup supply is required for stability.

(3) Capacitor represents the typical input capacitance of CMOS logic connected to the reset and hold outputs.

Fig.11 Test circuit of TDA3681TH.

Application information

NOISE

Table 1 Noise figures

REGULATOR	**NOISE FIGURE (μV)**[1]		
	C_o = 10 μF	**C_o = 47 μF**	**C_o = 100 μF**
1	170	110	110
2	440	240	190
3	120	100	80
4	85	70	55

Note

1. Measured at a bandwidth of 30 kHz.

The noise on the supply line depends on the value of the supply capacitor and is caused by a current noise (the output noise of the regulators is translated to a current noise by the output capacitors). The noise is minimal when a high frequency capacitor of 220 nF in parallel with an electrolytic capacitor of 100 μF is connected directly to the supply pins V_{P1}, V_{P2} and GND.

STABILITY

The regulators are stabilized by the externally connected output capacitors.

The output capacitors can be selected by using the graphs given in Figs 12 and 13. When an electrolytic capacitor is used, its temperature behaviour can cause oscillations at a low temperature. The two examples below show how an output capacitor value is selected.

Example 1

Regulators 1, 3 and 4 are stabilized with an electrolytic output capacitor of 220 μF (ESR = 0.15 Ω). At T_{amb} = –30 °C, the capacitor value is decreased to 73 μF and the ESR is increased to 1.1 Ω. The regulator remains stable at T_{amb} = –30 °C; see Fig.12.

Example 2

Regulator 2 is stabilized with a 10 μF electrolytic capacitor (ESR = 3 Ω). At T_{amb} = –30 °C, the capacitor value is decreased to 3 μF and the ESR is increased to 23.1 Ω. As can be seen from Fig.13, the regulator will be unstable at T_{amb} = –30 °C.

Solution

To avoid problems with stability at low temperatures, the use of tantalum capacitors is recommended. Use a tantalum capacitor of 10 μF or a larger electrolytic capacitor.

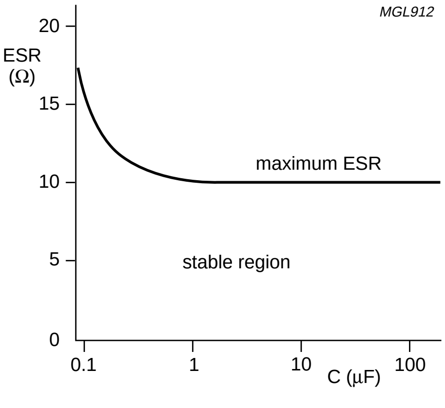


Fig.12 Curve for selecting the value of the output capacitor for regulators 1, 3 and 4.

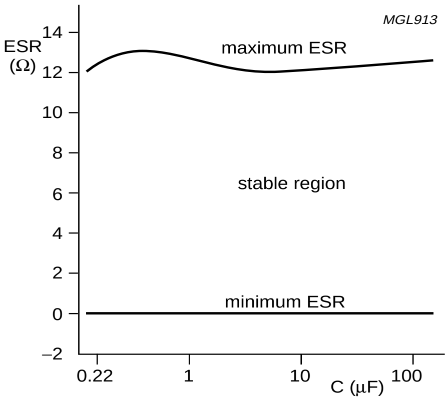


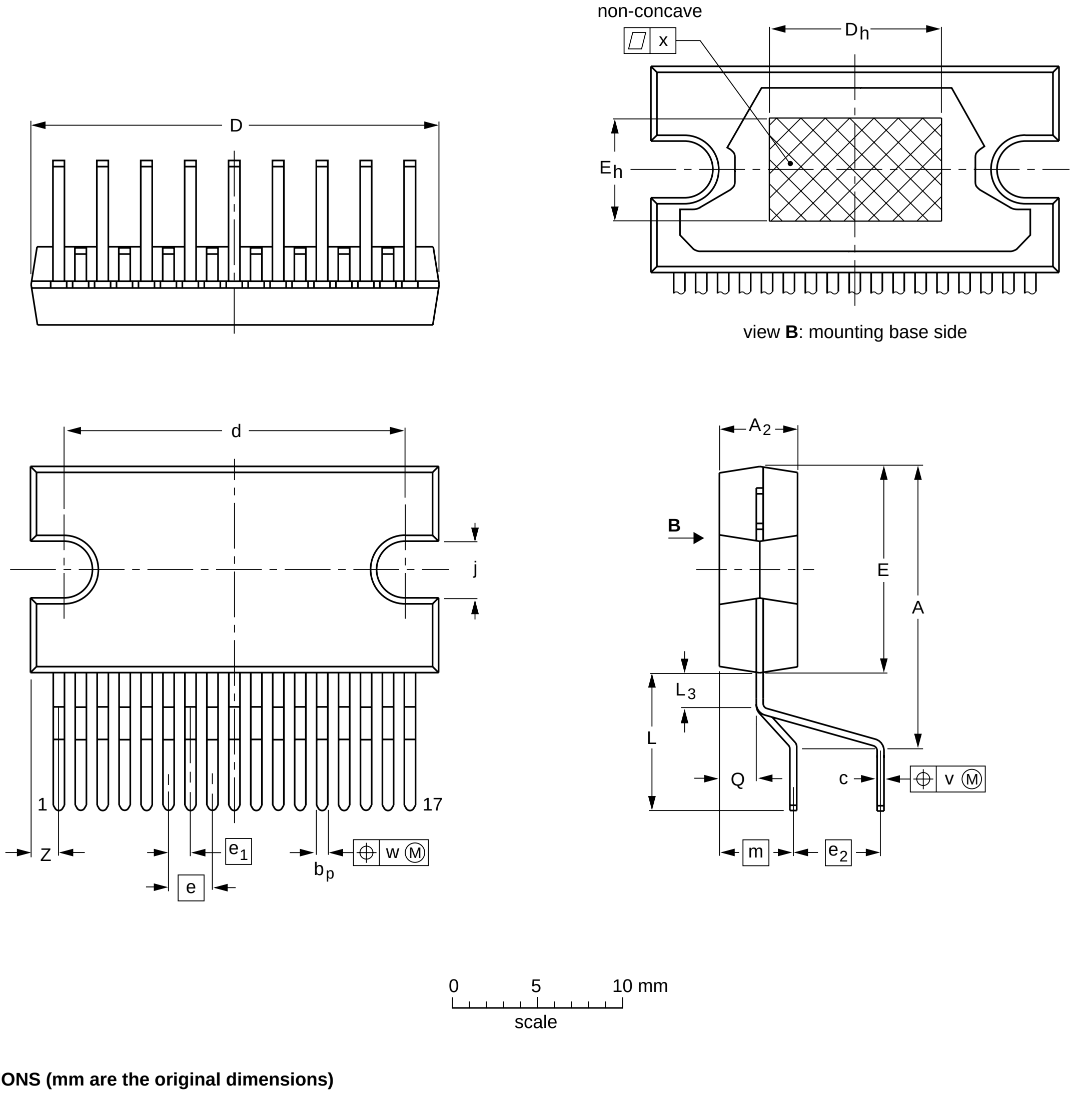
Fig.13 Curve for selecting the value of the output capacitor for regulator 2.

Multiple voltage regulator with switch and ignition buffer

TDA3681

PACKAGE OUTLINES

DBS17P: plastic DIL-bent-SIL power package; 17 leads (lead length 7.7 mm) SOT243-3



DIMENSIONS (mm are the original dimensions)

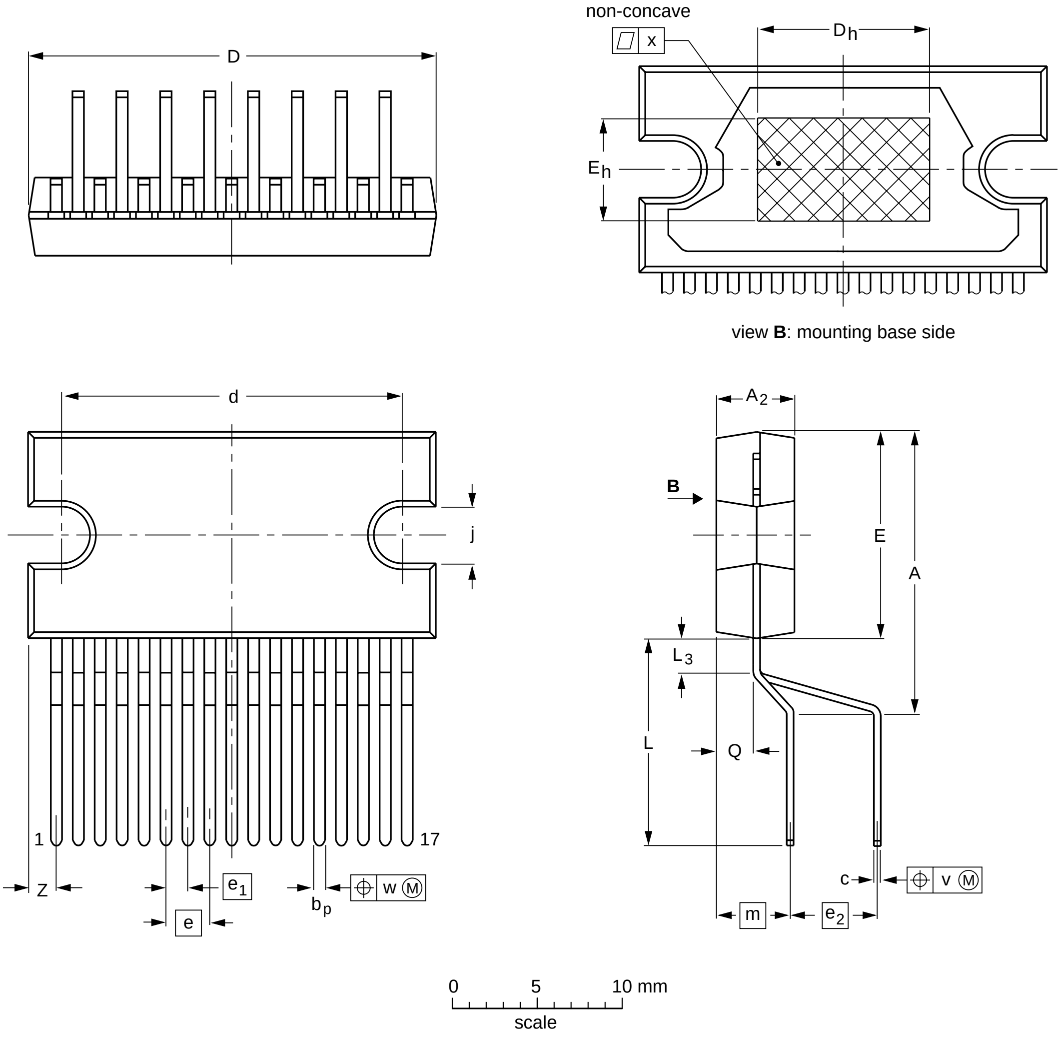
UNIT	A	A_2	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	j	L	L_3	m	Q	v	w	x	$Z^{(1)}$
mm	17.0 15.5	4.6 4.4	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	2.54	1.27	5.08	6	3.4 3.1	8.4 7.0	2.4 1.6	4.3	2.1 1.8	0.6	0.25	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT243-3						~~99-12-17~~ 03-03-12

DBS17P: plastic DIL-bent-SIL (special bent) power package; 17 leads (lead length 12 mm) SOT475-1



DIMENSIONS (mm are the original dimensions)

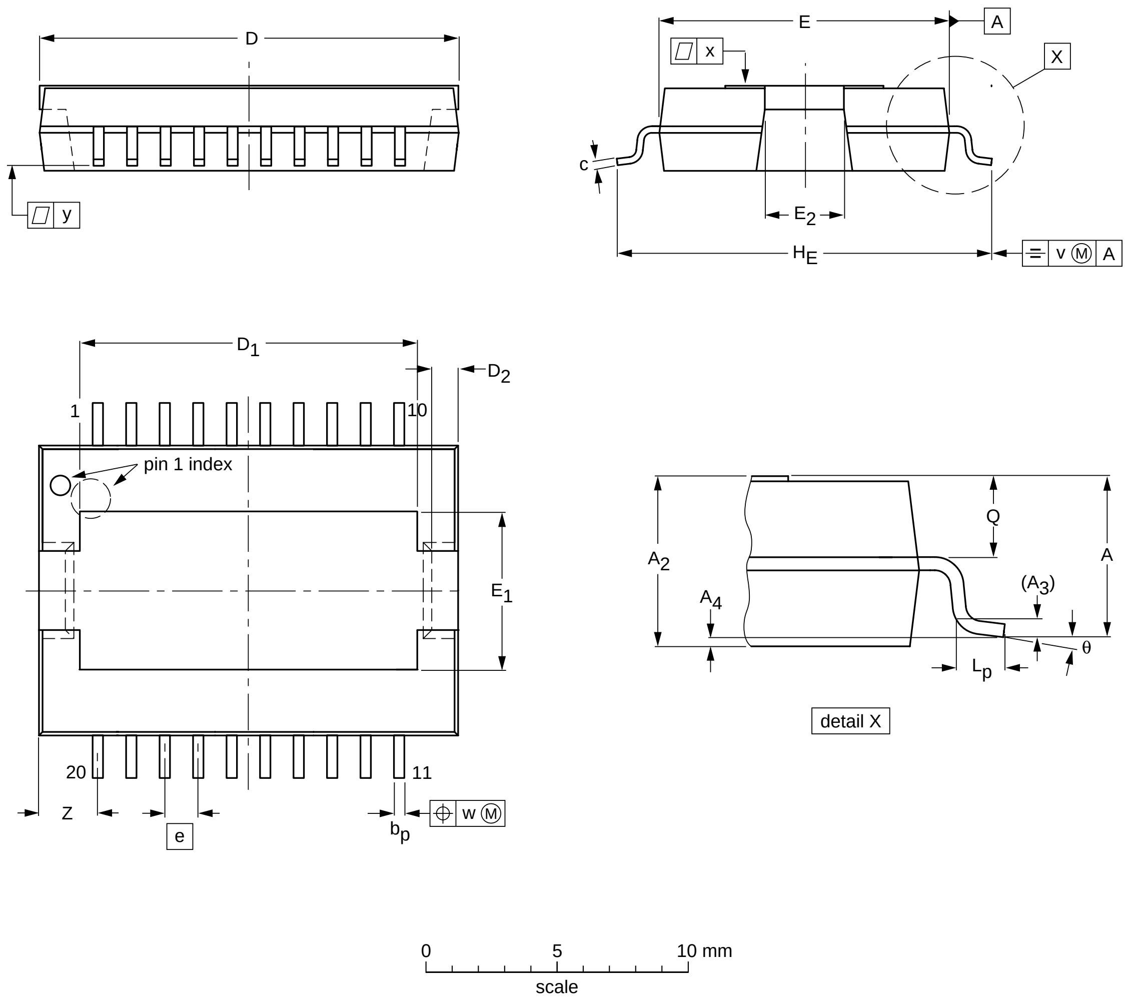
UNIT	A	A_2	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	j	L	L_3	m	Q	v	w	x	$Z^{(1)}$
mm	17.0 15.5	4.6 4.4	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	2.54	1.27	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.4	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT475-1						~~99-12-17~~ 03-03-12

HSOP20: plastic, heatsink small outline package; 20 leads; low stand-off height **SOT418-3**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_2	A_3	$A_4^{(1)}$	b_p	c	$D^{(2)}$	D_1	D_2	$E^{(2)}$	E_1	E_2	e	H_E	L_p	Q	v	w	x	y	Z	θ
mm	3.5	3.5 3.2	0.35	+0.08 −0.04	0.53 0.40	0.32 0.23	16.0 15.8	13.0 12.6	1.1 0.9	11.1 10.9	6.2 5.8	2.9 2.5	1.27	14.5 13.9	1.1 0.8	1.7 1.5	0.25	0.25	0.03	0.07	2.5 2.0	8° 0°

Notes

1. Limits per individual lead.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT418-3						~~02-02-12~~ 03-07-23

SOLDERING

Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Through-hole mount packages

SOLDERING BY DIPPING OR BY SOLDER WAVE

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

MANUAL SOLDERING

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Surface mount packages

REFLOW SOLDERING

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven.

Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all the BGA, HTSSON..T and SSOP-T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

WAVE SOLDERING

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

MANUAL SOLDERING

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of IC packages for wave, reflow and dipping soldering methods

MOUNTING	PACKAGE[1]	SOLDERING METHOD		
		WAVE	REFLOW[2]	DIPPING
Through-hole mount	CPGA, HCPGA	suitable	–	suitable
	DBS, DIP, HDIP, RDBS, SDIP, SIL	suitable[3]	–	–
Through-hole-surface mount	PMFP[4]	not suitable	not suitable	–
Surface mount	BGA, HTSSON..T[5], LBGA, LFBGA, SQFP, SSOP-T[5], TFBGA, USON, VFBGA	not suitable	suitable	–
	DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[6]	suitable	–
	PLCC[7], SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended[7][8]	suitable	–
	SSOP, TSSOP, VSO, VSSOP	not recommended[9]	suitable	–
	CWQCCN..L[11], PMFP[10], WQCCN32L[11]	not suitable	not suitable	–

Notes

1. For more detailed information on the BGA packages refer to the *“(LF)BGA Application Note*” (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *“Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”*.
3. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
4. Hot bar soldering or manual soldering is suitable for PMFP packages.
5. These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
6. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
7. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
8. Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
9. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
10. Hot bar or manual soldering is suitable for PMFP packages.
11. Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

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