INTEGRATED CIRCUITS

DATA SHEET

UAA2077AM

Image rejecting front-end
for DECT applications

Product specification

Supersedes data of 1995 Feb 16
File under Integrated Circuits, IC17

1996 Jul 04

Philips
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Image rejecting front-end for DECT applications

UAA2077AM

FEATURES

- Low-noise, wide dynamic range amplifier
- Very low noise figure
- Dual balanced mixer for over 25 dB on-chip image rejection
- IF I/Q combiner at 110 MHz
- On-chip quadrature network
- RX fast **on/off** power-down mode
- Shrink small outline packaging
- Very small application (no image filter).

APPLICATIONS

- 1800 MHz front-end for DECT hand-portable equipment
- Compact digital mobile communication equipment
- TDMA receivers.

GENERAL DESCRIPTION

UAA2077AM contains a high frequency low noise receiver front-end intended to be used in DECT mobile telephones. Designed in an advanced BiCMOS process it combines high performance with low power consumption and a high degree of integration, thus reducing external component costs and total front-end size.

The main advantage of the UAA2077AM is its ability to provide over 25 dB of image rejection. Consequently, the image filter between the LNA and the mixer is suppressed.

Image rejection is achieved in the internal architecture by two RF mixers in quadrature and two all-pass filters in I and Q IF channels that phase shift the IF by 45° and 135° respectively. The two phase shifted IFs are recombined and buffered to furnish the IF output signal.

For instance, signals presented at the RF input at LO + IF frequency are rejected through this signal processing while signals at LO − IF frequency can form the IF signal. An internal switch enables the upper or lower image frequency to be rejected.

The receiver section consists of a low-noise amplifier that drives a quadrature mixer pair. The IF amplifier has on-chip 45° and 135° phase shifting and a combining network for image rejection. The IF driver has differential open-collector type outputs.

The LO part consists of an internal all-pass type phase shifter to provide quadrature LO signals to the receive mixers.The centre frequency of the phase shifter is adjustable for maximum image rejection in a given band. The all-pass filters outputs are buffered before being fed to the receive mixers. All RF and IF inputs or outputs are balanced.

Two pins RXON and SXON are used to control the different power-down modes. A special mode of operation called synthesizer-on mode (SX mode), controlled by pin SXON can be used to minimize the LO pulling when the receiver is turned **on**. When SXON is HIGH, all internal buffers on the LO path are turned **on**. Pin SBS allows a selection of whether to reject the upper or lower image frequency. Special care has been taken for fast power-up switching.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	T_{amb} = 0 to +70 °C	3.15	4.0	5.3	V
		over full temperature range	3.6	4.0	5.3	V
$I_{CC(RX)}$	receive supply current		21.5	26.5	33.5	mA
$I_{CC(PD)}$	supply current in power-down		–	0.2	50	μA
T_{amb}	operating ambient temperature		−30	+25	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	NAME	DESCRIPTION		VERSION
UAA2077AM	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm		SOT266-1

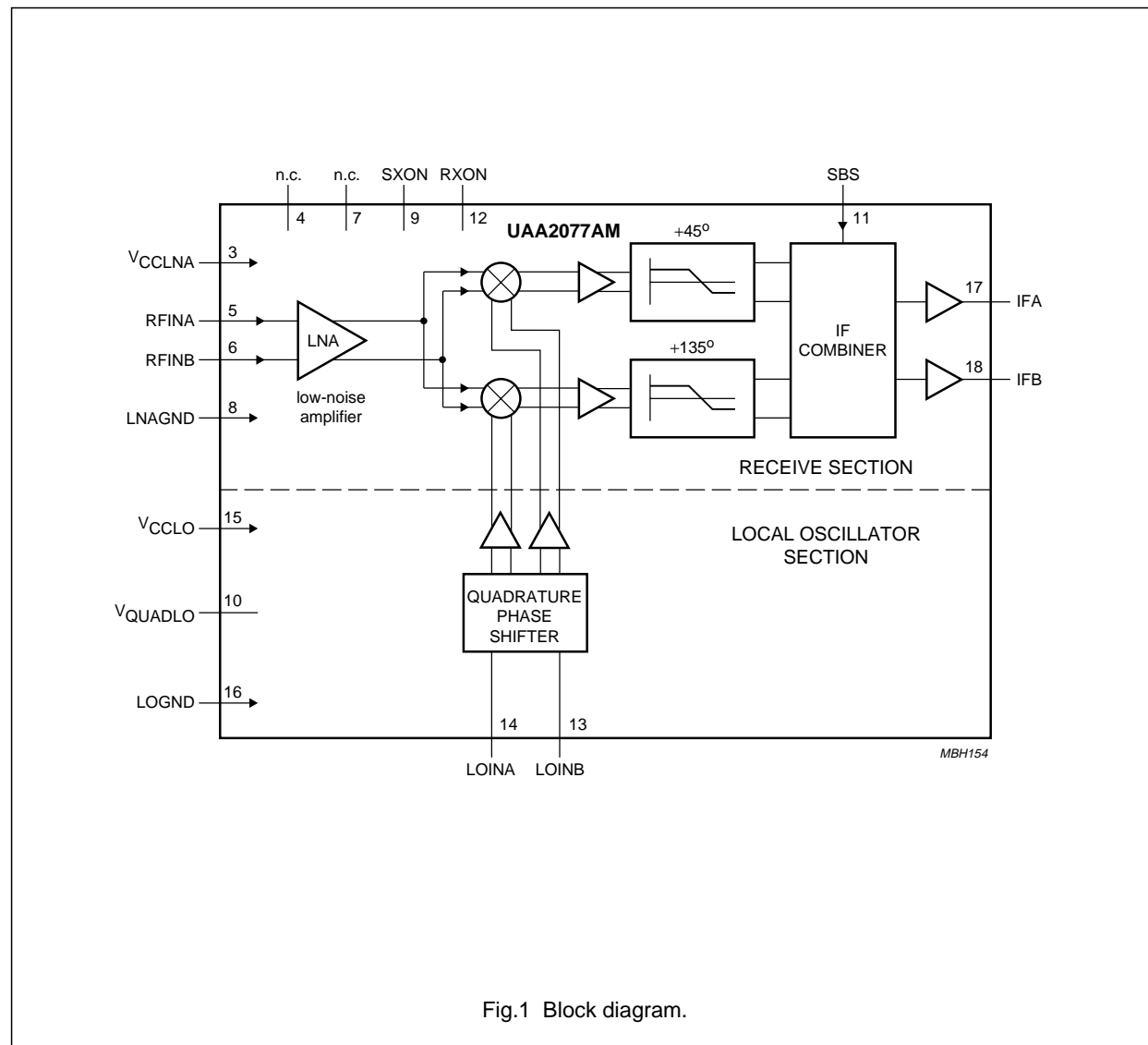## Image rejecting front-end for DECT applications

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BLOCK DIAGRAM

Fig.1 Block diagram.

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PINNING

| SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
n.c.	2	not connected
V_{CCLNA}	3	supply voltage for LNA and IF parts
n.c.	4	not connected
RFINA	5	RF input A (balanced)
RFINB	6	RF input B (balanced)
n.c.	7	not connected
LNAGND	8	ground for LNA and IF parts
SXON	9	SX mode enable (see Table 1)
V_{QUADLO}	10	input voltage for LO quadrature trimming
SBS	11	sideband selection
RXON	12	RX mode enable (see Table 1)
LOINB	13	LO input B (balanced)
LOINA	14	LO input A (balanced)
V_{CCLO}	15	supply voltage for LO parts
LOGND	16	ground for LO parts
IFA	17	IF output A (balanced)
IFB	18	IF output B (balanced)
n.c.	19	not connected
n.c.	20	not connected
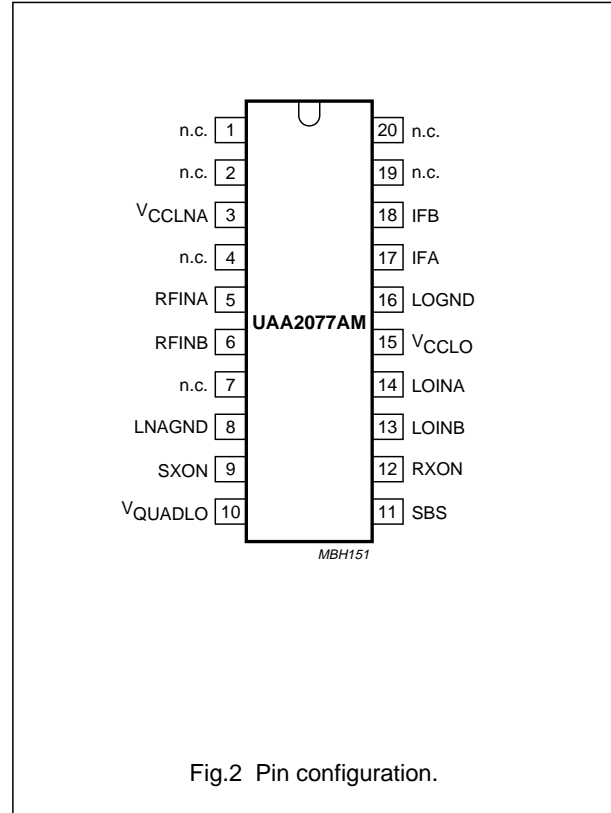
Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Receive section

The circuit contains a low-noise amplifier followed by two high dynamic range mixers. These mixers are of the Gilbert-cell type, the whole internal architecture is fully differential.

The local oscillator, shifted in phase to 45° and 135°, mixes the amplified RF to create I and Q channels.
The two I and Q channels are buffered, phase shifted by 45° and 135° respectively, amplified and recombined internally to realize the image rejection.

Pin SBS allows sideband selection:

- $f_{LO} > f_{RF}$ (SBS = 1)
- $f_{LO} < f_{RF}$ (SBS = 0).

where f_{RF} is the frequency of the wanted signal.

Balanced signal interfaces are used for minimizing crosstalk due to package parasitics.

The IF output is differential and of the open-collector type. Typical application will load the output with a differential 1 kΩ load; for example, a 1 kΩ resistor load at each IF output, plus a differential 2 kΩ load consisting of the input impedance of the IF filter or the input impedance of the matching network for the IF filter. The power gain refers to the available power on this 2 kΩ load. The path to V_{CC} for the DC current should be achieved via tuning inductors. The output voltage is limited to $V_{CC} + 3V_{be}$ or 3 diode forward voltage drops.

Fast switching, **on/off**, of the receive section is controlled by the hardware input RXON.

Fig.3 Block diagram, receive section.
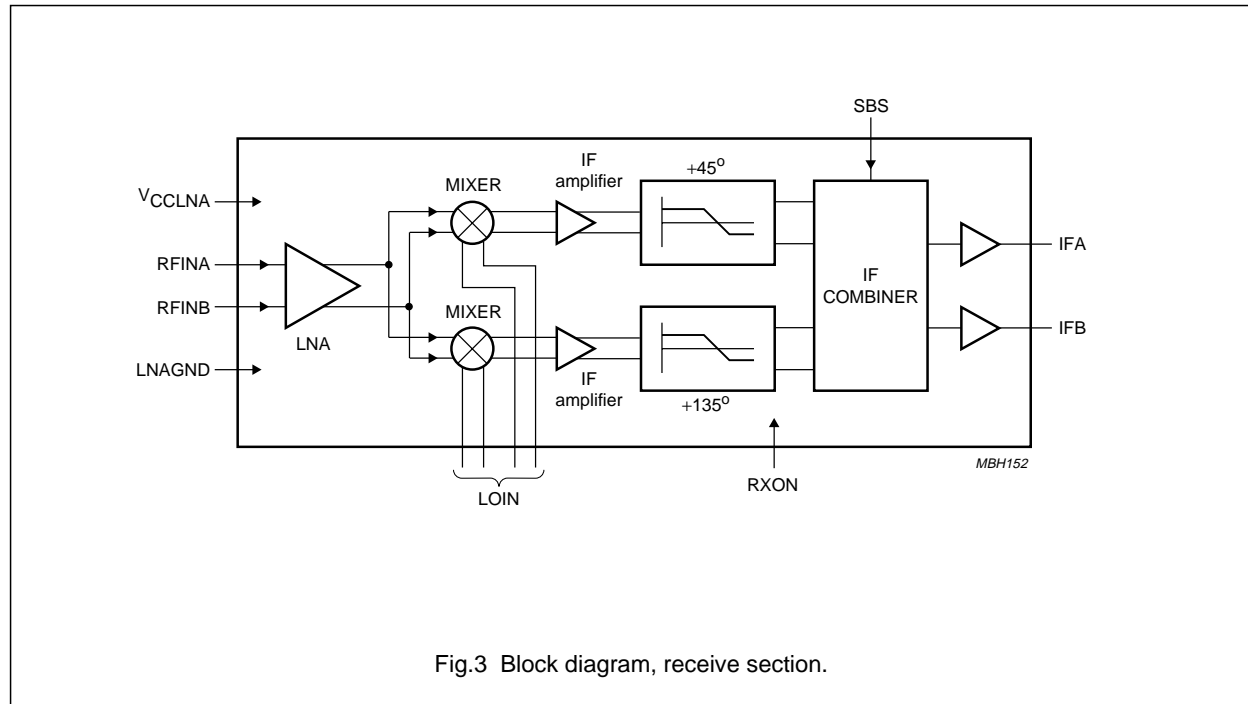
Local oscillator section

The local oscillator (LO) input directly drives the two internal all-pass networks to provide quadrature LO to the receive mixers.

The centre frequency of the receive band is adjustable by the voltage on pin V_{QUADLO}. This should be achieved by connecting a resistor between V_{QUADLO} and V_{CC}. Over 25 dB of image rejection can be obtained by an optimum resistor value.

A synthesizer-on (SX) mode is used to power-up the LO input buffers, thus minimizing the pulling effect on the external VCO when entering receive mode. This mode is active when SXON = 1.

There are no internal biassing components attached to the pins LOINA and LOINB. These pins are connected by capacitors to the internal phase shifting network.

Fig.4 Block diagram, LO section.
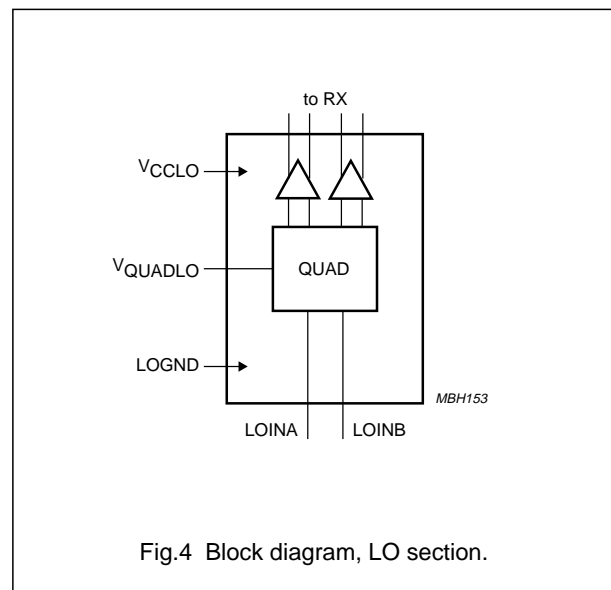
Table 1 Control of power status

EXTERNAL PIN LEVEL		CIRCUIT MODE OF OPERATION
RXON	**SXON**	
LOW	LOW	power-down mode
HIGH	X	RX mode (receive and LO sections **on**)
LOW	HIGH	SX mode (only LO section **on**)

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–	9	V
ΔGND	difference in ground supply voltage applied between LOGND and LNAGND	–	0.6	V
$P_{I(max)}$	maximum power input	–	20	dBm
$T_{j(max)}$	maximum operating junction temperature	–	150	°C
P_{max}	maximum power dissipation	–	250	mW
T_{stg}	IC storage temperature	–65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	120	K/W

HANDLING

Every pin withstands the ESD test in accordance with *"MIL-STD-883C Class 2 (method 3015.5)"*.

DC CHARACTERISTICS

V_{CC} = 4.0 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins V_{CCLNA} and V_{CCLO}						
V_{CC}	supply voltage	T_{amb} = 0 to +70 °C	3.15	4.0	5.3	V
		over full temperature range	3.6	4.0	5.3	V
$I_{CC(RX)}$	supply current in RX mode		21.5	26.5	33.5	mA
$I_{CC(PD)}$	supply current in power-down mode		–	0.2	50	μA
$I_{CC(SX)}$	supply current in SX mode		3	5	7	mA
Pins RXON, SXON and SBS						
V_{th}	CMOS threshold voltage	note 1	–	1.25	–	V
V_{IH}	HIGH level input voltage		$0.7V_{CC}$	–	V_{CC}	V
V_{IL}	LOW level input voltage		–0.3	–	+0.8	V
I_{IH}	HIGH level static input current	pin at V_{CC} – 0.4 V	–1	–	+1	μA
I_{IL}	LOW level static input current	pin at 0.4 V	–1	–	+1	μA

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins RFINA and RFINB						
V_I	DC input voltage level	receive section **on**	–	2.0	–	V
Pins IFA and IFB						
I_O	DC output current	receive section **on**	–	2.5	–	mA

Note

1. The referenced inputs should be connected to a valid CMOS input level.

AC CHARACTERISTICS

V_{CC} = 4.0 V; T_{amb} = −30 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receive section (receive section enabled)						
R_{iRX}	RF input resistance (real part of the parallel input impedance)	balanced; at 1890 MHz	–	60	–	Ω
C_{iRX}	RF input capacitance (imaginary part of the parallel input impedance)	balanced; at 1890 MHz	–	1	–	pF
f_{iRX}	RF input frequency		1880	–	1900	MHz
RL_{iRX}	return loss on matched RF input	balanced; note 1	11	15	–	dB
G_{CP}	conversion power gain	differential RF inputs to differential IF outputs loaded to 1 kΩ differential	17	20	23	dB
G_{rip}	gain ripple as a function of RF frequency	note 2	–	0.2	–	dB
$\Delta G/T$	gain variation with temperature	T_{amb} = −30 to +25 °C; note 2	−20	0	+10	mdB/°C
		T_{amb} = +25 to +85 °C; note 2	−40	−30	−20	mdB/°C
$CP1_{RX}$	1 dB compression point	differential RF inputs to differential IF outputs; note 1	−26	−23	–	dBm
DES3	3 dB desensitisation point	interferer frequency offset: 3 MHz; differential RF inputs to differential IF outputs; note 1	–	−30	–	dBm
		interferer frequency offset: 20 MHz; differential RF inputs to differential IF outputs; note 1	–	−28	–	dBm
$IP2D_{RX}$	2nd order intercept point	differential RF inputs to differential IF outputs; note 2	15	30	–	dBm
$IP3_{RX}$	3rd order intercept point	differential RF inputs to differential IF outputs; note 2	−23	−17	–	dBm
NF_{RX}	overall noise figure	differential RF inputs to differential IF outputs; notes 2 and 3	–	4.3	5.0	dB

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Z_{LRX}	typical application IF output load impedance	balanced	–	1	–	kΩ
RL_{oRX}	return loss on matched IF output	balanced; note 1	11	15	–	dB
f_{oRX}	IF frequency		–	110	–	MHz
IR	rejection of image frequency	$f_{LO} < f_{RF}$; f_{IF} = 110 MHz; note 4	26	32	–	dB
Local oscillator section (receive section enabled)						
f_{iLO}	LO input frequency		1770	–	2010	MHz
R_{iLO}	LO input resistance (real part of the parallel input impedance)	balanced; at 1780 MHz	–	40	–	Ω
C_{iLO}	LO input capacitance (imaginary part of the parallel input impedance)	balanced; at 1780 MHz	–	2	–	pF
RL_{iLO}	return loss on matched LO input (including power-down mode)	note 1	9	12	–	dB
ΔRL_{iLO}	return loss variation ratio between SX and RX modes	linear S_{11} variation; note 1	–	5	–	mU
P_{iLO}	LO input power level		–6	–3	+3	dBm
RI_{LO}	reverse isolation	LOIN to RFIN at LO frequency; note 2	40	–	–	dB
Timing						
t_{start}	start-up time of each block		1	5	20	μs

Notes

1. Measured and guaranteed only on UAA2077AM demonstration board at T_{amb} = 25 °C.

2. Measured and guaranteed only on UAA2077AM demonstration board.

3. This value includes printed-circuit board and balun losses.

4. Measured and guaranteed only on UAA2077AM demonstration board at T_{amb} = 25 °C. V_{QUADLO} open-circuit.

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INTERNAL PIN CONFIGURATION

SYMBOL	PIN	DC VOLTAGE (V)	EQUIVALENT CIRCUIT
V_{CCLNA}	3	4.0	
RFINA	5	2.0	
RFINB	6	2.0	
LNAGND	8	0	
SXON	9	–	
SBS	11	–	
RXON	12	–	
LOINB	13	–	
LOINA	14	–	
V_{CCLO}	15	4.0	
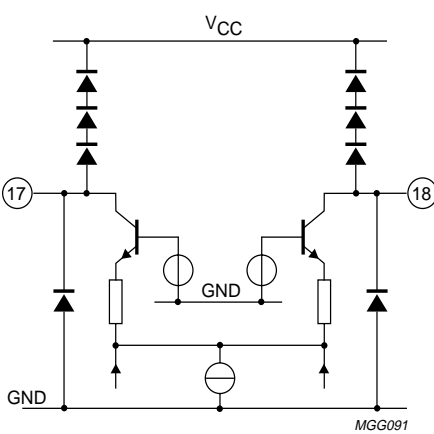
SYMBOL	PIN	DC VOLTAGE (V)	EQUIVALENT CIRCUIT
LOGND	16	0	
IFA	17	2.5	
IFB	18	2.5	

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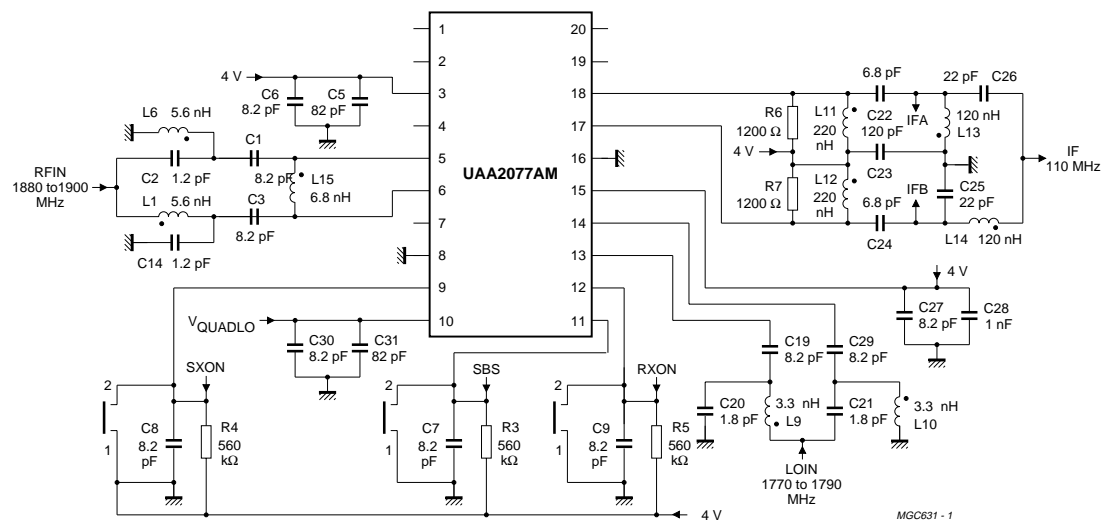
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APPLICATION INFORMATION

Figure 5 illustrates the electrical diagram of the UAA2077AM Philips demonstration board for DECT applications. All matching is to 50 Ω for measurement purposes. Different values will be used in a real application.
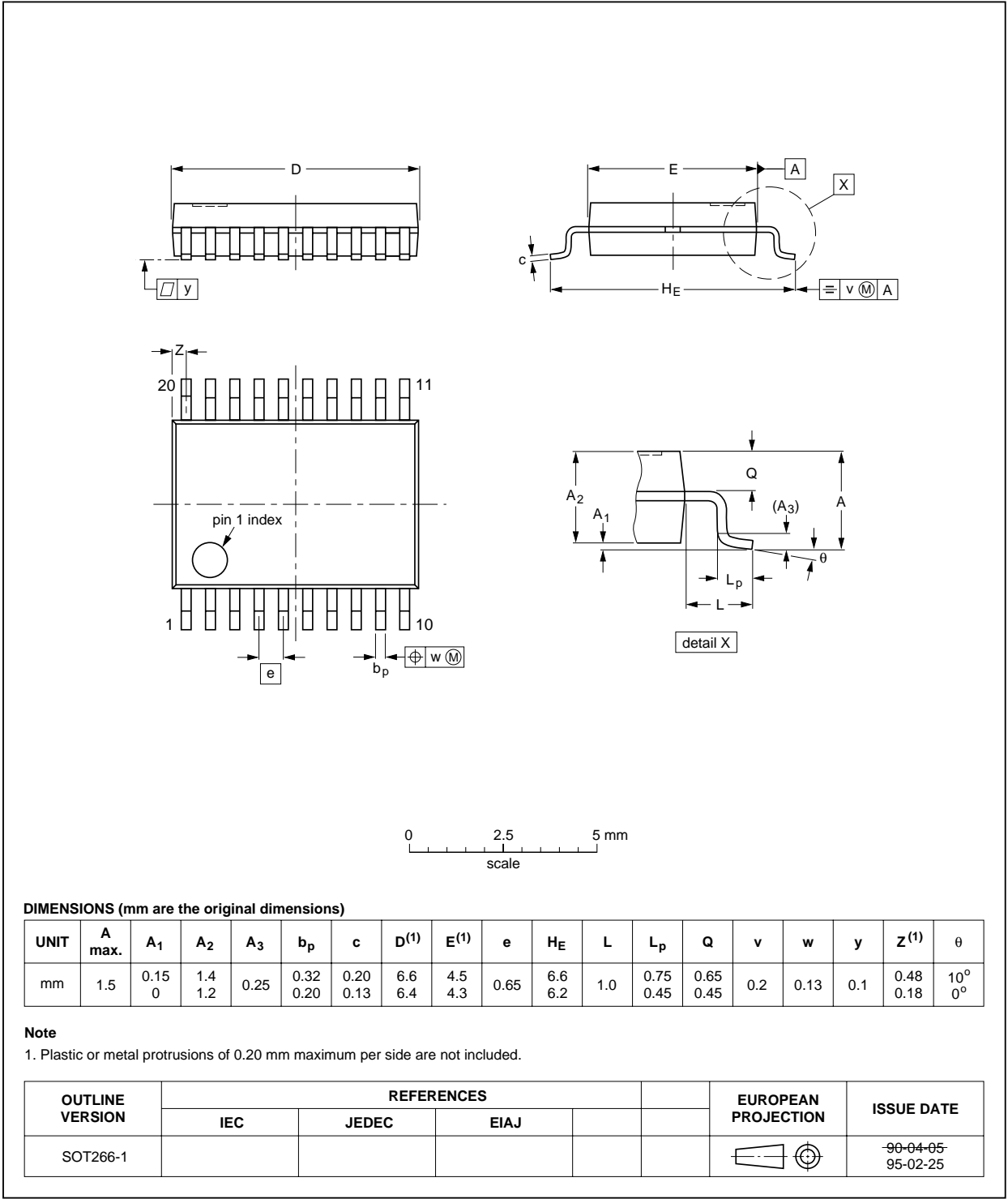
Fig.5 Application diagram.

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PACKAGE OUTLINE

SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm

SOT266-1

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0	1.4 1.2	0.25	0.32 0.20	0.20 0.13	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT266-1						~~90-04-05~~ 95-02-25

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SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for SSOP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.**

Even with these conditions, only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381, Fax. +1 708 296 8556

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 1949

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 615 800, Fax. +358 615 80920

France: 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 52 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS,
Tel. +30 1 4894 339/911, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Shivsagar Estate, A Block, Dr. Annie Besant Rd.
Worli, MUMBAI 400 018, Tel. +91 22 4938 541, Fax. +91 22 4938 722

Indonesia: see Singapore

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, TEL AVIV 61180,
Tel. +972 3 645 0444, Fax. +972 3 648 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +1 800 234 7381, Fax. +1 708 296 8556

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 83749, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 926 5361, Fax. +7 095 564 8323

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Rua do Rocio 220, 5th floor, Suite 51,
04552-903 São Paulo, SÃO PAULO - SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 829 1849

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 632 2000, Fax. +46 8 632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2686, Fax. +41 1 481 7730

Taiwan: PHILIPS TAIWAN Ltd., 23-30F, 66,
Chung Hsiao West Road, Sec. 1, P.O. Box 22978,
TAIPEI 100, Tel. +886 2 382 4443, Fax. +886 2 382 4444

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 2A Akademika Koroleva str., Office 165,
252148 KIEV, Tel. +380 44 476 0297/1642, Fax. +380 44 476 6991

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381, Fax. +1 708 296 8556

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 825 344, Fax.+381 11 635 777

For all other countries apply to: Philips Semiconductors, Marketing & Sales Communications, Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825   **Internet:** http://www.semiconductors.philips.com/ps/

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