DATA SHEET

UAA2068G
Transmit chain and synthesizer with integrated VCO for DECT

Product specification
Supersedes data of 1998 Jan 07
File under Integrated Circuits, IC17

1998 Nov 19

Philips Semiconductors

Transmit chain and synthesizer with integrated VCO for DECT

UAA2068G

FEATURES

- Economical integrated solution for frequency generation in DECT cordless telephones
- Integrated low phase noise 950 MHz VCO with frequency doubler
- Local Oscillator (LO) drive (–14 dBm) for RF mixer circuit
- Dedicated DECT PLL synthesizer
- 3-line serial interface bus
- 3 dBm output preamplifier with an integrated switch
- Low current consumption from 3 V supply
- Compatible with Philips Semiconductors ABC baseband chip (PCD509x series).

APPLICATIONS

- 1880 to 1920 MHz DECT cordless telephones.

GENERAL DESCRIPTION

The UAA2068G BiCMOS device integrates a 950 MHz VCO, a frequency doubler, main and reference dividers and a phase comparator, to implement a phase-locked loop for DECT channel frequencies. The 1.9 GHz signal is buffered and switched, in TX mode, to drive the transmit power amplifier (CGY20xx series) or, in RX mode, to be used as an LO signal for the receiver mixer IC (UAA2078).

The synthesizer's main divider is driven by the frequency doubler output in the range from 1880 to 1920 MHz and programmed via a 3-wire serial bus.

The reference divider ratio is fixed at 8. Outputs of the main and reference dividers drive a phase comparator where a charge pump produces phase error current pulses for integration in an external loop filter. Only a passive loop filter is necessary. The charge-pump current (phase comparator gain) is set by an external resistor at pin R_{SET}.

The VCO is powered from an internally regulated voltage source and includes internal varicap diodes. Its tuning range is wider than the required band to allow for production spreads. In a TDMA system such as DECT, the VCO and the synthesizer are switched on one slot before the required one to lock the VCO to the required channel frequency. Just before the required slot, the synthesizer is switched off, allowing open-loop modulation of the VCO during transmission. When opening the loop, the frequency pulling (due to switching off the synthesizer) can be maintained within the DECT specification.

The device is designed to operate from 3 NiCd cells in pocket phones, with low current and nominal 3.6 V supplies. Separate power and ground pins are provided to the different parts of the circuit. The ground leads should be short-circuited externally to prevent large currents flowing across the die and thus causing damage.
All supply pins (V_{CC}) must also be at the same potential, except $V_{CC(CP)}$ which can be equal to or greater than the other supply pins (e.g. V_{CC} = 3 V and $V_{CC(CP)}$ = 5 V for wider VCO control voltage range).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA2068G	LQFP32	plastic low profile quad flat package; 32 leads; body 5 × 5 × 1.4 mm	SOT401-1

QUICK REFERENCE DATA

V_{CC} = 3.6 V; $V_{CC(CP)}$ = 3.6 V; T_{amb} = 25 °C; unless otherwise specified. Characteristics for which only a typical value is given are not tested.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	general supply voltage		3.0	3.6	5.2	V
$V_{CC(CP)}$	charge-pump supply voltage	$V_{CC(CP)} \geq V_{CC}$	3.0	3.6	5.2	V
$I_{CC(SYA)}$ + $I_{CC(SYD)}$	synthesizer supply current	S_EN = 1	–	9.5	14	mA
$I_{CC(VCO)}$ + $I_{CC(BUF)}$	VCO and buffer parts supply current	VCO_ON = 1	–	9.5	14	mA
$I_{CC(DBL)}$	doubler supply current	in RX mode	–	14.4	19	mA
		in TX mode	–	10	14	mA
$I_{CC(AMP)}$	TX preamplifier supply current	in RX mode	–	0	50	µA
		in TX mode	–	24	32	mA
$I_{CC(pd)}$	total supply current in power-down mode		–	5	50	µA
$f_{o(RF)}$	RF output frequency		1880	–	1920	MHz
f_{xtal}	crystal reference input frequency		–	13.824	–	MHz
f_{PC}	phase comparator frequency		–	1728	–	kHz
T_{amb}	operating ambient temperature		–10	–	+60	°C

BLOCK DIAGRAM

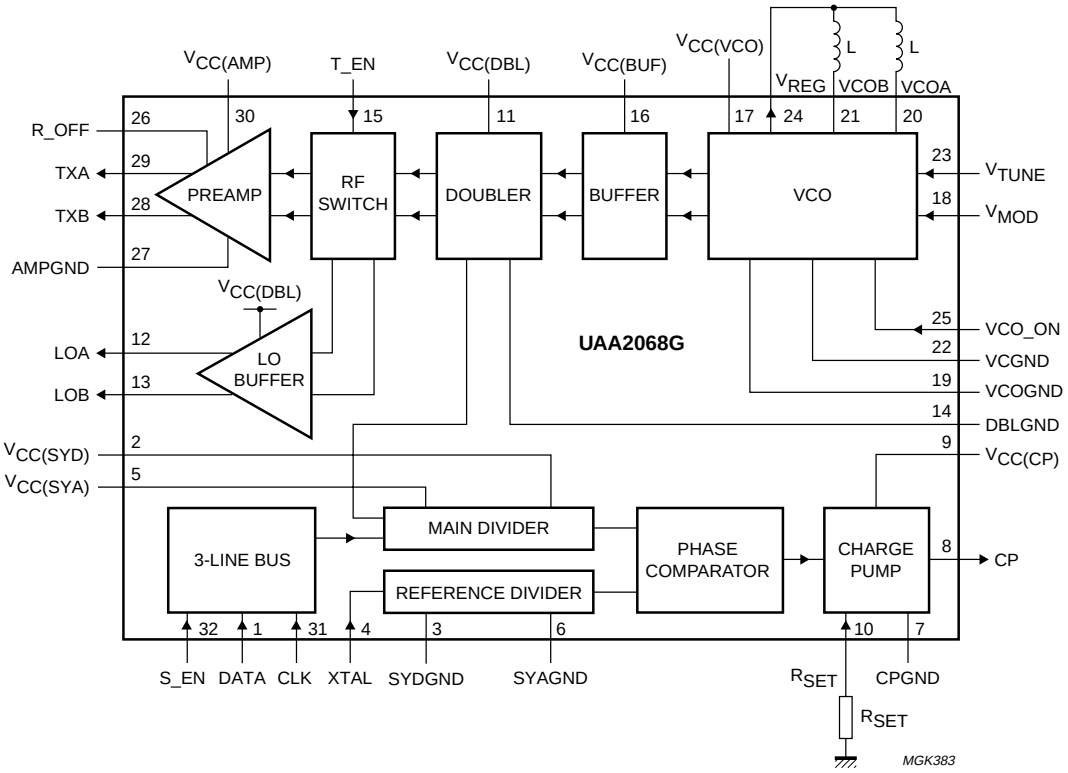


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
DATA	1	3-wire programming bus data input
$V_{CC(SYD)}$	2	synthesizer CMOS divider positive supply voltage
SYDGND	3	synthesizer CMOS divider ground
XTAL	4	reference frequency input
$V_{CC(SYA)}$	5	synthesizer prescaler positive supply voltage
SYAGND	6	synthesizer prescaler ground
CPGND	7	charge-pump ground
CP	8	charge-pump output signal
$V_{CC(CP)}$	9	charge-pump positive supply voltage
R_{SET}	10	charge-pump current setting input
$V_{CC(DBL)}$	11	doubler positive supply voltage
LOA	12	local oscillator output A
LOB	13	local oscillator output B
DBLGND	14	doubler ground
T_EN	15	transmit enable signal input
$V_{CC(BUF)}$	16	VCO isolation buffer positive supply voltage
$V_{CC(VCO)}$	17	VCO positive supply voltage
V_{MOD}	18	transmit modulation input
VCOGND	19	VCO ground; note 1
VCOA	20	VCO inductor connection A
VCOB	21	VCO inductor connection B
VCGND	22	internal varicap ground; note 1
V_{TUNE}	23	VCO tuning input
V_{REG}	24	VCO regulator output
VCO_ON	25	VCO power on control input; note 2
R_OFF	26	power on control for RX LO buffer/TX preamplifier; note 3
AMPGND	27	transmit amplifier ground
TXB	28	transmit amplifier output B
TXA	29	transmit amplifier output A
$V_{CC(AMP)}$	30	transmit amplifier positive supply voltage
CLK	31	3-wire programming bus clock input
S_EN	32	synthesizer enable signal input

Notes

1. Pins 19 and 22 are internally short-circuited.
2. Use with S_PWR on ABC baseband chip.
3. Use with R_PWR on ABC baseband chip.

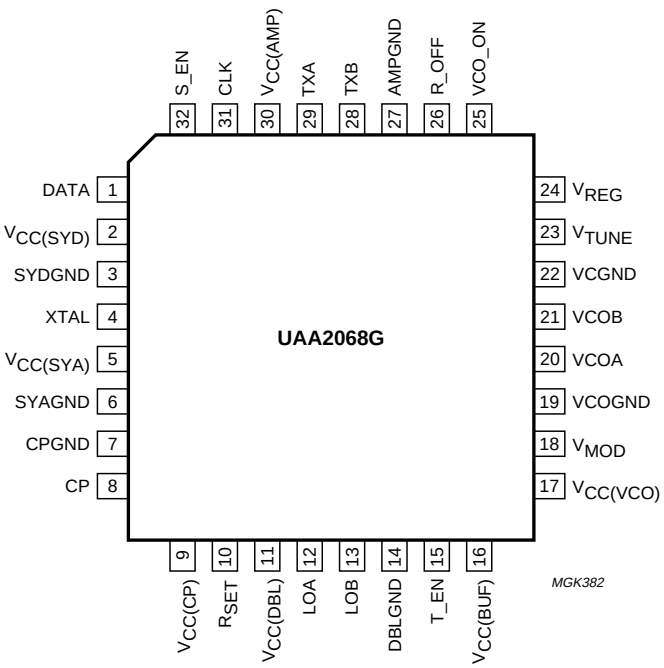


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Transmit chain

VCO, BUFFER AND FREQUENCY DOUBLER

The VCO operates at a nominal centre frequency of 950 MHz. It is fully integrated apart from two inductors which complete the resonator network. This VCO operates from an on-chip regulated power supply (V_{REG}), which minimizes frequency disturbances due to variations in supply voltage. The buffered VCO signal is fed into a frequency doubler. The large difference between the transmitted and VCO frequencies reduces transmitter-oscillator coupling problems.

The output of the doubler is used to drive the synthesizer main divider and can also be switched to either the TX preamplifier or the RX LO output buffer. The high isolation obtained from the VCO buffer and the frequency doubler ensures very small frequency changes when turning on the TX preamplifier or the RX LO output buffer. In TX mode, the oscillator can be directly modulated with GMSK filtered data at pin V_{MOD}.

RF SWITCH

The RF switch passes the doubled VCO signal to either the TX preamplifier (when T_EN is HIGH) or to the RX LO buffer (when T_EN is LOW). In TX mode, the difference in the RF power levels, observed at the TX output when T_EN is switched from LOW-to-HIGH, is typically 40 dB.

TX PREAMPLIFIER

The TX preamplifier amplifies the RF signal up to a level of 3 dBm which is suitable for use with Philips Semiconductors DECT power amplifiers such as the CGY20xx series. It is powered-up when both R_OFF and VCO_ON are HIGH.

RX LO BUFFER

The RX LO buffer outputs the frequency doubled VCO signal at a level of −14 dBm. This signal can then be used as the local oscillator drive for the receive mixers of devices such as the UAA2078. The buffer is powered-up when R_OFF is LOW and VCO_ON is HIGH.

Synthesizer

Main divider

The main divider is clocked by the RF signal from the internal frequency doubler. The divider operates at frequencies from 1880 to 1920 MHz. It consists of a bipolar prescaler followed by a CMOS counter. Any main divider ratio from 1024 to 1151 inclusive can be programmed.

Reference divider

The reference divider is clocked by the signal at pin XTAL. The circuit operates with levels from 50 to 500 mV (RMS) at a frequency of 13.824 MHz, with a fixed divider ratio of 8.

Phase comparator

The phase comparator is driven by the output of the main and reference dividers. It produces current pulses at pin CP. The pulse duration is equal to the difference in time of arrival of the edges from the two dividers. If the main divider edge arrives first, CP sinks current. If the reference divider edge arrives first, CP sources current. The DC value of the charge-pump current is nominally ten times the current drawn by the external resistor connected to pin R_{SET}. Additional circuitry is included to ensure that the gain of the phase detector remains linear even for small phase errors.

The charge pump has a separate supply, $V_{CC(CP)}$, which helps to reduce the interference on the charge-pump output from other parts of the circuit. $V_{CC(CP)}$ can be higher than the other supply voltages if a wider range on the VCO input is required. The $V_{CC(CP)}$ voltage must not be less than that on other V_{CC} pins.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. These 3 lines are data (DATA), clock (CLK) and enable (S_EN). The data sent to the device is loaded in bursts framed by S_EN. Programming clock edges and their appropriate data bits are ignored until S_EN goes active LOW. The programmed information is read directly by the main divider when S_EN returns HIGH. During synthesizer operation, S_EN should be kept HIGH.
In normal operating mode, only the last 8 bits serially clocked into the device are retained within the register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The data format is shown in Table 2. The first bit entered is b7, the last bit is b0.

For the divider ratio, the first bit (b6) entered is the most significant (MSB).

S_EN must be LOW to capture new programming data. S_EN must be HIGH to switch on the synthesizer.

Operating modes

The synthesizer is on when the input signal S_EN is HIGH, and off when S_EN is LOW. When turned on, the dividers and phase detector are synchronized to avoid a random initial phase error. When turned off, the phase detector is synchronized with the dividers to avoid interrupting a charge-pump pulse.

The VCO is on when the input signal VCO_ON is HIGH. The polarity of VCO_ON is chosen for compatibility with output S_PWR at the ABC chip. When turned on, it needs some time (typically 30 μs) to reach its steady state.

The TX preamplifier is on when both R_OFF and VCO_ON are HIGH. The polarity of R_OFF is chosen for compatibility with output R_PWR at the ABC chip. When turned on, it needs some time (typically 10 μs) to reach its steady state. In transmit mode, the timing of the R_OFF LOW-to-HIGH transition can be chosen such that the TX preamplifier is turned on while the synthesizer loop remains closed thus avoiding frequency pulling of the VCO. In the receive mode, depending on the exact timing of R_OFF compared to VCO_ON, the TX preamplifier can be switched on at the beginning of the previous slot, but is switched off when the R_OFF goes LOW; this occurs when the synthesizer loop is closed. The LO output amplifier is turned on when R_OFF is LOW and VCO_ON is HIGH.

The UAA2068G has a very low current consumption in power-down mode.

Table 1 Mode control; note 1

BLOCK STATUS	VCO_ON	R_OFF	T_EN	S_EN
VCO, buffer, doubler, RF switch, TX preamplifier and LO buffer powered-down	0	X	X	X
VCO, buffer, doubler, RF switch and TX preamplifier powered-up	1	1	1	X
LO buffer powered-down				
Nominal RF signal at TX output				
VCO, buffer, doubler, RF switch and TX preamplifier powered-up	1	1	0	X
LO buffer powered-down				
No RF signal output				
VCO, buffer, doubler, RF switch and LO buffer powered-up	1	0	0	X
TX preamplifier powered-down				
Nominal RF signal at LO buffer output				
VCO, buffer, doubler, RF switch and LO buffer powered-up	1	0	1	X
TX preamplifier powered-down				
No RF signal output				
To power-down PLL blocks; notes 2 and 3	1	X	X	0
To power-up PLL blocks; notes 2 and 3	1	X	X	1
All blocks in power-down state; notes 2 and 3	0	X	X	0
New PLL division ratio is loaded and the PLL blocks are powered-up on the rising edge of S_EN; note 3	1	X	X	0 to 1

Notes

1. X = don’t care.
2. PLL blocks are the main divider, reference divider, phase detector and charge pump.
3. A reference signal is needed on pin XTAL for correct operation.

Table 2 Bit allocation; notes 1 and 2

FIRST IN	REGISTER BIT ALLOCATION														LAST IN
DATA FIELD															
b15[3]	b14[3]	b13[3]	b12[3]	b11[3]	b10[3]	b9[3]	b8[3]	b7[4]	b6[5]	b5	b4	b3	b2	b1	b0
X	X	X	X	X	X	X	X	0	main divider programming[6]						

Notes

1. X = don't care.
2. In normal operation, only 8 bits are programmed into the register.
3. For normal operation, b15 to b8 do not need to be programmed.
4. The validation bit (b7) must be programmed with zero for normal operation.
5. Bit b6 is the MSB of the main divider coefficient.
6. The main divider ratio is equal to 1024 plus the programmed value (see Table 3).

Table 3 Main divider programming

b6	b5	b4	b3	b2	b1	b0	MAIN DIVIDER RATIO	SYNTHESIZED FREQUENCY (MHz)
Binary equivalent of n							1024 + n	1.728 × (1024 + n)
1	0	0	0	0	0	1	1089	1881.792
1	0	0	1	0	1	0	1098	1897.344

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.3	+5.5	V
$V_{CC(CP)}$	charge-pump supply voltage		–0.3	+5.5	V
$V_{CC(CP)} - V_{CC}$	difference in voltage between $V_{CC(CP)}$ and V_{CC}		–0.3	+5.5	V
ΔGND	difference in ground supply voltage applied between all ground pins	note 1	–	0.3	V
P_{tot}	total power dissipation		–	275	mW
T_{stg}	storage temperature		–55	+125	°C
T_{amb}	operating ambient temperature		–10	+60	°C
T_j	junction temperature		–	150	°C

Note

1. Pins short-circuited internally must be short-circuited externally.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	100	K/W

CHARACTERISTICS

V_{CC} = 3.6 V; $V_{CC(CP)}$ = 3.6 V; T_{amb} = 25 °C; unless otherwise specified. Characteristics for which only a typical value is given are not tested.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CC}	supply voltage		3	3.6	5.2	V
$V_{CC(CP)}$	charge-pump supply voltage	$V_{CC(CP)} \geq V_{CC}$	3	3.6	5.2	V
$I_{CC(SYA)}$ + $I_{CC(SYD)}$	synthesizer supply current	S_EN = 1	–	9.5	14	mA
$I_{CC(VCO)}$ + $I_{CC(BUF)}$	VCO and buffer parts supply current	VCO_ON = 1	–	9.5	14	mA
$I_{CC(DBL)}$	doubler supply current	in RX mode	–	14.4	19	mA
		in TX mode	–	10	14	mA
$I_{CC(AMP)}$	TX preamplifier supply current	in RX mode	–	0	50	µA
		in TX mode	–	24	32	mA
$I_{CC(pd)}$	total supply current in power-down mode		–	5	50	µA
Synthesizer main divider						
f_{RF}	RF frequency		1880	–	1920	MHz
R_m	main divider ratio		1024	–	1151	
Synthesizer reference divider input						
f_{xtal}	crystal reference input frequency		–	13.824	–	MHz
$V_{xtal(rms)}$	sinusoidal input signal level (RMS value)		50	–	500	mV
R_{ref}	reference division ratio		–	8	–	
R_i	input resistance (real part of the input impedance)	f_{xtal} = 13.824 MHz	–	4.5	–	kΩ
C_i	input capacitance (imaginary part of the input impedance)		–	2.5	–	pF
Phase detector						
f_{PC}	phase comparator frequency		–	1728	–	kHz
Charge-pump output						
$I_{o(cp)}$	charge-pump output current	V_{CP} = ½V_{CC}; R_{SET} = 8.2 kΩ	–	1.5	–	mA
$I_{o(cp)(err)}$	charge-pump output current error	note 1	–25	–	+25	%
I_{match}	sink-to-source current matching	V_{CP} = ½V_{CC}	–	±5	–	%
$I_{L(cp)}$	charge-pump-off leakage current	V_{CP} = ½V_{CC}	–1	0	+1	nA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Charge-pump current setting resistor input; pin R_{SET}						
R_{SET}	external resistor connected between pin R_{SET} and ground		5.6	–	12	kΩ
V_{SET}	regulated voltage at pin R_{SET}		–	1.2	–	V
VCO						
f_{VCO}	oscillator frequency	over full temperature range; note 2	940	–	960	MHz
G_{VCO}	tuning input VCO gain		–	45	–	MHz/V
G_{MOD}	modulation input VCO gain		–	1	–	MHz/V
Switch part						
$FTLO_{TXoff}$	isolation between LO and TX outputs when TX preamplifier is off (RX mode)	f = 1890 MHz; note 2	–	–50	–	dB
$FTLO_{TXon}$	isolation due to the switch when TX preamplifier is on (TX mode)	f = 1890 MHz; note 2	–	–40	–	dB
TX preamplifier and LO buffer parts						
$P_{o(TX)}$	TX preamplifier output power	over full temperature range; note 2	0	3	7	dBm
$f_{o(TX)}$	output frequency on TX preamplifier or LO buffer		1880	–	1920	MHz
$R_{o(TX)}$	TX preamplifier output resistance (real part of the parallel output impedance)	balanced	–	150	–	Ω
$C_{o(TX)}$	TX preamplifier output capacitance (imaginary part of the parallel output impedance)	balanced	–	0.5	–	pF
$FTVCO_{TX}$	VCO frequency feedthrough at the TX output	referenced to the $f_{o(TX)}$ level; note 2	–	–41	–36	dBc
CNR_{25}	carrier-to-noise ratio at TX output	carrier offset Δf = 25 kHz	–	–75	–	dBc/Hz
CNR_{4686}	carrier-to-noise ratio at TX output	carrier offset Δf = 4686 kHz	–	–135	–132	dBc/Hz
$\Delta f_{o(offset)}$	total frequency shift due to 200 mV V_{CC} change disabling the synthesizer	note 2 measured 20 μs after disabling the synthesizer	–	–	±15	kHz
$\Delta f_{o(drift)}$	frequency drift during a slot	note 2	–	1	± 10	kHz
$P_{o(LO)}$	LO preamplifier output power	note 2	–	–14	–	dBm
$R_{o(LO)}$	LO preamplifier output resistance (real part of the parallel output impedance)	balanced	–	120	–	Ω
$C_{o(LO)}$	LO preamplifier output capacitance (imaginary part of the parallel output impedance)	balanced	–	0	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Interface logic input signal levels; pins DATA, CLK, S_EN, T_EN, R_OFF and VCO_ON						
V_{IH}	HIGH-level input voltage	note 3	2.2	–	V_{CC} + 0.3	V
V_{IL}	LOW-level input voltage		–0.3	–	+0.5	V
I_{bias}	input bias current	logic 1 or logic 0	–5	–	+5	μA
C_i	input capacitance		–	2	–	pF

Notes

1. Condition: $0.5 < V_{CP} < (V_{CC(CP)} - 0.5)$.
2. Measured and guaranteed only on the Philips evaluation board, including PCB and balun filter.
3. V_{IH} should never exceed 5.2 V.

SERIAL BUS TIMING CHARACTERISTICS

V_{CC} = 3.6 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r	input rise time	–	10	40	ns
t_f	input fall time	–	10	40	ns
T_{cy}	clock period	100	–	–	ns
Enable programming; S_EN					
t_{START}	delay to rising clock edge	40	–	–	ns
t_{END}	delay from last falling clock edge	–20	–	–	ns
t_W	minimum inactive pulse width	4000	–	–	ns
$t_{SU;S\_EN}$	enable set-up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	input data to clock hold time	20	–	–	ns

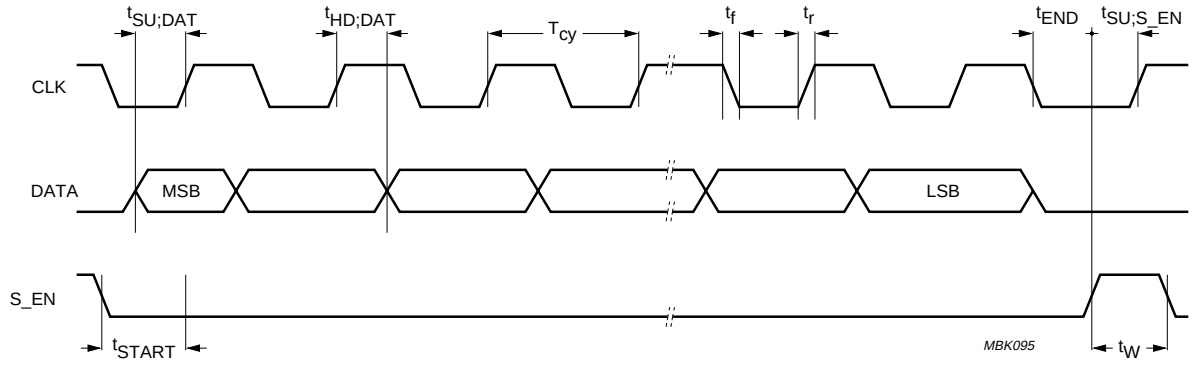
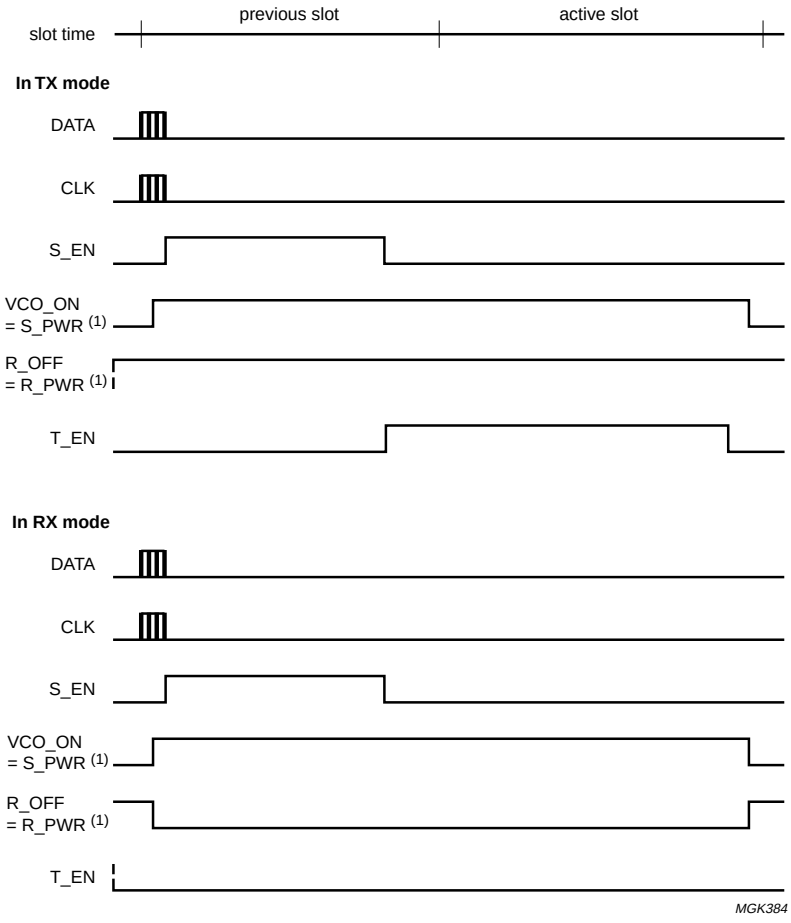


Fig.3 Serial bus timing diagram.

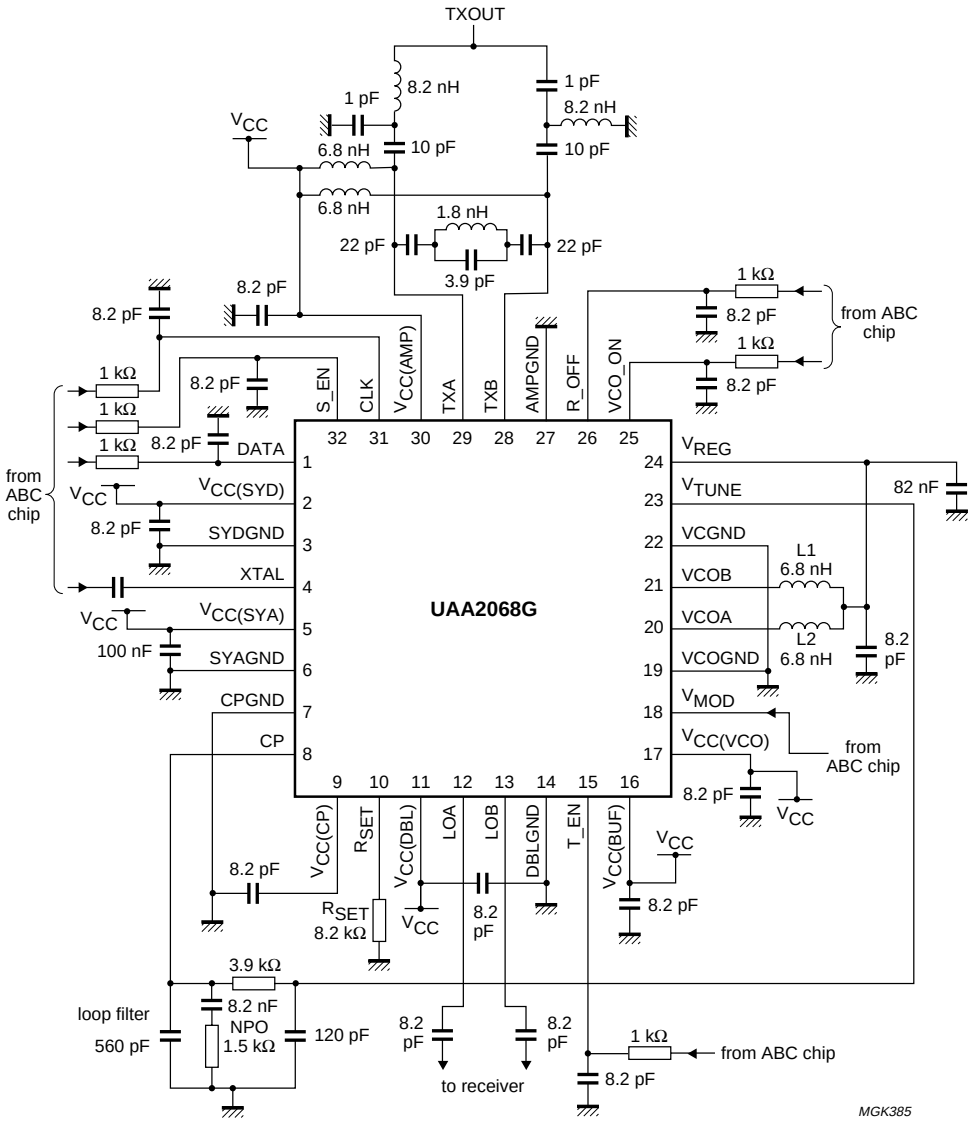
TIMING CHARACTERISTICS



(1) On ABC baseband chip.

Fig.4 Application bus timing diagram.

APPLICATION INFORMATION

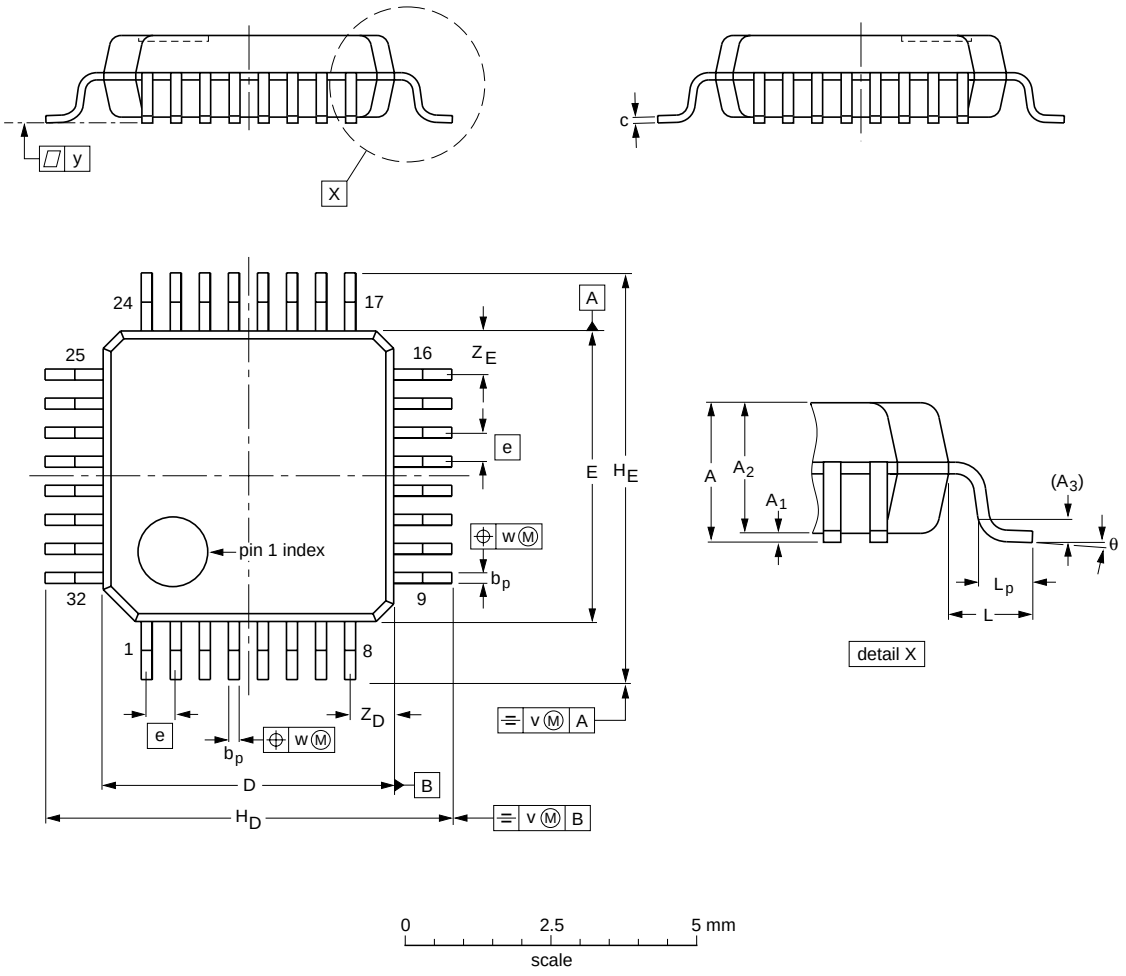


L1 and L2: order of magnitude.
Values depend on board layout.

Fig.5 Typical application diagram.

PACKAGE OUTLINE

LQFP32: plastic low profile quad flat package; 32 leads; body 5 x 5 x 1.4 mm **SOT401-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.15 0.05	1.5 1.3	0.25	0.27 0.17	0.18 0.12	5.1 4.9	5.1 4.9	0.5	7.15 6.85	7.15 6.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT401-1						~~95-12-19~~ 97-08-04

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

NOTES

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