

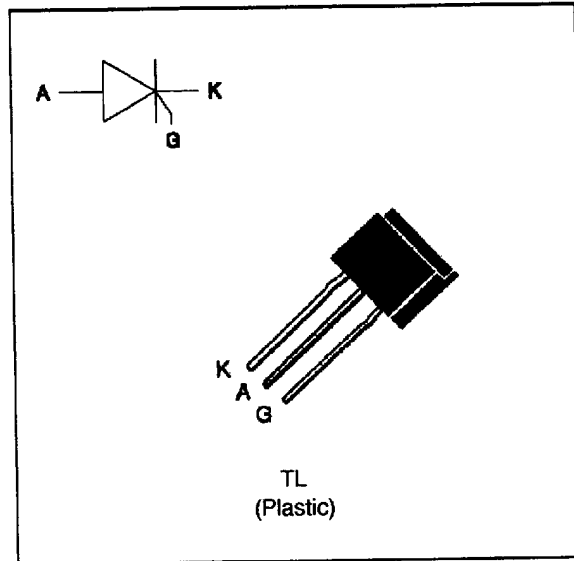
**SENSITIVE GATE SCR**

**FEATURES**

- LOW  $I_{GT} \leq 200 \mu A$
- LOW  $I_H \leq 5 mA$
- $I_T(RMS) = 4 A$

**DESCRIPTION**

The TLS 106 Silicon Controlled Rectifiers are high performance MESA diffused PNP devices glass passivated sensitive gate technology. These parts are intended to general purpose switching and phase control application.



**ABSOLUTE RATINGS (limiting values)**

Symbol	Parameter		Value	Unit
$I_T(RMS)$	RMS on-state current (180° conduction angle)	$T_I = 25^\circ C$	4	A
$I_T(AV)$	Average on-state current (180° conduction angle, single phase circuit)	$T_I = 25^\circ C$	2.5	A
$I_{TSM}$	Non repetitive surge peak on-state current ( $T_J$ initial = 25°C)	$t_p = 8.3 ms$	37	A
		$t_p = 10 ms$	35	
$i^2t$	$i^2t$ value	$t_p = 10 ms$	6	A <sup>2</sup> s
$di/dt$	Critical rate of rise of on-state current Gate supply : $I_G = 10 mA$ $di_G/dt = 0.1 A/\mu s$		100	A/ $\mu s$
$T_{stg}$ $T_J$	Storage and operating junction temperature range		- 40 to + 150	°C
			- 40 to + 110	°C
$T_I$	Maximum lead temperature for soldering during 4 s at 4.5 mm from case		230	°C

Symbol	Parameter	TLS 106-					Unit
		05	1	2	4	6	
$V_{DRM}$ $V_{RRM}$	Repetitive peak off-state voltage $T_J = 110^\circ C$ $R_{GK} = 1 K\Omega$	50	100	200	400	600	V

**THERMAL RESISTANCES**

Symbol	Parameter	Value	Unit
Rth (j-a)	Junction to ambient on printed circuit with Cu surface 1cm <sup>2</sup>	50	°C/W
Rth (j-l) DC	Junction to leads for DC	15	°C/W

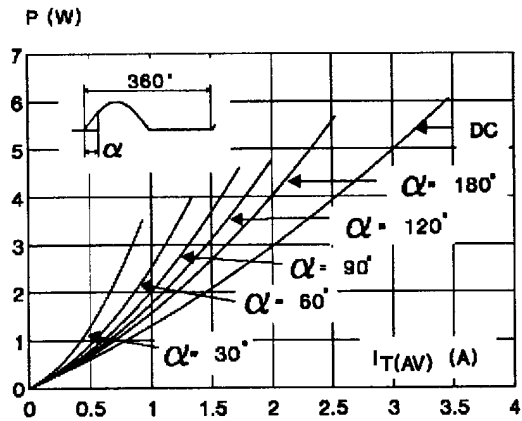
**GATE CHARACTERISTICS (maximum values)**

P<sub>G</sub> (AV) = 0.2W P<sub>GM</sub> = 3W (tp = 20 μs) I<sub>FGM</sub> = 1.2A (tp = 20 μs) V<sub>RGM</sub> = 5 V.

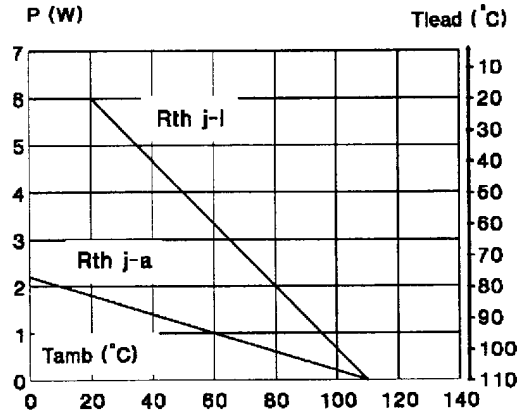
**ELECTRICAL CHARACTERISTICS**

Symbol	Test Conditions	Value	Unit
I <sub>GT</sub>	V <sub>D</sub> =12V (DC) R <sub>L</sub> =140Ω T <sub>J</sub> =25°C	MAX	0.2 mA
V <sub>GT</sub>	V <sub>D</sub> =12V (DC) R <sub>L</sub> =140Ω T <sub>J</sub> =25°C	MAX	1 V
V <sub>GD</sub>	V <sub>D</sub> =V <sub>DRM</sub> R <sub>L</sub> =3.3kΩ R <sub>GK</sub> =1kΩ T <sub>J</sub> =110°C	MIN	0.1 V
t <sub>gt</sub>	V <sub>D</sub> =V <sub>DRM</sub> I <sub>G</sub> =10mA dI <sub>G</sub> /dt = 0.1A/μs T <sub>J</sub> =25°C	TYP	1.5 μs
I <sub>L</sub>	I <sub>G</sub> =1mA R <sub>GK</sub> =1kΩ T <sub>J</sub> =25°C	MAX	7 mA
I <sub>H</sub>	I <sub>T</sub> =50mA R <sub>GK</sub> =1kΩ T <sub>J</sub> =25°C	MAX	5 mA
V <sub>TM</sub>	I <sub>TM</sub> =4A tp=380μs T <sub>J</sub> =25°C	MAX	1.9 V
I <sub>DRM</sub> I <sub>RRM</sub>	V <sub>DRM</sub> Rated R <sub>GK</sub> =1kΩ V <sub>RRM</sub> Rated R <sub>GK</sub> =1kΩ	T <sub>J</sub> =25°C T <sub>J</sub> =110°C	MAX 0.01 0.3 mA
dV/dt	Linear slope up to V <sub>D</sub> =67%V <sub>DRM</sub> R <sub>GK</sub> =1kΩ C <sub>GK</sub> =0.1μF T <sub>J</sub> =110°C	MIN	10 V/μs
t <sub>q</sub>	V <sub>D</sub> =67%V <sub>DRM</sub> I <sub>TM</sub> =4A V <sub>R</sub> =10V dI <sub>TM</sub> /dt=10 A/μs dV <sub>D</sub> /dt=2V/μs R <sub>GK</sub> =1kΩ T <sub>J</sub> =110°C	TYP	100 μs

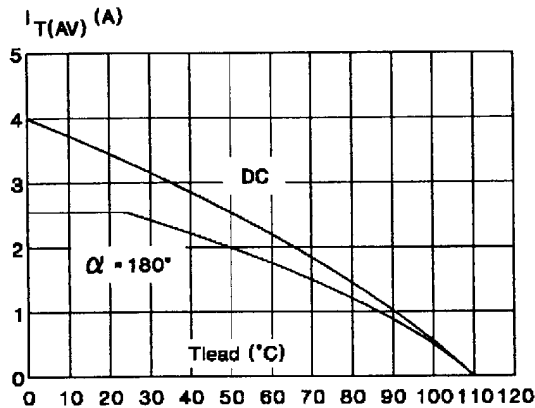
**Fig.1 :** Maximum average power dissipation versus average on-state current.



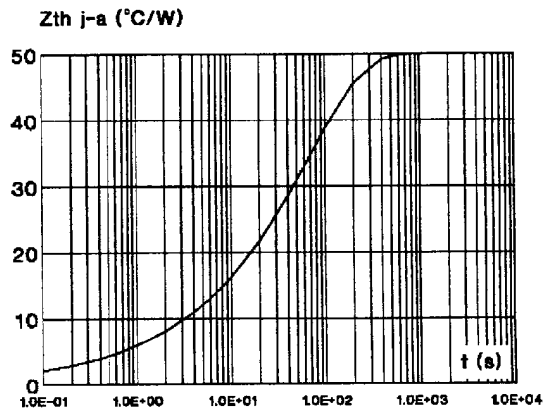
**Fig.2 :** Correlation between maximum average power dissipation and maximum allowable temperatures ( $T_{amb}$  and  $T_{lead}$ ).



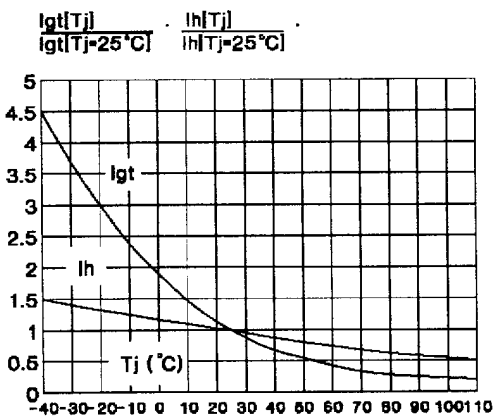
**Fig.3 :** Average on-state current versus leads temperature.



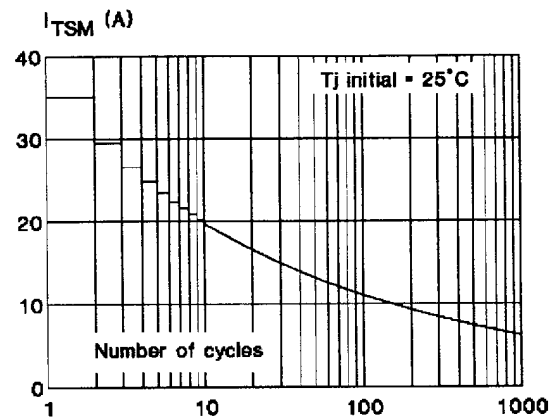
**Fig.4 :** Thermal transient impedance junction to ambient versus pulse duration.



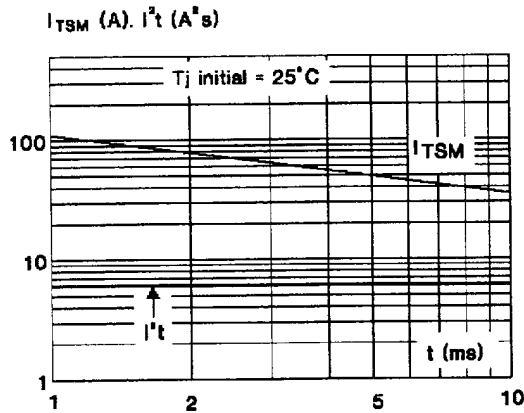
**Fig.5 :** Relative variation of gate trigger current versus junction temperature.



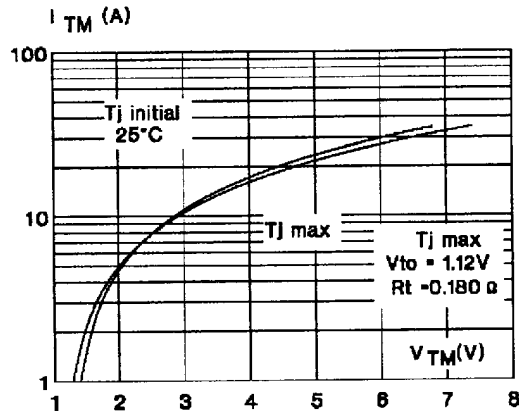
**Fig.6 :** Non repetitive surge peak on-state current versus number of cycles.



**Fig.7** : Non repetitive surge peak on-state current for a sinusoidal pulse with width :  $t \leq 10$  ms, and corresponding value of  $I^2t$ .

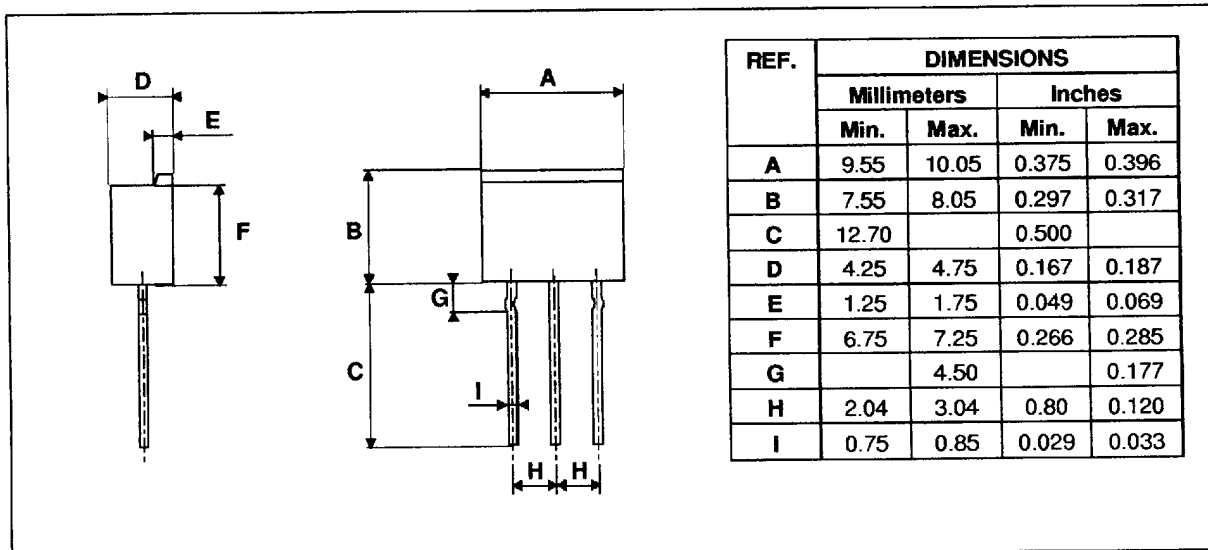


**Fig.8** : On-state characteristics (maximum values).



**PACKAGE MECHANICAL DATA**

TL Plastic



Marking : type number  
Weight : 0.8 g

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