Peak 2.5A Sink/Source Bus Termination Regulator

Description

The AP1260MP is a simple, cost-effective and high-speed linear regulator designed to generate termination voltage in double data rate (DDR) memory system to comply with the JEDEC SSTL_2 and SSTL_18 or other specific interfaces such as HSTL, SCSI-2 and SCSI-3 etc. devices requirements. The regulator is capable of actively sinking or sourcing up to 2.5A transient peak current while regulating an output voltage to within 40mV. The output termination voltage can be tightly regulated to track 1/2VDDQ by two external voltage divider resistors or the desired output voltage can be programmed by externally forcing the REFEN pin voltage.

The AP1260MP also incorporates a high-speed differential amplifier to provide ultra-fast response in line/load transient. Other features include extremely low initial offset voltage, excellent load regulation, current limiting in bi-directions and on-chip thermal shut-down protection.

The AP1260MP are available in the ESOP-8 (Exposed Pad) surface mount packages.

Features

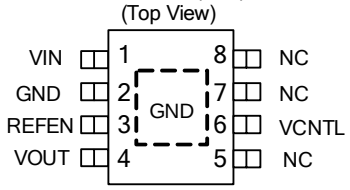
- Ideal for DDR-I, DDR-II and DDR-III V_{TT} Applications
- Sink and Source peak 2.5A for DDRI, DDRII and DDRIII.
- Integrated Power MOSFETs
- Generates Termination Voltage for SSTL_2, SSTL _18, HSTL, SCSI-2 and SCSI-3 Interfaces.
- High Accuracy Output Voltage at Full-Load
- Output Adjustment by Two External Resistors
- Low External Component Count
- Shutdown for Suspend to RAM (STR) Functionality with High-Impedance Output
- Current Limiting Protection
- On-Chip Thermal Protection
- Available in ESOP-8 (Exposed Pad) Packages
- V_{IN} and V_{CNTL} No Power Sequence Issue
- 100% Lead (Pb)-Free

Application

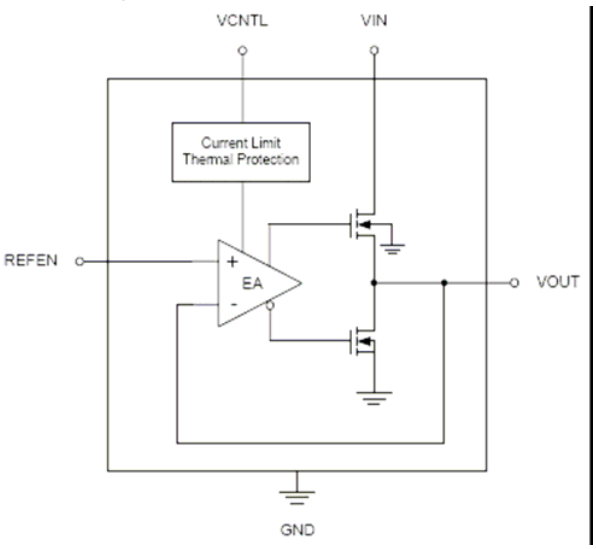
- Desktop PCs, Notebooks, and Workstations
- Graphics Card Memory Termination
- Set Top Boxes, Digital TVs, Printers
- Embedded Systems
- Active Termination Buses
- DDR-I, DDR-II & DDRIII Memory Systems

Pin Configuration

ESOP-8 (MP)
(Top View)



Block Diagram



Pin Description

Pin Name	Pin function
V_{IN}	Power Input
GND	Ground
V_{CNTL}	Gate Drive Voltage
REFEN	Reference Voltage input and Chip Enable
V_{OUT}	Output Voltage

Absolute Maximum Rating (1)

Parameter	Symbol	Value	Unit
Input Voltage	V_{IN}	6	V
Control Voltage	V_{CNTL}	6	V
Power Dissipation	P_D	Internally Limited	--
ESD Rating	--	2	KV
Storage Temperature Range	T_S	-65 to 150	°C
Lead Temperature (Soldering, 5 sec.)	T_{LEAD}	260	°C
Package Thermal Resistance	Θ_{JC}	28	°C/W

Operating Rating(2)

Parameter	Symbol	Value	Units
Input Voltage	V_{IN}	2.5V to 1.5V ±3%	V
Control Voltage	V_{CNTL}	5.0 or 3.3 ±5%	V
Ambient Temperature	T_A	-40 to +85	℃
Junction Temperature	T_J	-40 to +125	℃

Electrical Characteristics

V_{IN}=1.8V, V_{CNTL}=3.3V, V_{REFEN}=0.9V, C_{OUT}=10μF (Ceramic)), T_A=25°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input						
V_{CNTL} Operation Current	I_{CNTL}	I_{OUT}=0A	--	1	3	mA
Standby Current	I_{STBY}	V_{REFEN} < 0.2V (Shutdown),R_{LOAD} = 180Ω	--	50	90	μA
Output						
Output Offset Voltage(3)	V_{OS}	I_{OUT}= 0A	-20	--	+20	mV
Load Regulation(4)	ΔV_{LOAD}	I_{OUT}= +2A	-20	--	+20	
		I_{OUT}= -2A				
Protection						
Current limit	I_{LIM}		2.5	--	--	A
Thermal Shutdown Temperature	T_{SD}	3.3V ≤ V_{CNTL} ≤ 5V	--	170	--	℃
Thermal Shutdown Hysteresis	ΔT_{SD}	3.3V ≤ V_{CNTL} ≤ 5V	--	35	--	
REFEN Shutdown						
Shutdown Threshold	V_{IH}	Enable	0.6	--	--	V
	V_{IL}	Shutdown	--	--	0.2	

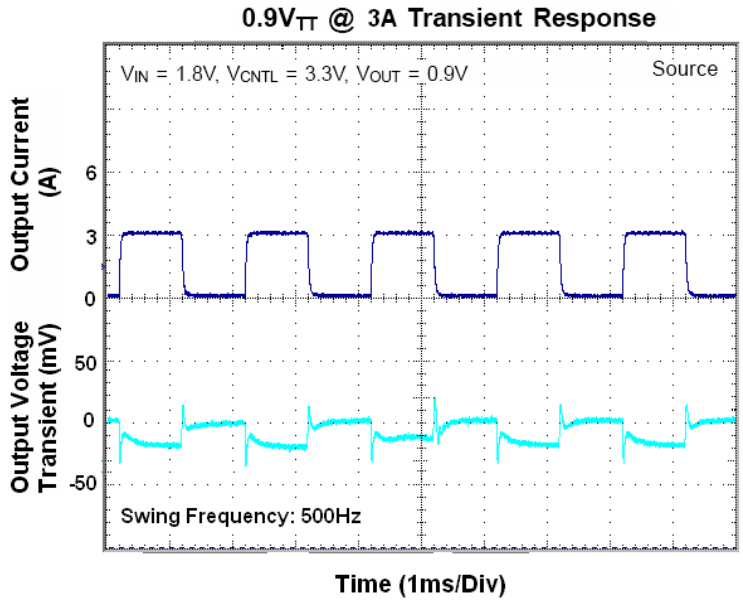
Note 1: Exceeding the absolute maximum rating may damage the device.

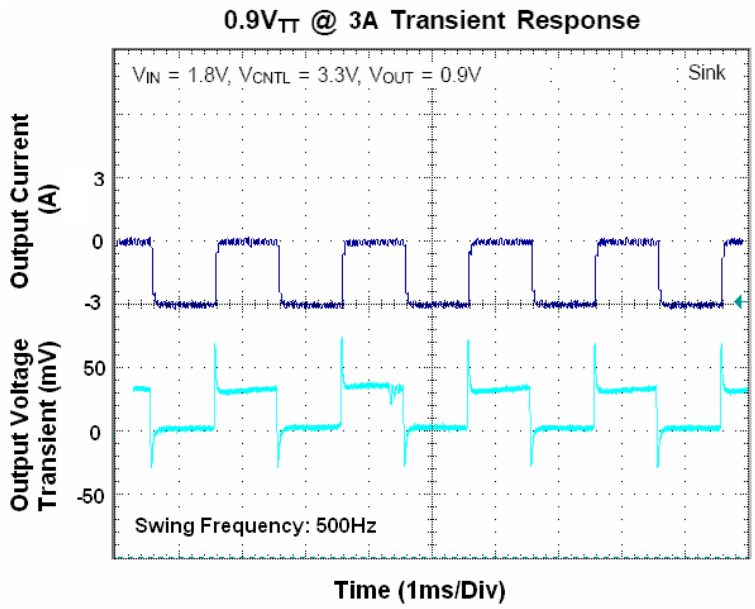
Note 2: V_{OS} offset is the voltage measurement defined as V_{OUT} subtracted from V_{REFEN}

Note 3: V_{OS} offset is the voltage measurement defined as V_{OUT} subtracted from V_{REFEN}.

Note 4: Regulation is measured at constant junction temperature by using a 5ms current pulse. Devices are tested for load regulation in the load range from 0A to 2A.

Typical Operating Characteristics





Application Information

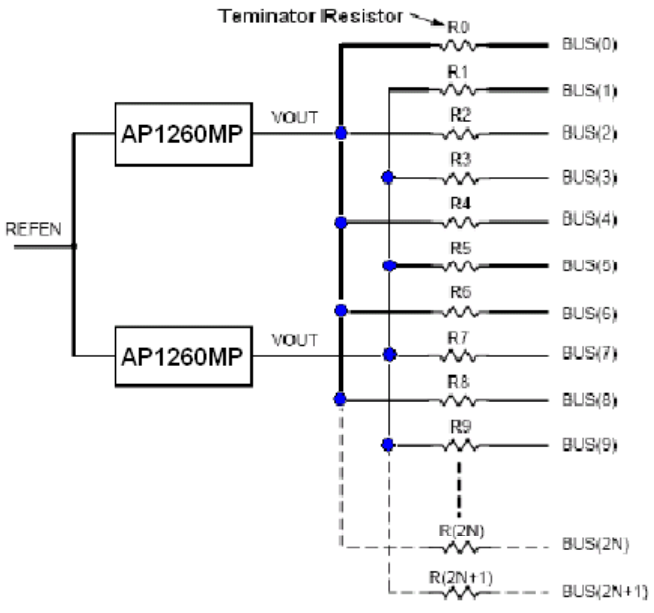
Input Capacitor and Layout Consideration

Place the input bypass capacitor as close as possible to the AP1260MP. A low ESR capacitor larger than 470uF is recommended for the input capacitor. Use short and wide traces to minimize parasitic resistance and inductance.

Inappropriate layout may result in large parasitic inductance and cause undesired oscillation between AP1260MP and the preceding powe converter.

Consideration while designs the resistance of voltage divider

Make sure the sinking current capability of pull-down NMOS if the lower resistance was chosen so that the voltage on V_{REFEN} is below 0.2V. In addition, the capacitor and voltage divider form the lowpass filter. There are two reasons doing this design; one is for output voltage soft-start while another is for noise immunity.



Thermal Consideration

AP1260MP regulators have internal thermal limiting circuitry designed to protect the device during overload conditions.For continued operation, do not exceed maximum operation junction temperature 125℃. The power dissipation definition in device is:

$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula:

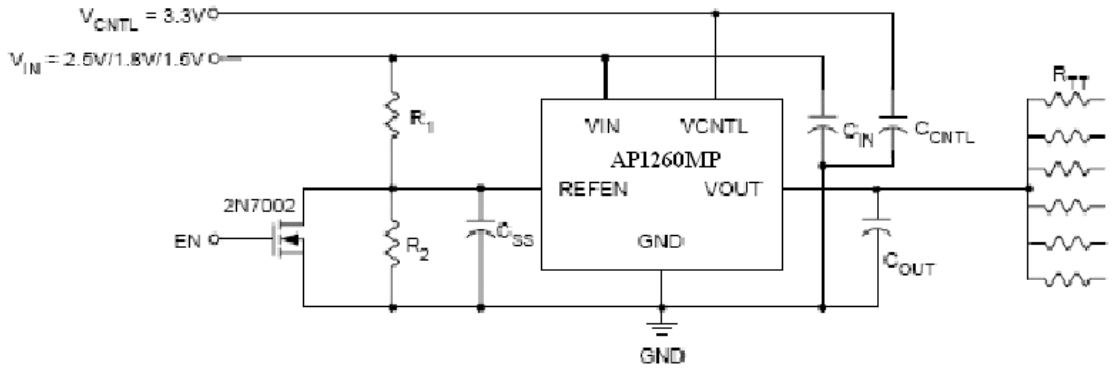
$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \Theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125℃, T_A is the ambient temperature and the Θ_{JA} is the junction to ambient thermal resistance. The junction to ambient thermal resistance (Θ_{JA} is layout dependent) for ESOP-8 package (Exposed Pad) is 75℃/W on standard JEDEC 51-7 (4 layers, 2S2P) thermal test board. The maximum power dissipation at T_A = 25℃ can be calculated by following formula:

$P_{D(MAX)} = (125℃ - 25℃) / 75℃/W = 1.33W$

The thermal resistance Θ_{JA} of ESOP-8 (Exposed Pad) is determined by the package design and the PCB design. However, the package design has been decided. If possible, it's useful to increase thermal performance by the PCB design. The thermal resistance can be decreased by adding copper under the expose pad of ESOP-8 package. We have to consider the copper couldn't stretch infinitely and avoid the tin overflow.

Application Diagram



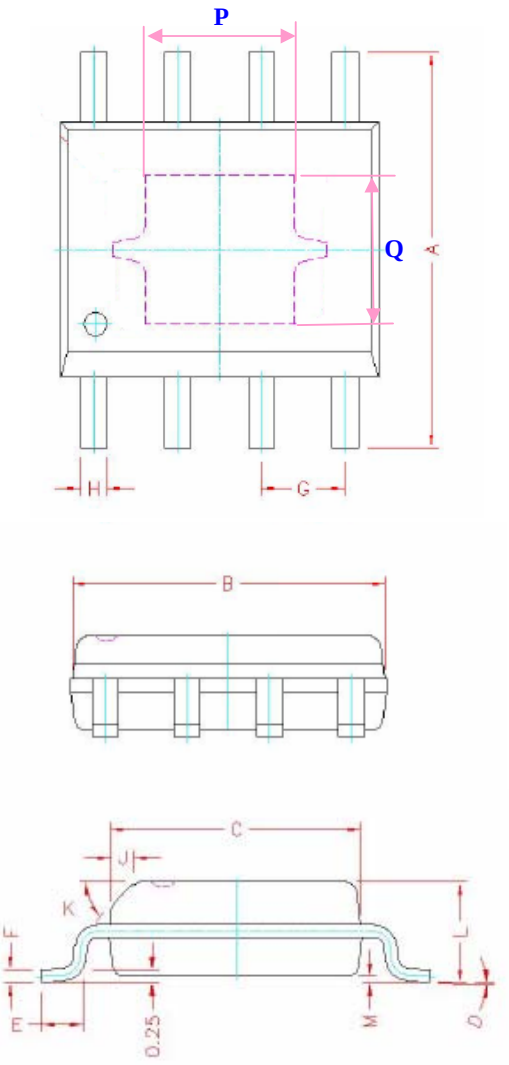
$R_1 = R_2 = 100K\Omega$, $R_{TT} = 50\Omega/33\Omega/25\Omega$

$C_{OUT, min}$ = 10µF (Ceramic) + 1000µF under the worst case testing condition

R_{DUMMY} = 1kΩ as for VOUT discharge when VIN is not present but VCNTL is present

C_{SS} = 1µF, C_{IN} = 470µF(Low ESR), C_{CNTL} = 47µF

Package Outline : ESOP-8



	Millimeters		
SYMBOLS	MIN	NOM	MAX
A	5.80	6.00	6.20
B	4.80	4.90	5.00
C	3.80	3.90	4.00
D	0°	4°	8°
E	0.40	0.65	0.90
F	0.19	0.22	0.25
M	0.00	0.08	0.15
H	0.35	0.42	0.49
L	1.35	1.55	1.75
J	0.375 REF.		
K	45°		
G	1.27 TYP.		
P	2.15	2.25	2.35
Q	2.15	2.25	2.35

1.All Dimension Are In Millimeters.

2.Dimension Does Not Include Mold Protrusions.

Part Marking Information & Packing : ESOP-8