

### Features

- Dual USB port power switches
- Over-current and thermal protection
- 0.8A accurate current limiting
- Reverse Current Blocking
- 90mΩ on-resistance
- Input voltage range: 2.7V – 5.5V
- 0.6ms typical rise time
- Very low shutdown current: 1uA (max)
- Fault report (FLG) with blanking time (7ms typ)
- ESD protection: 6KV HBM, 300V MM
- Active high (AP2146) or active low (AP2156) enable
- Ambient temperature range -40°C to 85°C
- SOP-8L and MSOP-8L-EP (Exposed Pad): Available in "Green" Molding Compound (No Br, Sb)
- Lead Free Finish / RoHS Compliant (Note 1)
- UL Recognized, File Number E322375
- IEC60950-1 CB Scheme Certified

### Description

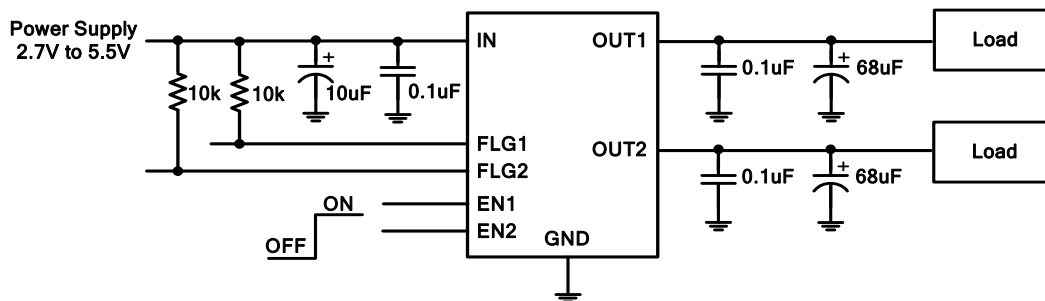
The AP2146 and AP2156 are integrated high-side power switches optimized for Universal Serial Bus (USB) and other hot-swap applications. The family of devices complies with USB 2.0 and available with both polarities of Enable input. They offer current and thermal limiting and short circuit protection as well as controlled rise time and under-voltage lockout functionality. A 7ms deglitch capability on the open-drain Flag output prevents false over-current reporting and does not require any external components.

All devices are available in SOP-8L and MSOP-8L-EP packages.

### Applications

- Consumer electronics – LCD TV & Monitor, Game Machines
- Communications – Set-Top-Box, GPS, Smartphone
- Computing – Laptop, Desktop, Servers, Printers, Docking Station, HUB

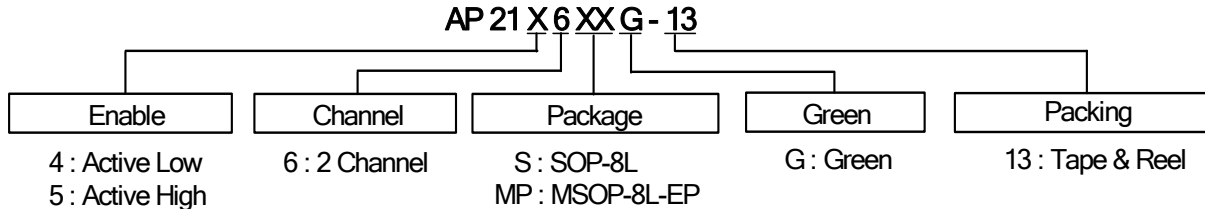
### Typical Application Circuit



### Available Options

Part Number	Channel	Enable Pin (EN)	Current Limit (Typical)	Recommended Maximum Continuous Load Current
AP2146	2	Active Low	0.8A	0.5A
AP2156	2	Active High	0.8A	0.5A

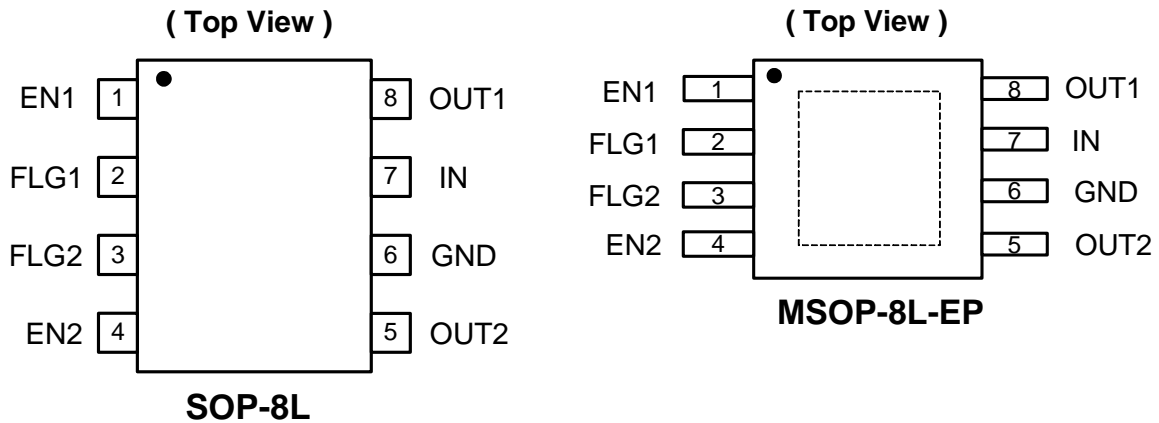
### Ordering Information



Device	Package Code	Packaging (Note 2)	13" Tape and Reel	
			Quantity	Part Number Suffix
AP21X6SG-13	S	SOP-8L	2500/Tape & Reel	-13
AP21X6MPG-13	MP	MSOP-8L-EP	2500/Tape & Reel	-13

Notes: 1. EU Directive 2002/95/EC (RoHS). All applicable RoHS exemptions applied. Please visit our website at [http://www.diodes.com/products/lead\\_free.html](http://www.diodes.com/products/lead_free.html)  
 2. Pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at <http://www.diodes.com/datasheets/ap02001.pdf>.

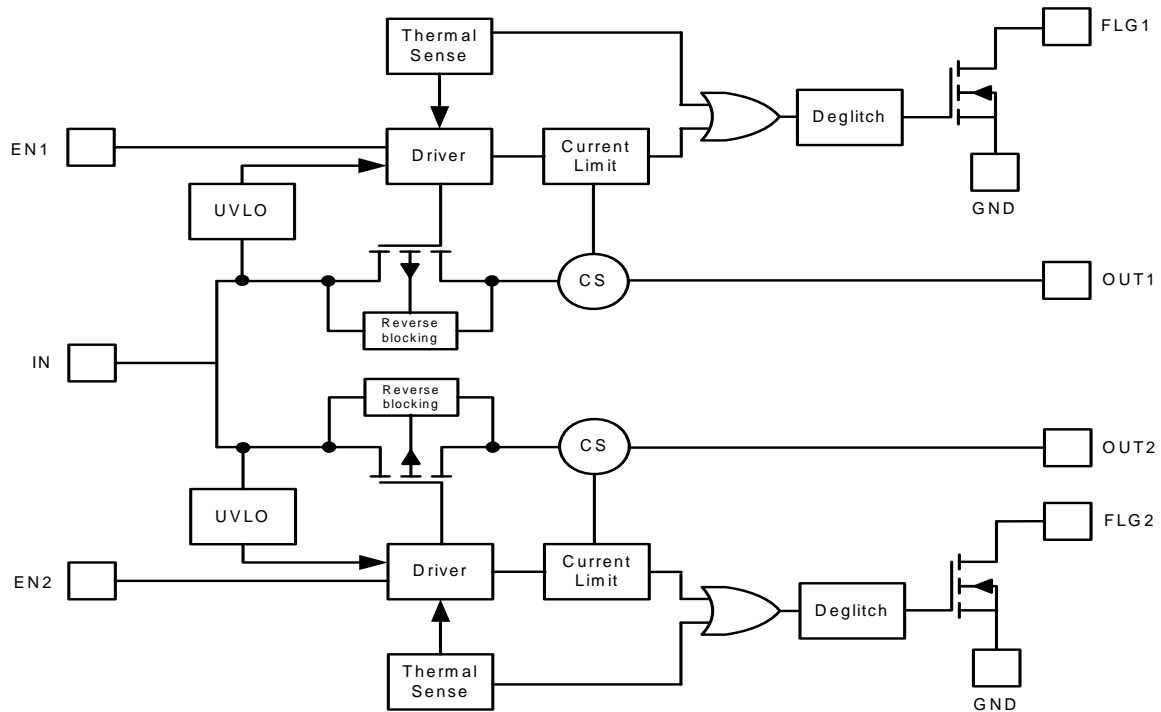
### Pin Assignment



### Pin Descriptions

Pin Name	Pin Number	Descriptions
EN1	1	Switch 1 enable input, active low (AP2146) or active high (AP2156)
FLG1	2	Switch 1 over-current and over-temperature fault report, open-drain
FLG2	3	Switch 2 over-current and over-temperature fault report, open-drain
EN2	4	Switch 2 enable input, active low (AP2146) or active high (AP2156)
OUT2	5	Switch 2 voltage output pin
GND	6	Ground
IN	7	Voltage input pin
OUT1	8	Switch 1 voltage output pin

### Functional Block Diagram



### Absolute Maximum Ratings

Symbol	Parameter	Ratings	Units
ESD HBM	Human Body Model ESD Protection	6	KV
ESD MM	Machine Model ESD Protection	300	V
$V_{IN}$	Input Voltage	6.5	V
$V_{OUT}$	Output Voltage	$V_{IN} + 0.3$	V
$V_{EN}, V_{FLG}$	Enable Voltage	6.5	V
$I_{load}$	Maximum Continuous Load Current	Internal Limited	A
$T_{Jmax}$	Maximum Junction Temperature	150	°C
$T_{ST}$	Storage Temperature Range (Note 3)	-65 ~ 150	°C

Notes: 3. UL Recognized Rating from -30°C to 70°C

### Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
$V_{IN}$	Input voltage	2.7	5.5	V
$I_{OUT}$	Output Current	0	500	mA
$T_A$	Operating Ambient Temperature	-40	85	°C

### Electrical Characteristics

( $T_A = 25^\circ\text{C}$ ,  $C_{IN} = 10\mu\text{F}$ ,  $V_{IN} = +5.0\text{V}$ , unless otherwise stated)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$V_{UVLO}$	Input UVLO	$R_{load} = 1\text{k}\Omega$	1.6	1.9	2.5	V
$I_{SHDN}$	Input Shutdown Current	Disabled, $I_{OUT} = 0$		0.5	1	$\mu\text{A}$
$I_Q$	Input Quiescent Current, Dual	Enabled, $I_{OUT} = 0$		95	140	$\mu\text{A}$
$I_{LEAK}$	Input Leakage Current	Disabled, OUT grounded			1	$\mu\text{A}$
$I_{REV}$	Reverse Leakage Current	Disabled, $V_{IN} = 0\text{V}$ , $V_{OUT} = 5\text{V}$ , $I_{REV}$ at $V_{IN}$		1		$\mu\text{A}$
$R_{DS(ON)}$	Switch on-resistance	$V_{IN} = 5\text{V}$ , $I_{OUT} = 0.5\text{A}$ , $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$		90	135	$\text{m}\Omega$
				100	135	$\text{m}\Omega$
		$V_{IN} = 3.3\text{V}$ , $I_{OUT} = 0.5\text{A}$ , $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$		120	160	$\text{m}\Omega$
$I_{SHORT}$	Short-circuit current limit	Enabled into short circuit, $C_L = 22\mu\text{F}$		0.7		A
$I_{LIMIT}$	Over-Load Current Limit	$V_{IN} = 5\text{V}$ , $V_{OUT} = 4.8\text{V}$ , $C_L = 120\mu\text{F}$ , $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	0.6	0.8	1.0	A
$I_{Trig}$	Current limiting trigger threshold	$V_{IN} = V_{EN}$ , Output Current Slew rate ( $< 100\text{A/s}$ ), $C_L = 22\mu\text{F}$		1.0		A
$T_{SHORT}$	Short-circuit Response Time	$V_{OUT} = 0\text{V}$ to $I_{OUT} = I_{LIMIT}$ (short applied to output), $C_L = 22\mu\text{F}$		20		$\mu\text{s}$
$V_{IL}$	EN Input Logic Low Voltage	$V_{IN} = 2.7\text{V}$ to $5.5\text{V}$			0.8	V
$V_{IH}$	EN Input Logic High Voltage	$V_{IN} = 2.7\text{V}$ to $5.5\text{V}$	2			V
$I_{SINK}$	EN Input leakage	$V_{EN} = 5\text{V}$			1	$\mu\text{A}$
$T_{D(ON)}$	Output turn-on delay time	$C_L = 1\mu\text{F}$ , $R_{load} = 10\Omega$		0.05		ms
$T_R$	Output turn-on rise time	$C_L = 1\mu\text{F}$ , $R_{load} = 10\Omega$		0.6	1.5	ms
$T_{D(OFF)}$	Output turn-off delay time	$C_L = 1\mu\text{F}$ , $R_{load} = 10\Omega$		0.01		ms
$T_F$	Output turn-off fall time	$C_L = 1\mu\text{F}$ , $R_{load} = 10\Omega$		0.05	0.1	ms
$R_{FLG}$	FLG output FET on-resistance	$I_{FLG} = 10\text{mA}$		20	40	$\Omega$
$I_{FOH}$	Error Flag Off Current	$V_{FLG} = 5\text{V}$		0.01	1	$\mu\text{A}$
$T_{Blank}$	FLG blanking time	$C_L = 22\mu\text{F}$	4	7	15	ms
$T_{SHDN}$	Thermal shutdown threshold	Enabled, $R_{load} = 1\text{k}\Omega$		140		$^\circ\text{C}$
$T_{HYS}$	Thermal shutdown hysteresis			25		$^\circ\text{C}$
$\theta_{JA}$	Thermal Resistance Junction-to-Ambient	SOP-8L (Note 4)		110		$^\circ\text{C/W}$
		MSOP-8L-EP (Note 5)		60		$^\circ\text{C/W}$

Notes: 4. Test condition for SOP-8L: Device mounted on FR-4 2-layer board, 2oz copper, with minimum recommended pad layout.  
5. Test condition for MSOP-8L-EP: Device mounted on FR-4 2-layer board, 2oz copper, with minimum recommended pad on top layer and 3 vias to bottom layer ground plane.

**Typical Performance Characteristics**

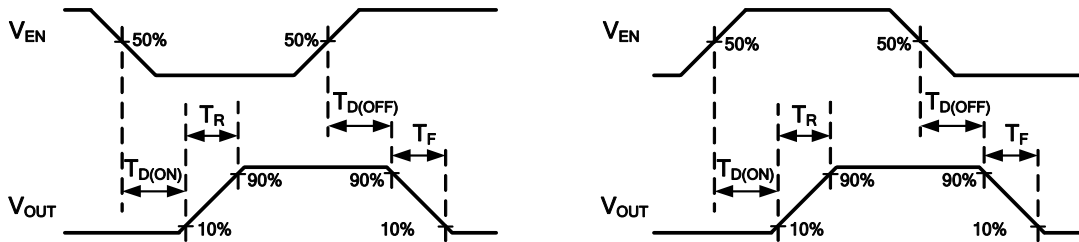
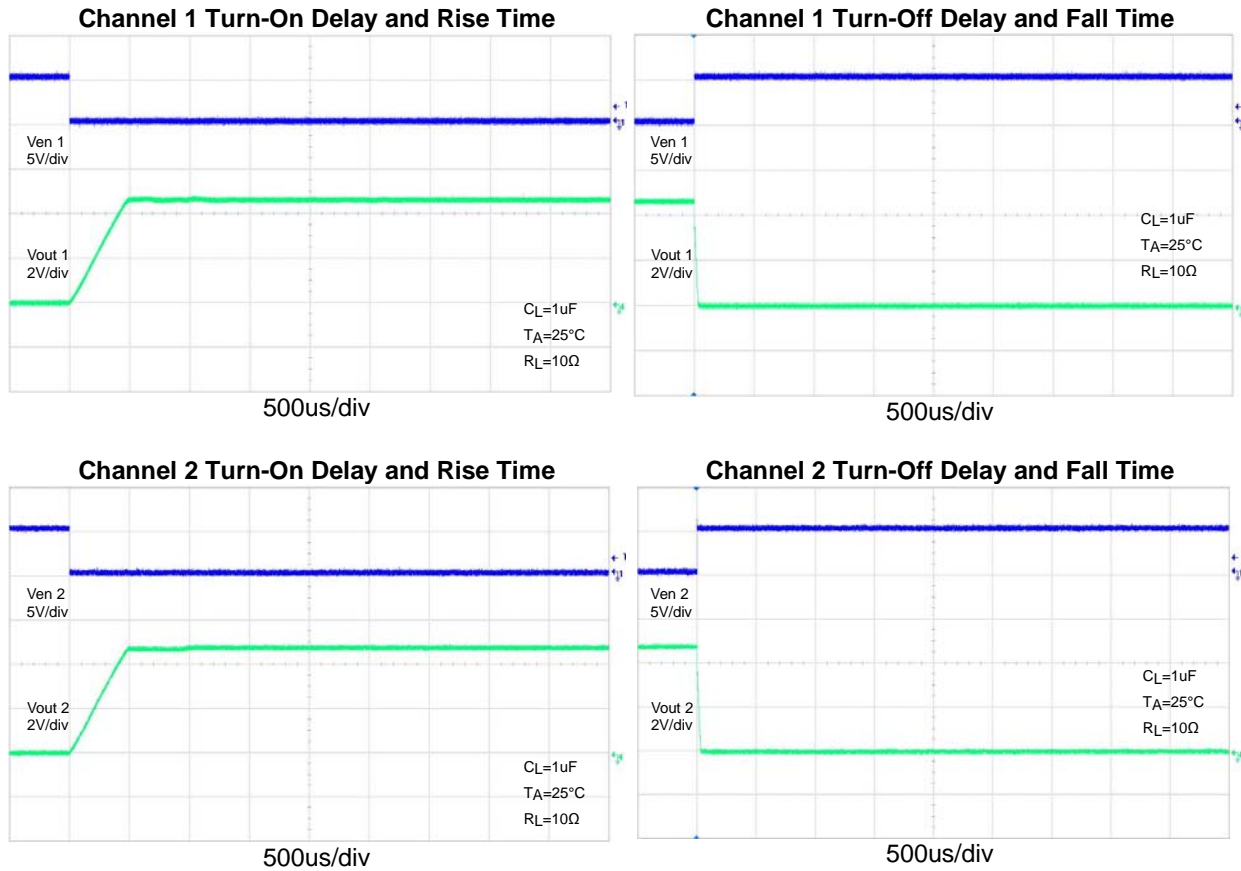
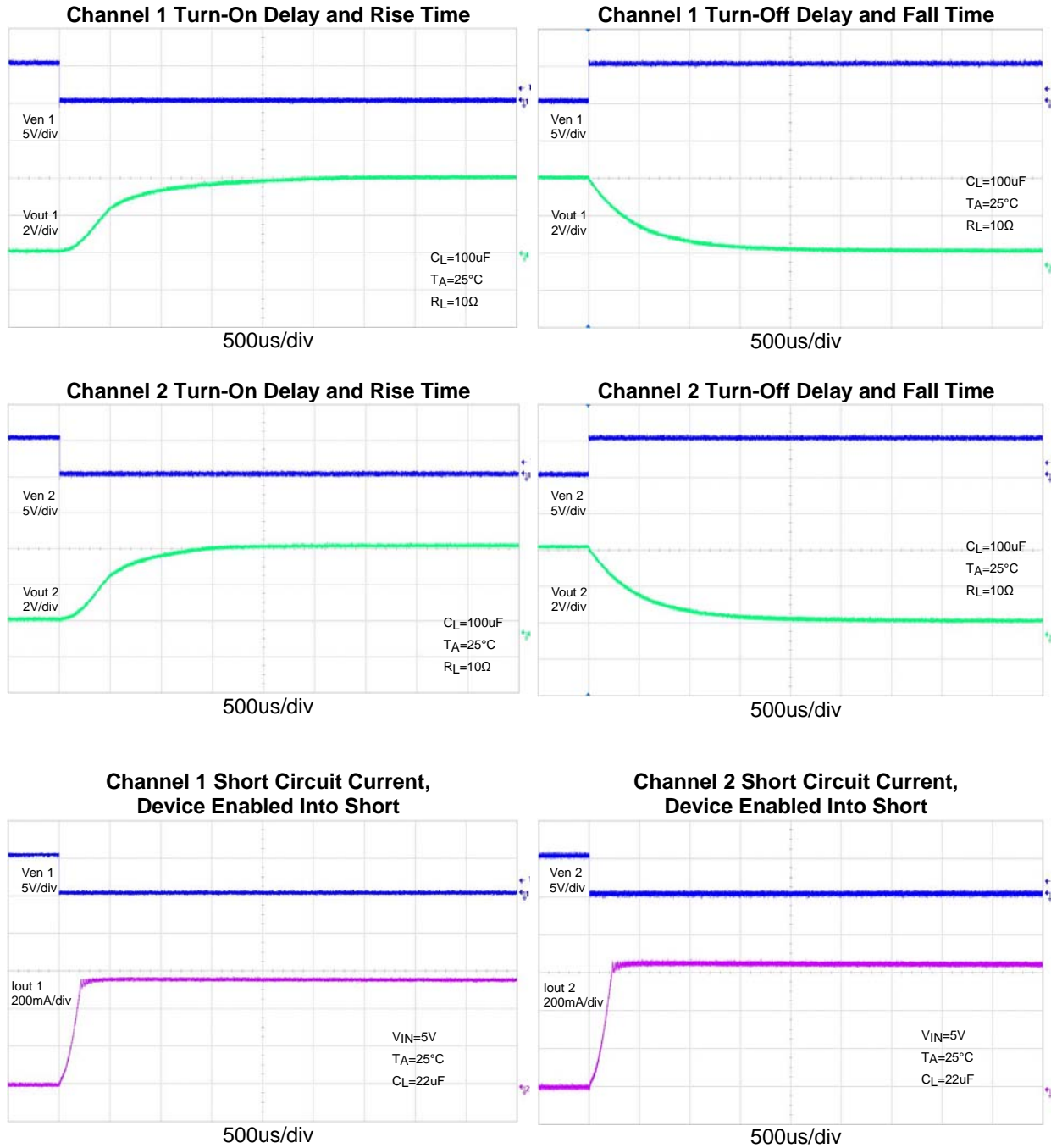


Figure 1. Voltage Waveforms: AP2146 (left), AP2156 (right)

All Enable Plots are for AP2146 Active Low

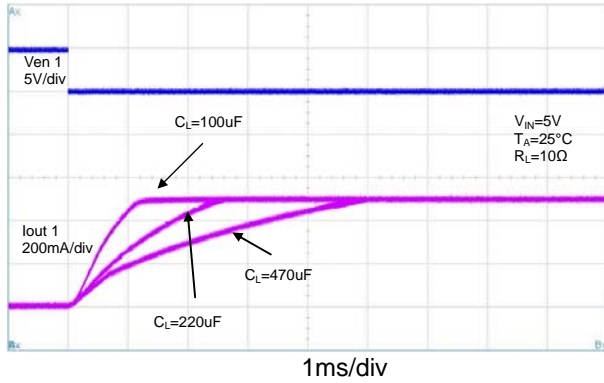


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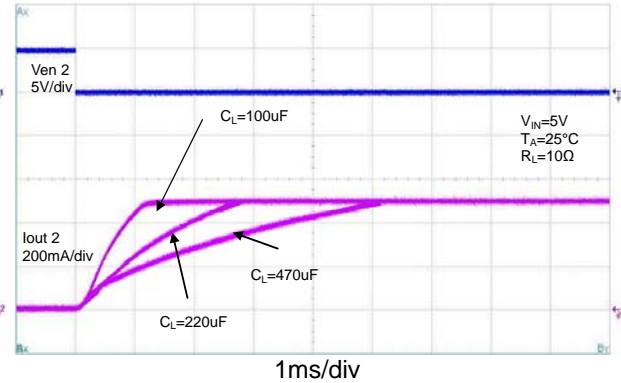


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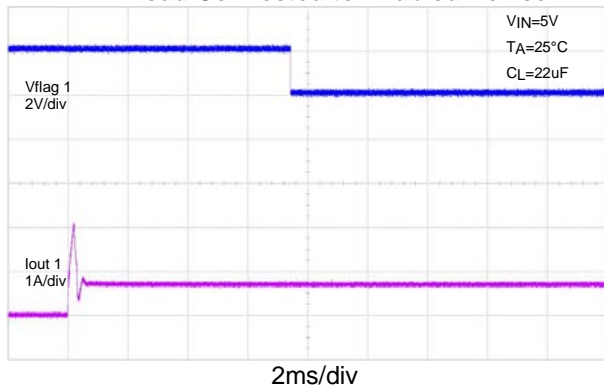
**Channel 1 Inrush Current**



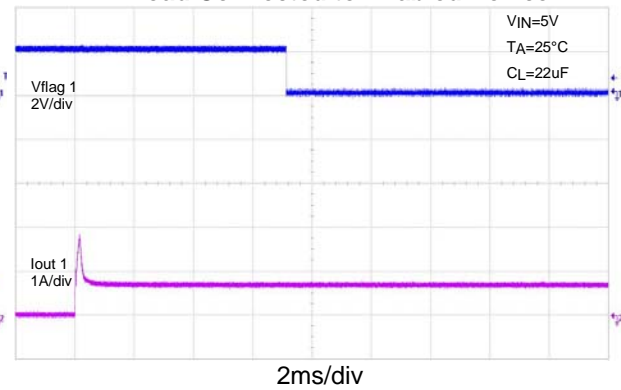
**Channel 2 Inrush Current**



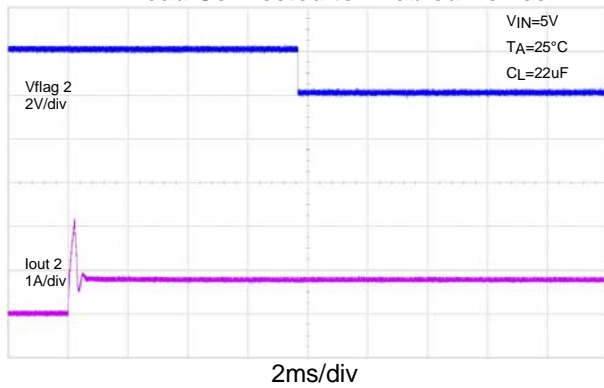
**Channel 1  
1 Ω Load Connected to Enabled Device**



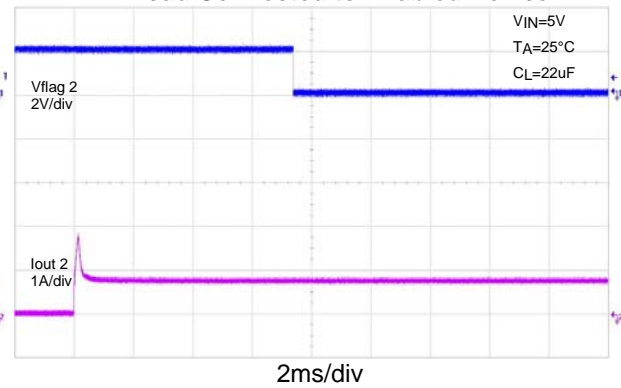
**Channel 1  
2Ω Load Connected to Enabled Device**



**Channel 2  
1 Ω Load Connected to Enabled Device**

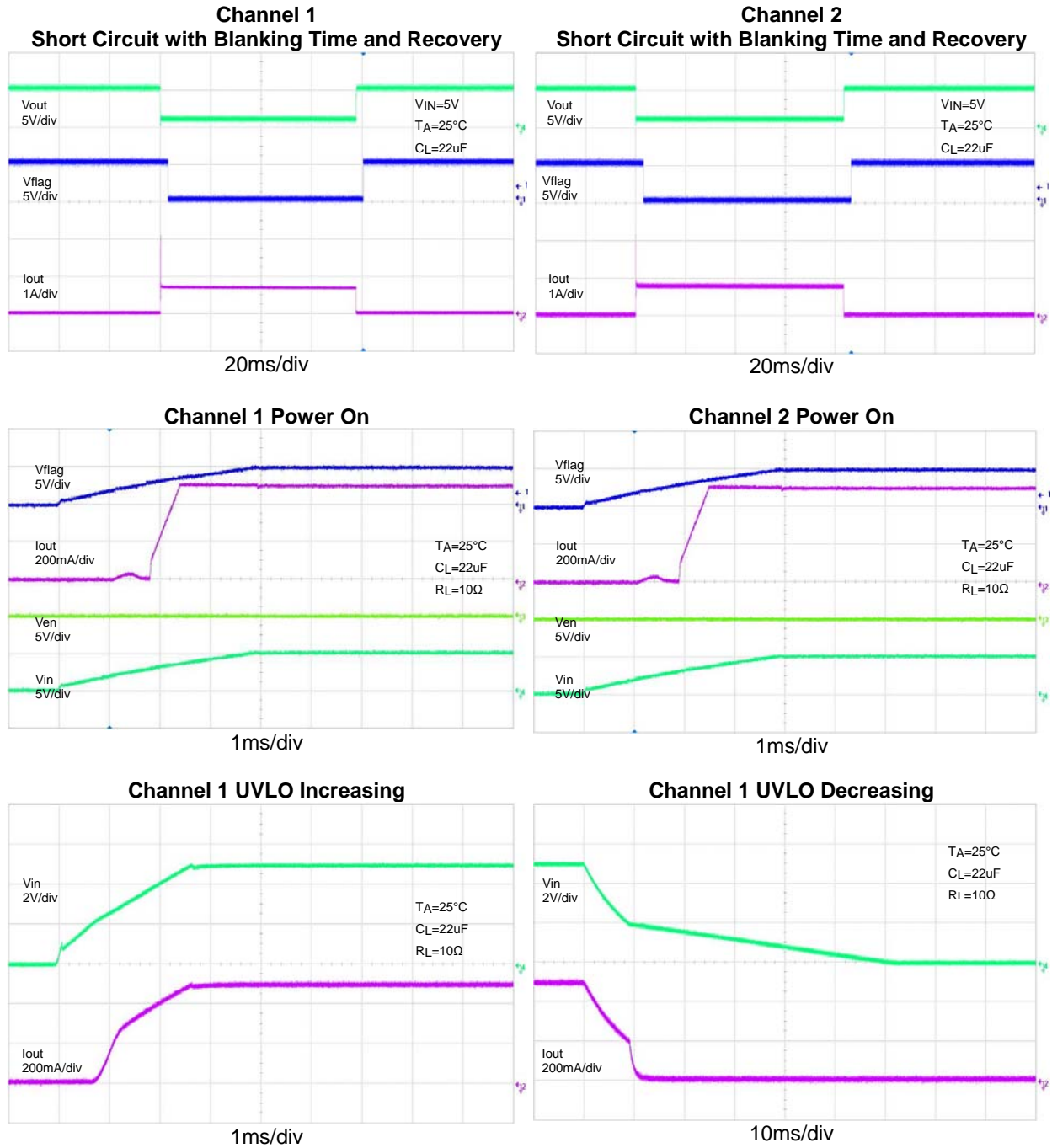


**Channel 2  
2Ω Load Connected to Enabled Device**

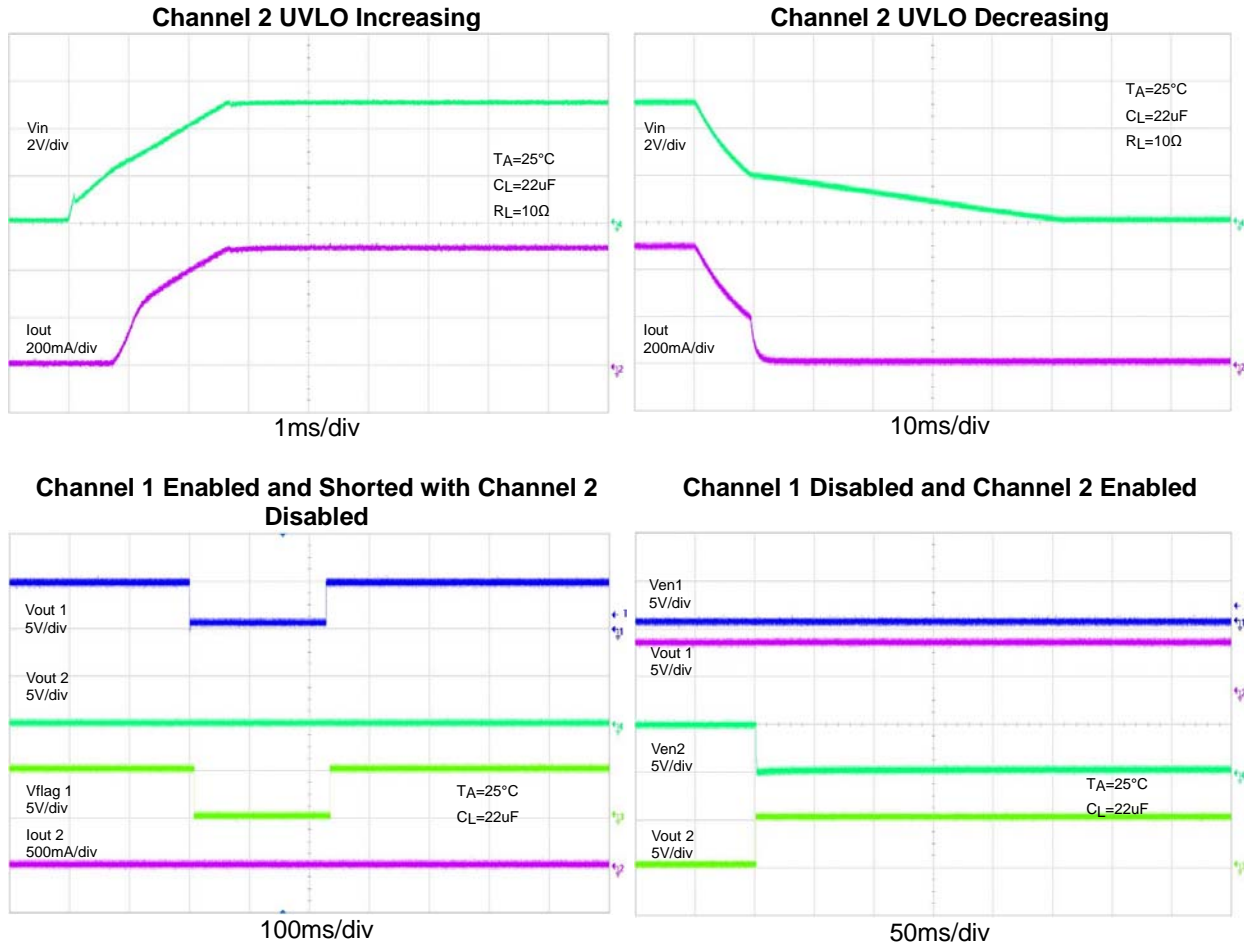




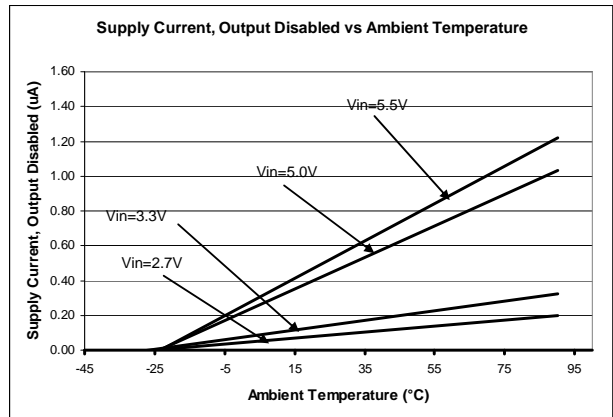
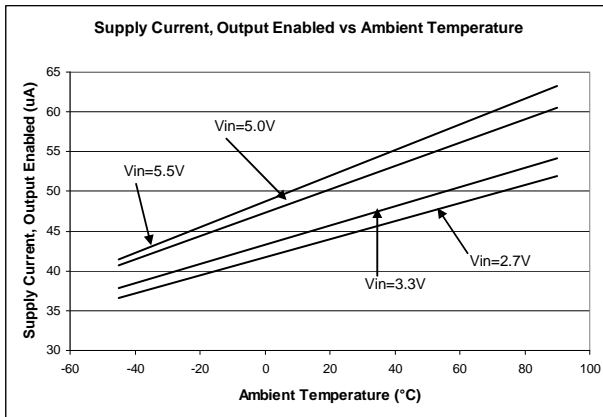
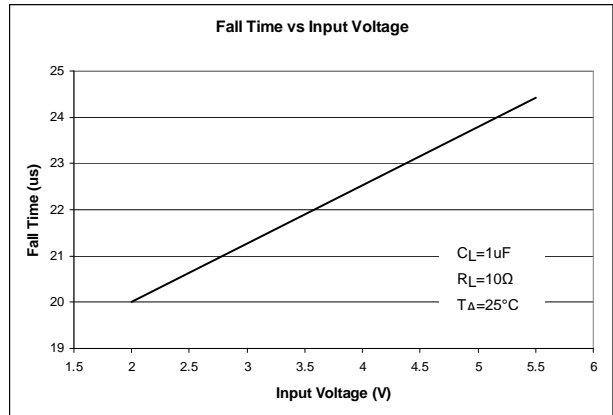
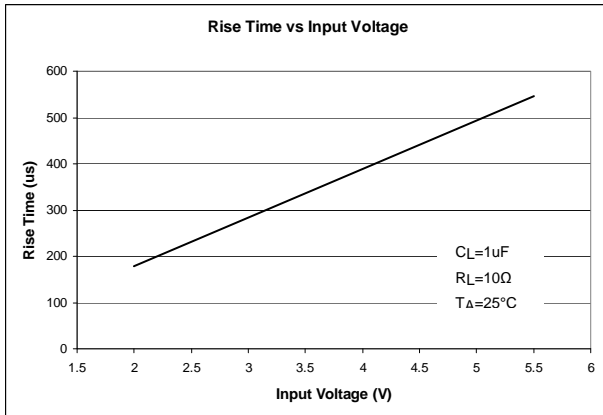
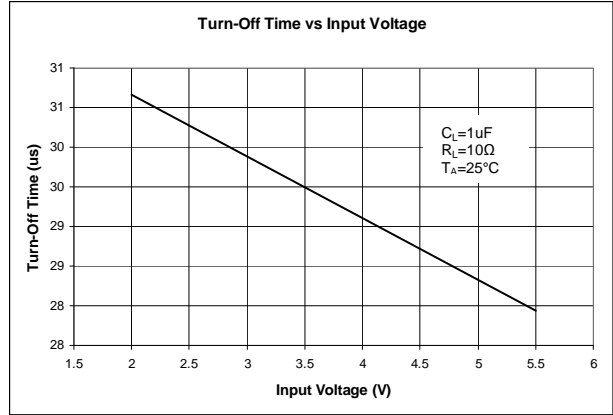
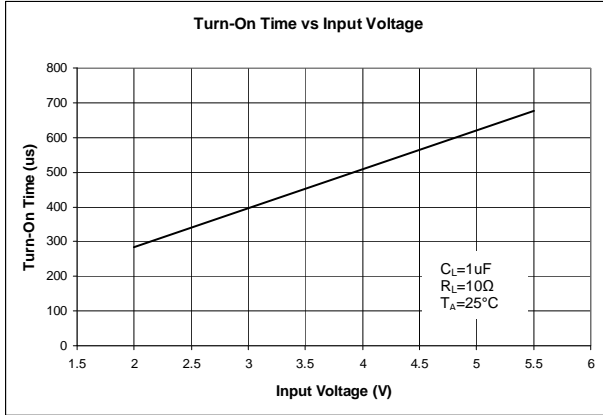
**Typical Performance Characteristics (Continued)**



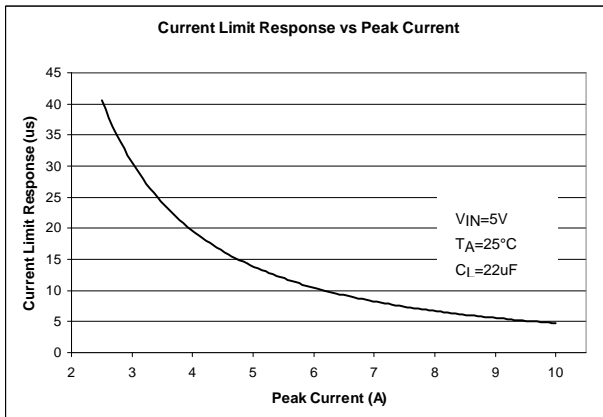
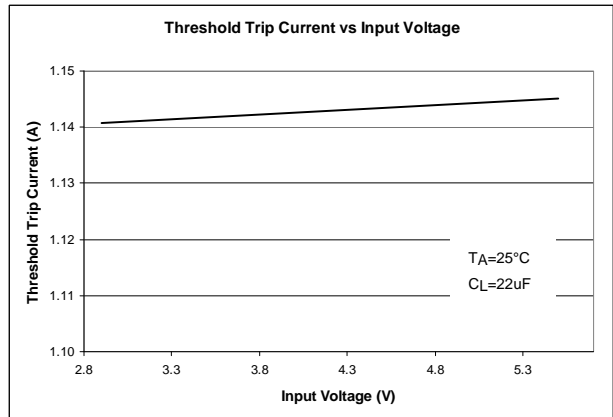
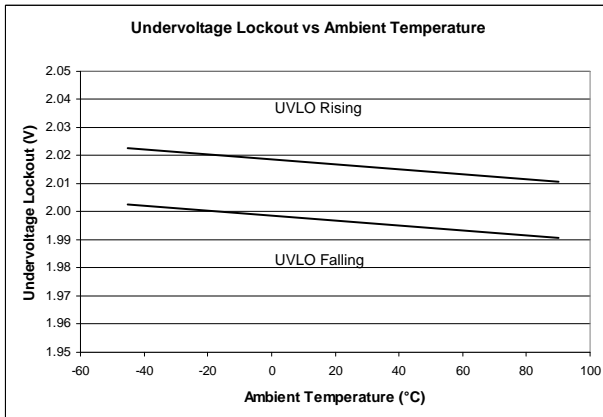
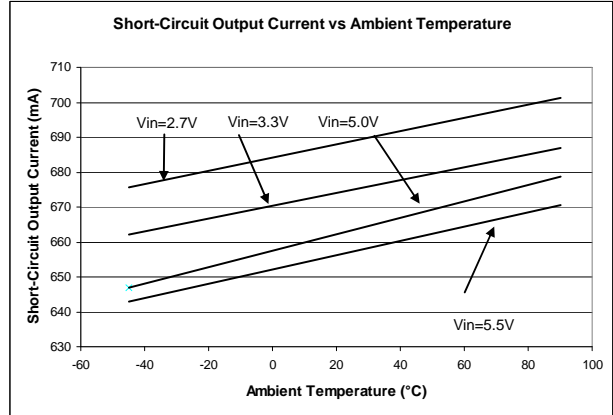
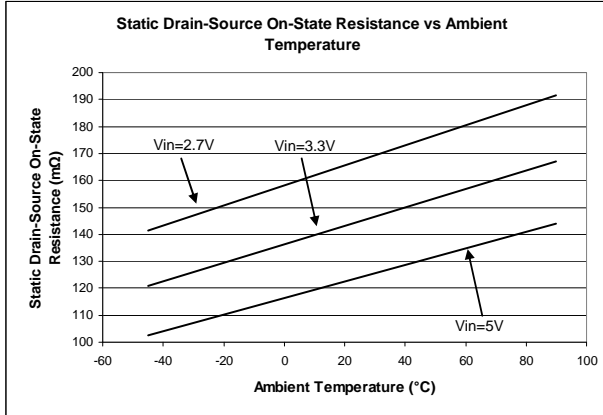
**Typical Performance Characteristics (Continued)**



**Typical Performance Characteristics (Continued)**



**Typical Performance Characteristics (Continued)**



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## Application Note

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### Power Supply Considerations

A 0.01- $\mu$ F to 0.1- $\mu$ F X7R or X5R ceramic bypass capacitor between IN and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the input (10- $\mu$ F minimum) and output pin(s) is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01- $\mu$ F to 0.1- $\mu$ F ceramic capacitor improves the immunity of the device to short-circuit transients.

### Over-current and Short Circuit Protection

An internal sensing FET is employed to check for over-current conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault stays long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted to GND before the device is enabled or before  $V_{IN}$  has been applied. The AP2146/AP2156 senses the short circuit and immediately clamps output current to a certain safe level namely  $I_{LIMIT}$ .

In the second condition, an output short or an overload occurs while the device is enabled. At the instance the overload occurs, higher current may flow for a very short period of time before the current limit function can react. After the current limit function has tripped (reached the over-current trip threshold), the device switches into current limiting mode and the current is clamped at  $I_{LIMIT}$ .

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold ( $I_{TRIG}$ ) is reached or until the thermal limit of the device is exceeded. The AP2146/AP2156 is capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its current limiting mode and is set at  $I_{LIMIT}$ .

Note that when the output has been shorted to GND at extremely low temperature ( $< -30^{\circ}\text{C}$ ), a minimum 120- $\mu$ F electrolytic capacitor on the output pin is recommended. A correct capacitor type with capacitor voltage rating and temperature characteristics must be properly chosen so that capacitance value does not drop too low at the extremely low temperature operation. A recommended capacitor should have temperature characteristics of less than 10% variation of capacitance change when operated at extremely low temp. Our recommended aluminum electrolytic capacitor type is Panasonic FC series.

### FLG Response

When an over-current or over-temperature shutdown condition is encountered, the FLG open-drain output goes active low after a nominal 7-ms deglitch timeout. The FLG output remains low until both over-current and over-temperature conditions are removed. Connecting a heavy capacitive load to the output of the device can cause a momentary over-current condition, which does not trigger the FLG due to the 7-ms deglitch timeout. The AP2146/AP2156 is designed to eliminate false over-current reporting without the need of external components to remove unwanted pulses.

**Application Note (Continued)**

**Power Dissipation and Junction Temperature**

The low on-resistance of the internal MOSFET allows the small surface-mount packages to pass large current. Using the maximum operating ambient temperature ( $T_A$ ) and  $R_{DS(ON)}$ , the power dissipation can be calculated by:

$$P_D = R_{DS(ON)} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

- $T_A$  = Ambient temperature °C
- $R_{\theta JA}$  = Thermal resistance
- $P_D$  = Total power dissipation

**Thermal Protection**

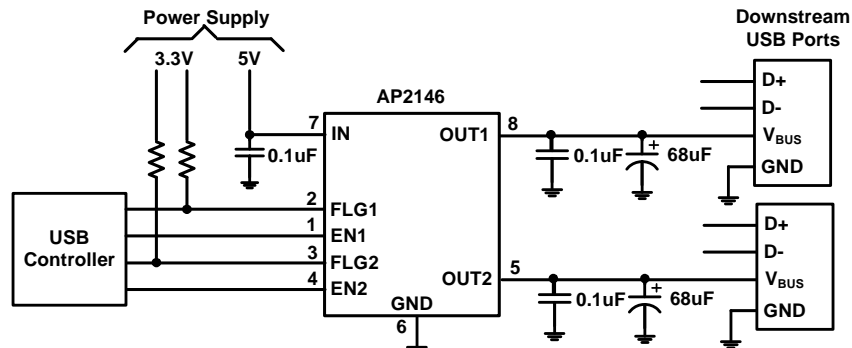
Thermal protection prevents the IC from damage when heavy-overload or short-circuit faults are present for extended periods of time. The AP2146/AP2156 implements a thermal sensing to monitor the operating junction temperature of the power distribution switch. Once the die temperature rises to approximately 140°C due to excessive power dissipation in an over-current or short-circuit condition the internal thermal sense circuitry turns the power switch off, thus preventing the power switch from damage. Hysteresis is built into the thermal sense circuit allowing the device to cool down approximately 25°C before the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed. The FLG open-drain output is asserted when an over-temperature shutdown or over-current occurs with 7-ms deglitch.

**Under-voltage Lockout (UVLO)**

Under-voltage lockout function (UVLO) keeps the internal power switch from being turned on until the power supply has reached at least 1.9V, even if the switch is enabled. Whenever the input voltage falls below approximately 1.9V, the power switch is quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed.

**Host/Self-Powered HUBs**

Hosts and self-powered hubs (SPH) have a local power supply that powers the embedded functions and the downstream ports (see Figure 2). This power supply must provide from 5.25V to 4.75V to the board side of the downstream connection under both full-load and no-load conditions. Hosts and SPHs are required to have current-limit protection and must report over-current conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.



**Figure 2. Typical Two-Port USB Host / Self-Powered Hub**

### Application Note (Continued)

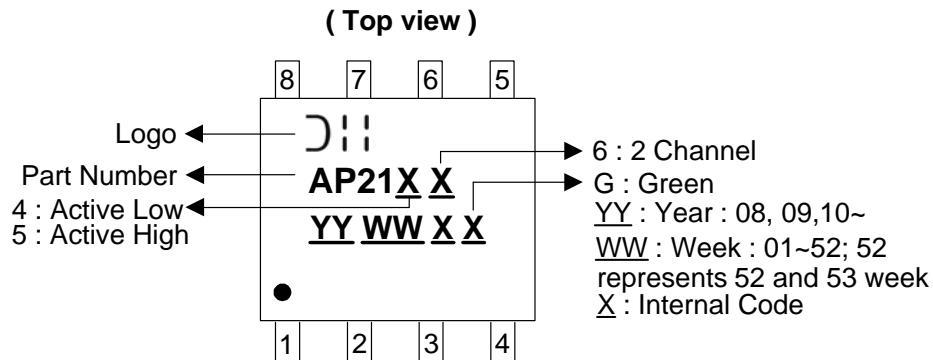
#### Generic Hot-Plug Applications

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise times and fall times of the AP2146/AP2156, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the AP2146/AP2156 also ensures that the switch is off after the card has been removed, and that the switch is off during the next insertion.

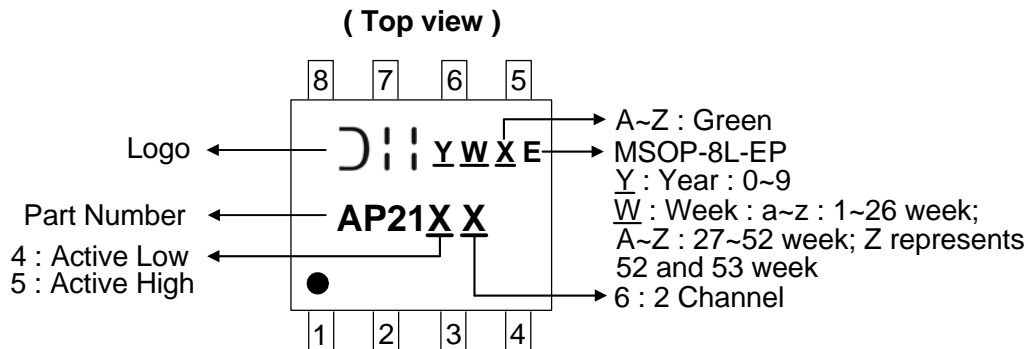
By placing the AP2146/AP2156 between the Vcc input and the rest of the circuitry, the input power reaches these devices first after insertion. The typical rise time of the switch is approximately 1ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge current and provides a hot-plugging mechanism for any device.

### Marking Information

#### (1) SOP-8L

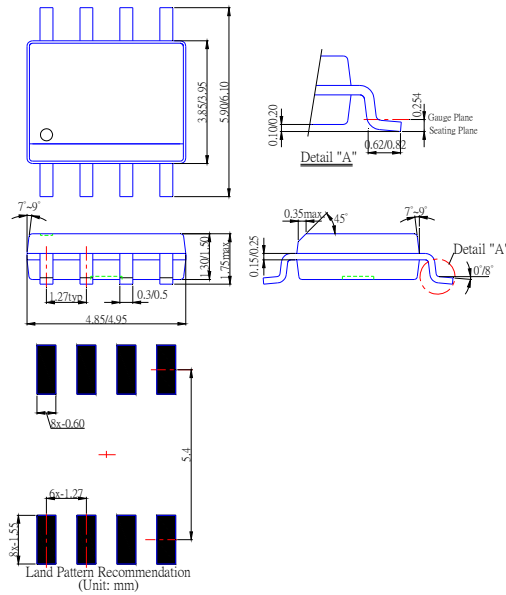


#### (2) MSOP-8L-EP

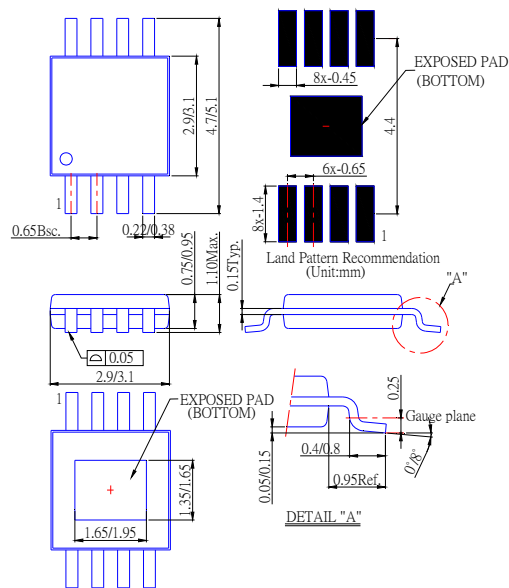


**Package Information (All Dimensions in mm)**

**(1) Package type: SOP-8L**



**(2) Package type: MSOP-8L-EP**





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