

FDC697P

P-Channel 1.8V PowerTrench® MOSFET

General Description

This P-Channel 1.8V specified MOSFET uses Fairchild's advanced low voltage Power Trench process. It has been optimized for battery power management applications.

Applications

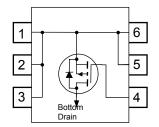
- Battery management
- Load Switch
- Battery protection

Features

• -8 A, -20 V $R_{DS(ON)} = 20 \text{ m}\Omega$ @ $V_{GS} = -4.5 \text{ V}$ $R_{DS(ON)} = 25 \text{ m}\Omega$ @ $V_{GS} = -2.5 \text{ V}$ $R_{DS(ON)} = 35 \text{ m}\Omega$ @ $V_{GS} = -1.8 \text{ V}$

- High performance trench technology for extremely low $R_{\ensuremath{\mathsf{DS}}(\ensuremath{\mathsf{ON}})}$
- · Fast switching speed
- FLMP SuperSOT-6 package: Enhanced thermal performance in industry-standard package size





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	I Parameter		Ratings	Units	
V _{DSS}	Drain-Source Voltage		-20	V	
V _{GSS}	Gate-Source Voltage		±8	V	
I _D	Drain Current - Continuous	(Note 1a)	-8	А	
	– Pulsed		-40		
P _D	Power Dissipation	(Note 1a)	2	W	
		(Note 1b)	1.5		
T _J , T _{STG}	Operating and Storage Junction Tem	perature Range	-55 to +150	°C	

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	60	°C/W
		(Note 1b)	111	
R _{0JC}	Thermal Resistance, Junction-to-Case		0.5	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.697	FDC697P	7"	8mm	3000 units

Symbol	Parameter	Test C	onditions	Min	Тур	Max	Units
Off Char	acteristics				l	I	I
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V,	I _D = -250 μA	-20			V
<u>ΔBV_{DSS}</u> ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = - 250 μA, R	eferenced to 25°C		-12.2		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -16 \text{ V},$	V _{GS} = 0 V			-1	μА
I _{GSS}	Gate-Body Leakage	$V_{GS} = \pm 8 V$,	V _{DS} = 0 V			±100	nA
On Char	acteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$	I _D = -250 μA	-0.4	-0.8	-1.5	V
$\Delta V_{GS(th)} \over \Delta T_J$	Gate Threshold Voltage Temperature Coefficient		eferenced to 25°C		2.9		mV/°C
R _{DS(on)}	Static Drain–Source On–Resistance	$V_{GS} = -2.5 \text{ V},$ $V_{GS} = -1.8 \text{ V},$	$I_D = -8 \text{ A}$ $I_D = -6.8 \text{ A}$ $I_D = -5.8 \text{ A}$ $I_D = -5.8 \text{ A}$ $I_D = -5.8 \text{ A}$		13 18 26 16	20 25 35 27	mΩ
g _{FS}	Forward Transconductance	$V_{DS} = -5 V$,	I _D = -8 A		37		S
Dvnamio	Characteristics				•	•	
C _{iss}	Input Capacitance	V _{DS} = - 10 V,	V _{GS} = 0 V.		3524		pF
Coss	Output Capacitance	f = 1.0 MHz			544		pF
C _{rss}	Reverse Transfer Capacitance				254		pF
R _G	Gate Resistance	V _{GS} = 15 mV,	f = 1.0 MHz		3.8		Ω
Switchin	g Characteristics (Note 2)						
t _{d(on)}	Turn–On Delay Time	$V_{DD} = -10 \text{ V},$	I _D = -1 A,		18	32	ns
t _r	Turn–On Rise Time	$V_{GS} = -4.5 \text{ V},$	R_{GEN} = 6 Ω		6	12	ns
t _{d(off)}	Turn-Off Delay Time	1			119	190	ns
t _f	Turn-Off Fall Time	1			43	69	ns
Q_g	Total Gate Charge	$V_{DS} = -10 \text{ V},$	I _D = -8 A,		39	55	nC
Q _{gs}	Gate-Source Charge	$V_{GS} = -4.5 \text{ V}$			6	8.4	nC
Q_{gd}	Gate-Drain Charge				5.6	7.8	nC
Drain-S	ource Diode Characteristics	and Maximur	n Ratings		•	•	
Is	Maximum Continuous Drain-Source					-1.6	Α
V _{SD}	Drain–Source Diode Forward Voltage	V _{GS} = 0 V, I _S =	= -1.6 A (Note 2)		-0.7	-1.2	V
t _{rr}	Reverse Recovery Time	I _F = -8 A,			27		ns
Q _{rr}	Reverse Recovery Charge	$d_{iF}/d_t = 100 \text{ A/µs}$	i		16		nC

Notes: 1. $R_{0,JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{0,JC}$ is guaranteed by design while $R_{0,CA}$ is determined by the user's board design.



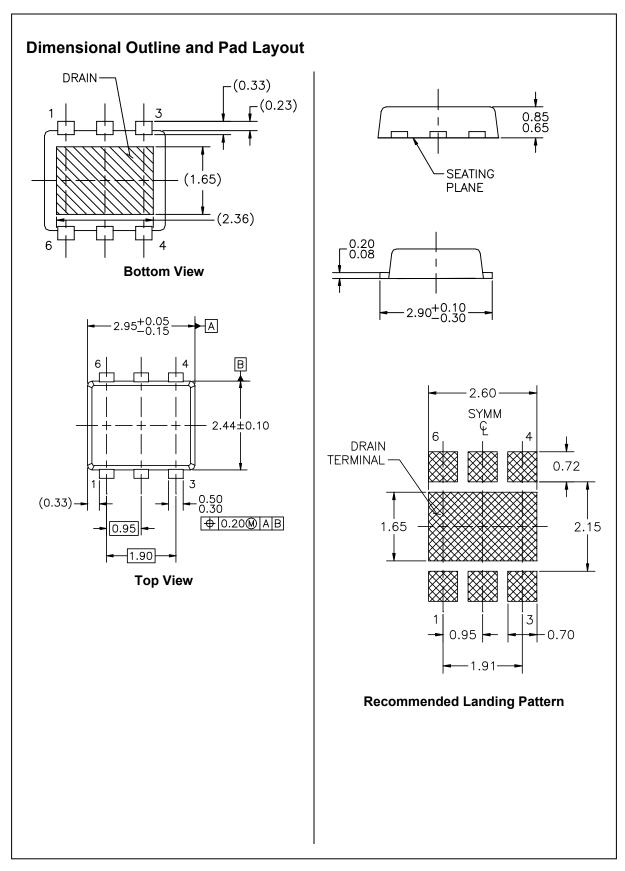
a) 60°C/W when mounted on a 1in² pad of 2 oz copper



b) 111°C/W when mounted on a minimum pad of 2 oz

Scale 1:1 on letter size paper

2. Pulse Test: Pulse Width < 300 μ s, Duty Cycle < 2.0%



Typical Characteristics

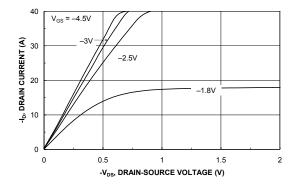


Figure 1. On-Region Characteristics.

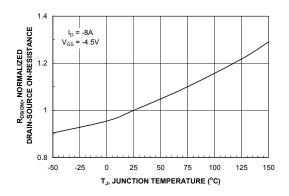


Figure 3. On-Resistance Variation withTemperature.

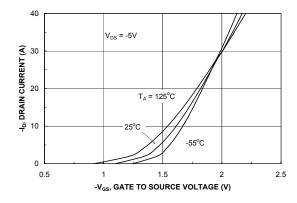


Figure 5. Transfer Characteristics.

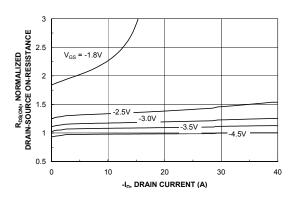


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

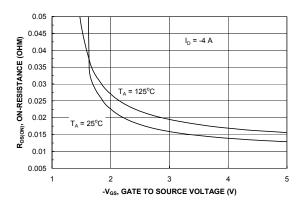


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

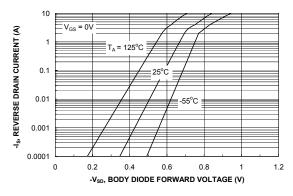
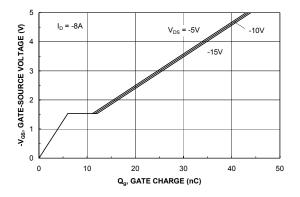


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

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Typical Characteristics



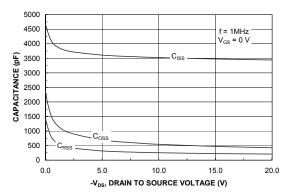
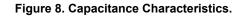
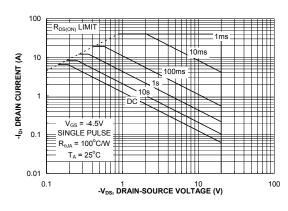


Figure 7. Gate Charge Characteristics.





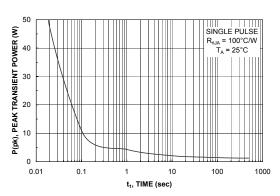


Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

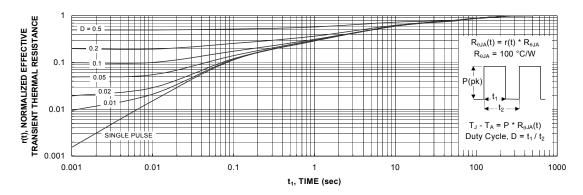


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

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CoolFET™	FPS™	MicroFET™	QFET®	SuperSOT™-8
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