ML4813*

Flyback Power Factor Controller

GENERAL DESCRIPTION

The ML4813 is a PWM controller designed for use in a discontinuous "flyback" or "buck-boost" type power factor correction (PFC) system for low power, low cost applications.

The circuit includes a precision reference, oscillator, error amplifier, over-voltage comparator, over-current comparator, and an extra op-amp as well as a high current output. In addition, start-up is simplified by an under-voltage lockout circuit.

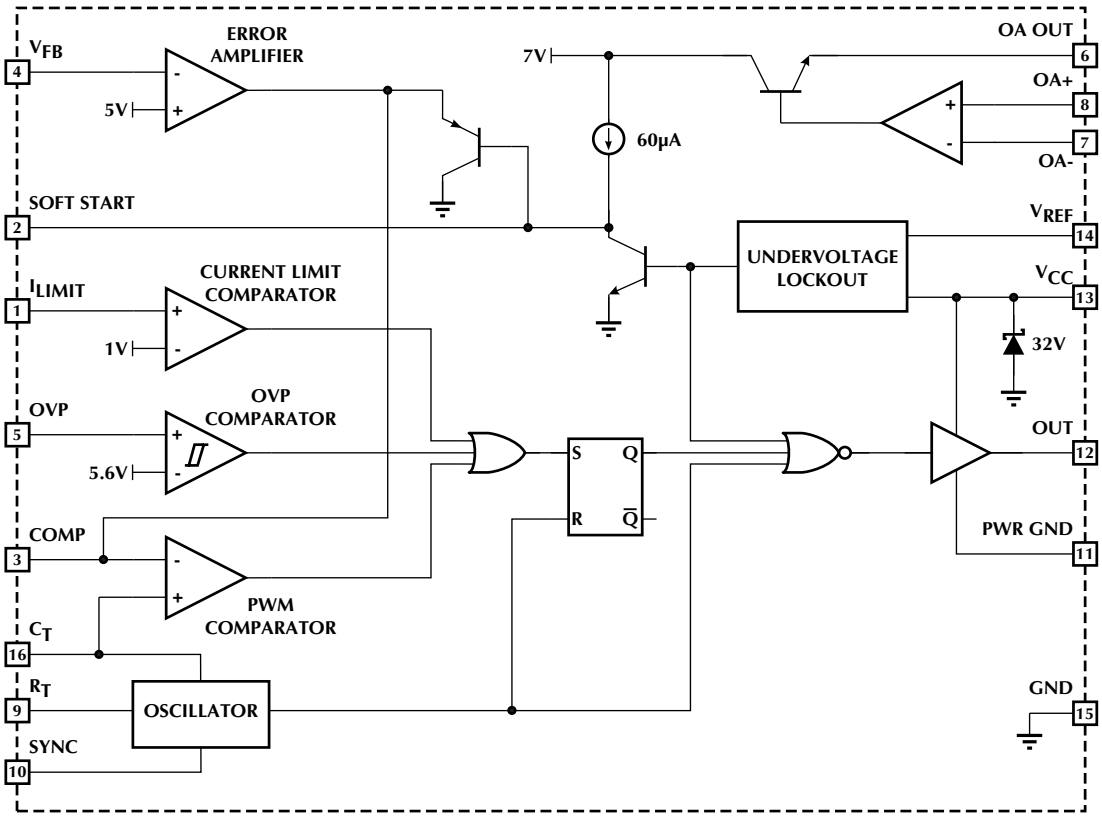
In a typical application, the ML4813 functions as a voltage mode regulator. By maintaining a constant duty cycle, the current follows the input voltage, making the impedance of the entire circuit appear purely resistive. With the flyback circuit, power factors of 0.99 are easily achievable with a small output inductor and a minimum of external components.

FEATURES

- Precision buffered 5V reference
- Extra op-amp for output voltage instrumentation amplifier
- Overcurrent comparator for switch protection
- Soft start and under-voltage lockout for easy low surge off-line starting
- 1A peak current Totem-pole output drive
- Overvoltage comparator eliminates output "runaway" due to load removal
- Large oscillator amplitude for better noise immunity

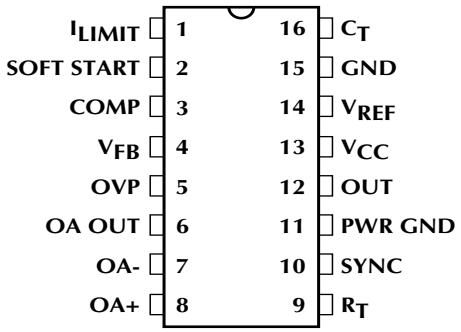
*** This Part Is End Of Life As Of August 1, 2000**

BLOCK DIAGRAM



PIN CONFIGURATION

ML4813
16-Pin PDIP (P16)
16-Pin SOIC (S16W)



TOP VIEW

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	I_{LIMIT}	Current limit sense pin which is normally connected to the sense resistor. When I_{LIMIT} exceeds 1V, the PWM cycle is terminated
2	SOFT START	Connection for the soft start capacitor
3	COMP	Output of error amplifier and input to the PWM comparator
4	V_{FB}	Control loop feedback voltage
5	OVP	Overvoltage comparator input
6	OA OUT	Output of the uncommitted op amp
7	OA-	Inverting input of the uncommitted op amp
8	OA+	Non-inverting input of the uncommitted op amp
9	R_T	Connection for the oscillator timing resistor
10	SYNC	Input for synchronizing the oscillator to an external source
11	PWR GND	Return for the high current output transistors
12	OUT	High current driver output
13	V_{CC}	Power supply input
14	V_{REF}	Buffered reference output
15	GND	Analog signal ground
16	C_T	Connection for the oscillator timing capacitor

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Current 40mA
OUT Current ..... ±1A
OUT Energy (capacitive load, per cycle) 5µJ
COMP Sink Current 10mA
C_T Charging Current 5mA
Analog Input Voltage (pins 1, 3-8) .... GND - 0.3V to 5.5V
Junction Temperature 150ºC
Storage Temperature Range ..... –65ºC to 150ºC
Lead Temperature (Soldering, 10 sec) 260ºC
Thermal Resistance (θ_{JA})
PDIP 88ºC/W
SOIC 105ºC/W

OPERATING CONDITIONS

Temperature Range
ML4813CX ..... 0ºC to 70ºC
ML4813IX ..... -40ºC to 85ºC

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, R_T = 14kΩ, C_T = 1nF, T_A = Operating Temperature Range (Notes 1, 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OSCILLATOR					
Initial Accuracy	T_j = 25ºC	90	97	104	kHz
Voltage Stability	12V < V_{CC} < 18V		0.3		%
Temperature Stability				2	%
Total Variation	Line, temp	88		108	kHz
Ramp Valley				1.0	V
Ramp Peak			4.3		V
R_T Voltage		4.8	5.0	5.2	V
Discharge Current	T_j = 25ºC, $V(C_T)$ = 2V		7.5	8.4	9.3	mA
	$V(C_T)$ = 2V	7.2	8.4	9.5	mA
SYNC Threshold		0.8	1.4	2.0	V
SYNC Bias Current				350	800	µA
REFERENCE					
Output Voltage (V_{REF})	T_j = 25ºC, I_{REF} = 1mA	4.95	5.00	5.05	V
Line Regulation	12V < V_{CC} < 25V		6	20	mV
Load Regulation	1mA < I_{REF} < 20mA		3	20	mV
Temperature Stability				0.4	%
Total Variation	Line, load, temp	4.9		5.1	V
Output Noise	10Hz to 10kHz		50		µV
Long Term Stability	T_j = 125ºC, 1000 hours			5	25	mV
Short Circuit Current	V_{REF} = GND	-30	-85	-180	mA

ELECTRICAL CHARACTERISTICS (cont.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ERROR AMPLIFIER					
Input Offset Voltage			-15	15	mV
Input Bias Current			-0.1	-1.0	µA
Open Loop Gain	1V < COMP < 5V	60	75		dB
PSRR	12V < V_{CC} < 25V	60	70		dB
Output Sink Current		COMP = 1.1V, V_{FB} = 6.2V	2	12	mA
Output Source Current		COMP = 5V, V_{FB} = 4.8V	-0.5	-1.0	mA
Output High Voltage		I_{COMP} = -0.5mA, V_{FB} = 4.8V	5.3	6.4	V
Output Low Voltage		I_{COMP} = 2mA, V_{FB} = 6.2V		0.5 1.0	V
Unity Gain Bandwidth				1.0	MHz
UNCOMMITTED OP AMP					
Input Offset Voltage		-10		10	mV
Input Bias Current			-0.1	-2.0	µA
Input Offset Current		-350		350	nA
Open Loop Gain			90		dB
PSRR		80	125		dB
Output High Voltage		I_{COMP} = -10mA	6.5	8	V
Output Low Voltage		R_L = 10kΩ		200 500	mV
I_{LIMIT} COMPARATOR					
Input Trip Point		0.8	1.0	1.2	V
Input Bias Current			-2	-15	µA
Propogation Delay Time			150		ns
OVP COMPARATOR					
Input Trip Point		5.4	5.55	5.7	V
Hysteresis			100		mV
Input Bias Current			-0.3	3	181A
PWM COMPARATOR					
Input Common Mode Range		-0.2		5.5	V
Input Bias Current			-2	-10	µA
Propogation Delay Time			150		ns
SOFT START					
Soft Start Current		$V_{SOFT\ START}$ = 1V	40	65 90	µA

ELECTRICAL CHARACTERISTICS (cont.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT					
Output Low Voltage	I_{OUT} = 10mA		0.1	0.4	V
I_{OUT} = 200mA			1.2	2.2	V
	V_{CC} = 8V, I_{OUT} = 5mA		0.1	0.8	V
Output High Voltage	I_{OUT} = -20mA		13	13.6	V
	I_{OUT} = -200mA	12	13.4		V
Rise/Fall Time	C_L = 1000pF		50		ns
UNDERVOLTAGE LOCKOUT					
Start-up Threshold		15	16.3	17.5	V
Shutdown Threshold		9	10.1	11.2	V
V_{REF} Good Threshold			4.4		V
SUPPLY					
Start-up Current V_{CC} = 14V			0.9	1.5	mA
Operating Current			20	30	mA
Shunt Regulator Voltage	I_{CC} = 30mA	25	30	34	V

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 2: VCC is raised above the UVLO start-up threshold, then returned to 15V.

FUNCTIONAL DESCRIPTION

OSCILLATOR

The ML4813 oscillator charges the external capacitor (C_T) with a current (I_{SET}) equal to $5/R_{SET}$. When the capacitor voltage reaches the upper threshold, the comparator changes state and the capacitor discharges to the lower threshold through Q1. While the capacitor is discharging, Q2 provides a high pulse.

The oscillator period can be described by:

$$t_{OSC} = t_{RAMP} + t_{DEADTIME} \quad (1)$$

where:

$$t_{RAMP} = \frac{C_T}{I_{SET}} \quad (2)$$

and:

$$t_{DEADTIME} = \frac{C_T}{8.4mA - I_{SET}} \quad (3)$$

A graph showing the relationship between R_T, C_T, the oscillator frequency, and maximum duty cycle is given in Figure 1. A pulse of a duration shorter than $t_{DEADTIME}$ from an external frequency source set to a higher frequency than f_{OSC} can be applied to pin SYNC to synchronize the oscillator. R_{SYNC} and C_{SYNC} shorten longer pulses, as shown in Figure 2.

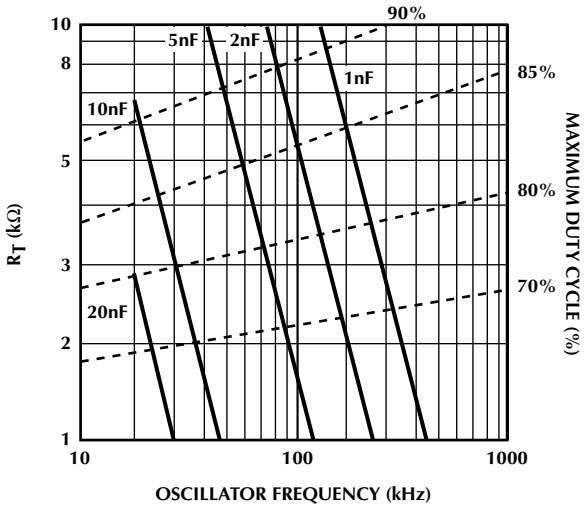


Figure 1. Oscillator Timing Resistance vs. Frequency

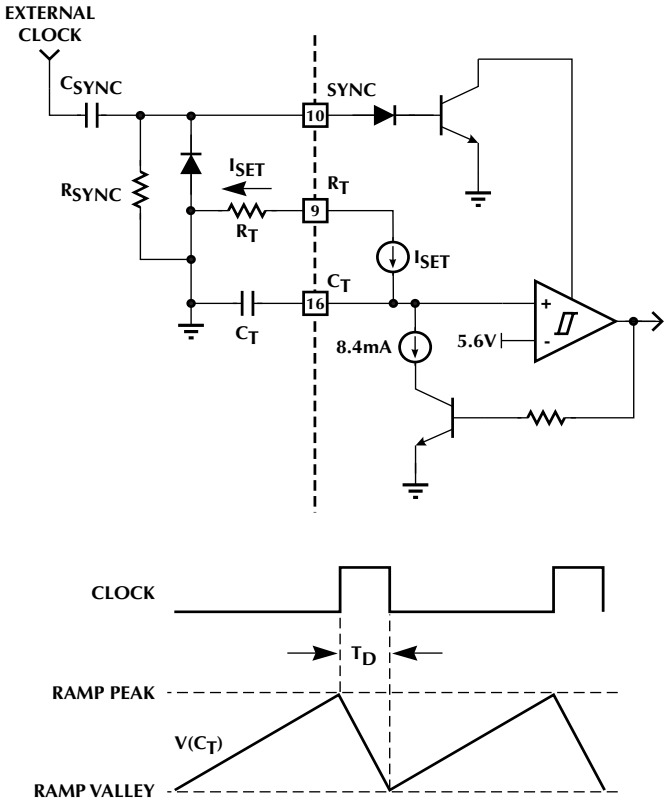


Figure 2. Oscillator Block Diagram

OUTPUT DRIVER STAGE

The ML4813 output driver is a 1A peak output high speed totem-pole circuit designed to quickly drive capacitive loads such as MOSFET gates. See Figure 3 for the output saturation characteristics for sourcing and sinking current.

ERROR AMPLIFIER

The ML4813 error amplifier is a high open loop gain, wide bandwidth amplifier. See Figure 4 for the gain and phase plot.

UN-COMMITTED OP-AMP

The ML4813 contains an uncommitted op amp which is normally configured as a differencing amplifier to sense the output voltage. The output voltage in the flyback configuration is not ground referenced. The op amp in the ML4813 is a PNP input amplifier similar to the LM324 but with an open emitter class A output stage.

REFERENCE

The reference output voltage versus output current characteristic is shown in Figure 5.

UNDERVOLTAGE LOCKOUT

On power-up, the ML4813 is in the UVLO condition; output low and quiescent current low. The ML4813 becomes operational when V_{CC} reaches 16V. When V_{CC} drops below 10V, the UVLO condition is re-imposed. During UVLO, the V_{REF} pin is off, making it usable as a "flag" for starting up a down-stream PWM converter.

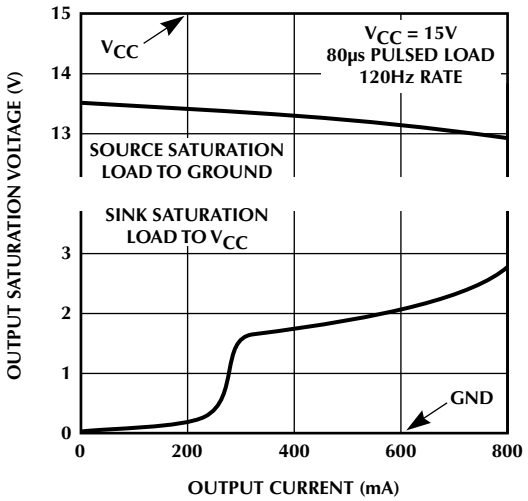


Figure 3. Output Saturation Voltage vs. Output Current

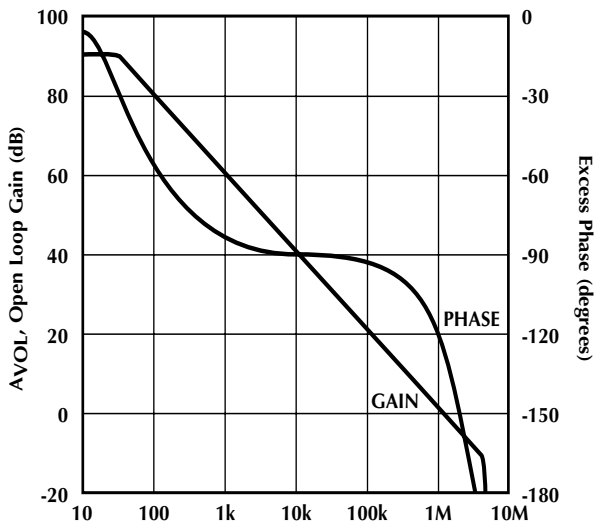


Figure 4. Error Amplifier Open Loop Gain and Phase vs. Frequency

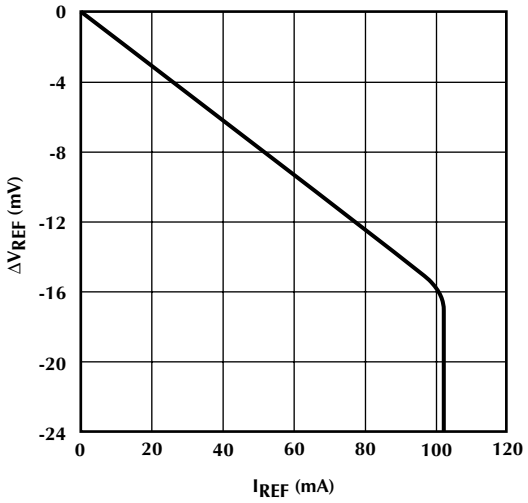


Figure 5. Reference Load Regulation vs. Output Current

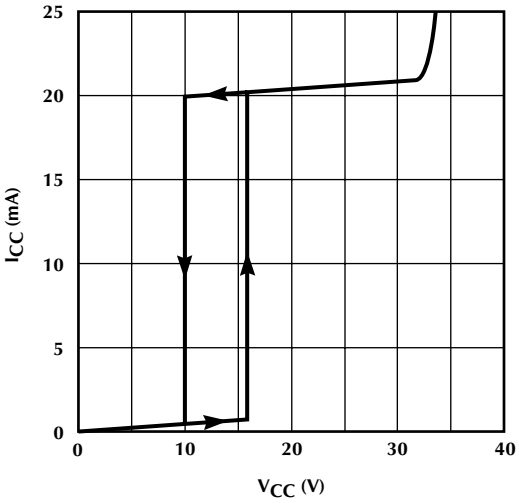


Figure 6. Supply Current vs. Supply Voltage

APPLICATIONS

The ML4813 is used to implement a discontinuous mode flyback (buck-boost) power factor regulator as shown in Figure 7. This topology is particularly well suited for low power applications such as fluorescent ballasts and low power switching supplies. It is also a useful topology when there is a requirement for the output voltage to be lower than the peak input voltage, or where an isolated output is required. This is not possible with a boost topology, where the output voltage must always be higher than the maximum peak of the input voltage range. The typical input range for the flyback power factor regulator is from 90VAC to 260VAC.

The regulator operates in the discontinuous current conduction mode. The inductor energy stored during the ON time of the power switch Q is completely delivered to the output capacitance during the OFF time. Under steady state conditions, the inductor current at the beginning of the ON time starts to ramp-up from 0 Amps to a value that is determined by the instantaneous value of the input full wave rectified voltage; the ON time as it is set by the error amplifier and the PWM comparator; and finally by the inductor itself.

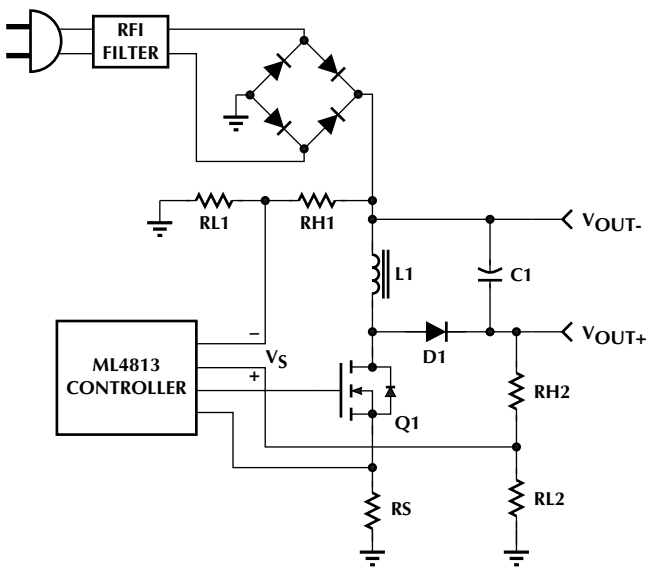


Figure 7. Simplified Application Circuit

The expression for the inductor peak current is given by:

$$I_L(\theta) = \frac{V_{IN}(\theta) \times t_{ON}}{L} \quad (4)$$

Where:

$I_L(\theta)$ = instantaneous peak inductor current

t_{ON} = Power MOSFET "ON" time

$V_{IN}(\theta) = V_P \sin \theta$ = Instantaneous input voltage

V_P = Input peak voltage

Figure 8 shows the relationship between the low frequency envelope and the high frequency inductor current. Note that for clarity the scale between the two waveforms has not been preserved. Normally for 60Hz input line and 100kHz switching frequency, each half of the sine wave contains approximately 833 high frequency triangular waveforms.

The envelope of the peaks of the switch current, which in this case represents the current drawn from the input source, has a sinewave shape. This relationship is shown as:

$$I_L(\theta) = I_P \times \sin\theta \quad (5)$$

By combining (4) and (5), the following useful relationship is obtained:

$$t_{ON} = \frac{L \times I_P}{\sqrt{2} \times V_{RMS}} \quad (6)$$

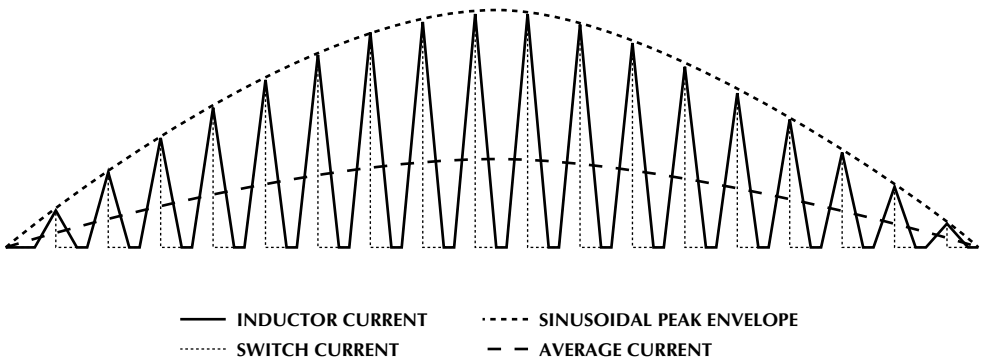


Figure 8. Switch and Line Currents in the Flyback PFC Circuit

APPLICATIONS (Continued)

Note that $V_{IN}(\theta) = V_P \times \sin(\theta)$ and that $V_P = 1.414 \times V_{RMS}$. The average value of the input triangular current is:

$$I_{AVG}(\theta) = \frac{t_{ON}}{2T} \times I_P \times \sin\theta \quad (7)$$

Where I_{AVG} is the average value of the switch current (the value of the current at the input of the regulator after filtering), and T is the period of the switch cycle.

Substitution of (6) into (7) yields:

$$I_{AVG}(\theta) = \frac{L \times {I_P}^2}{2.828 \times T \times V_{RMS}} \times \sin\theta \quad (8)$$

Equation (8) clearly shows that the average value of the switch current is sinusoidal and in phase with the input voltage. The peak value of the average current is:

$$I_{AVG(PEAK)} = \frac{L \times {I_P}^2}{2.828 \times T \times V_{RMS}} \times \sin\theta \quad (9)$$

Also:

$$I_{AVG(PEAK)} = \frac{\sqrt{2} \times P_{IN}}{V_{RMS}} \quad (10)$$

Rearranging equations (9) and (10) to solve for P_{IN} yields:

$$P_{IN} = \frac{L \times {I_P}^2 \times f}{4} \quad (11)$$

For optimum performance and the lowest inductor peak currents, the inductor current should be at the verge of continuity at the lowest operating voltage point and at full load. This can be satisfied if:

$$I_P \le \frac{V_{IN} \times V_{OUT}}{f \times L \times (V_{IN} + V_{OUT})} \quad (12)$$

Finally, (11) and (12) can be combined to derive an upper bound for the inductor value that will guarantee that the regulator always stays in the discontinuous mode of operation. If the regulator were to operate in the continuous mode the average input current would not be sinusoidal.

$$L \le \left[\frac{V_{IN} \times V_{OUT}}{2\sqrt{f \times P_{IN}} \times (V_{IN} + V_{OUT})} \right]^2 \quad (13)$$

FLYBACK INDUCTOR CALCULATION

Equation (13) gives the upper bound for the inductor value for any set of specified operating conditions. Normally, a few iterations may be required for finalizing the value to correct for second or third order effects. This means that a good initial value for the inductor is probably 10 to 20% lower than the value calculated by the right hand side expression in (13).

Several core materials are candidates for the inductor, such as powder iron, gapped ferrites, moly permalloy, etc. There are no particular restrictions on the inductor except that the inductance is the correct value and the losses are acceptable.

INPUT BYPASS CAPACITANCE

The triangular high frequency current is bypassed by an input capacitor (C_{IN}). This should be a high quality film capacitor with low ESR value for minimum losses and heating. Polyester, polypropylene or x-type (for line side) are good candidates. Typical values, depending on the power level, can range anywhere from 330nF to 1.5µF. The next filtering stage of the RFI filter has an inductor as an input to isolate C_{IN} from the other capacitors which may be present at the input circuit. Note that C_{IN} can be on either side of the bridge rectifier. The preferred location for low crossover distortion is on the input side. The ripple voltage across this capacitor is:

$$V_{C(P-P)} = \left(\frac{D}{C_{IN} \times f} \times \sqrt{\frac{P_{IN}}{L \times f}} \right) - \frac{\sqrt{2}P_{IN}}{C_{IN} \times f \times V_{IN}} \quad (14)$$

Where $V_{C(P-P)}$ is the peak to peak worst case high frequency capacitor voltage, and D is the switch duty cycle. The RFI filter that follows C_{IN} has to be able to attenuate $V_{C(P-P)}$ to the levels set by the relevant regulatory specifications.

INPUT TRANSIENT OVERVOLTAGE PROTECTION

Careful examination of the power circuits reveals that there is no large capacitance at the input of the regulator. The only capacitance present is that of the RFI filter capacitors. These capacitors have a combined value in the range of a few microfarads, and their ability to absorb and minimize any line induced transients is almost nonexistent. Transients can also occur under sudden load removal. If the line impedance is inductive, hazardous drain-source voltages may be generated leading to the destruction of the power MOSFET. To keep this from happening, a transient over-voltage protection device should be installed such that enough safety margin is allowed for the power MOSFET. A good rule of thumb is:

$$BV_{DSS} > V_{CLAMP} + V_{OUT(OVP)} \quad (15)$$

Where BV_{DSS} is the drain-source breakdown voltage for the MOSFET, V_{CLAMP} is the activation or clamping voltage of the over-voltage transient protector, and $V_{OUT(OVP)}$ is the maximum output voltage which is set by the OVP function of the controller.

THE OUTPUT CIRCUIT

The output circuit for this topology, although non-isolated, does not share the same ground with the power circuit. Therefore connecting the two grounds with the measuring leads of instruments should be avoided.

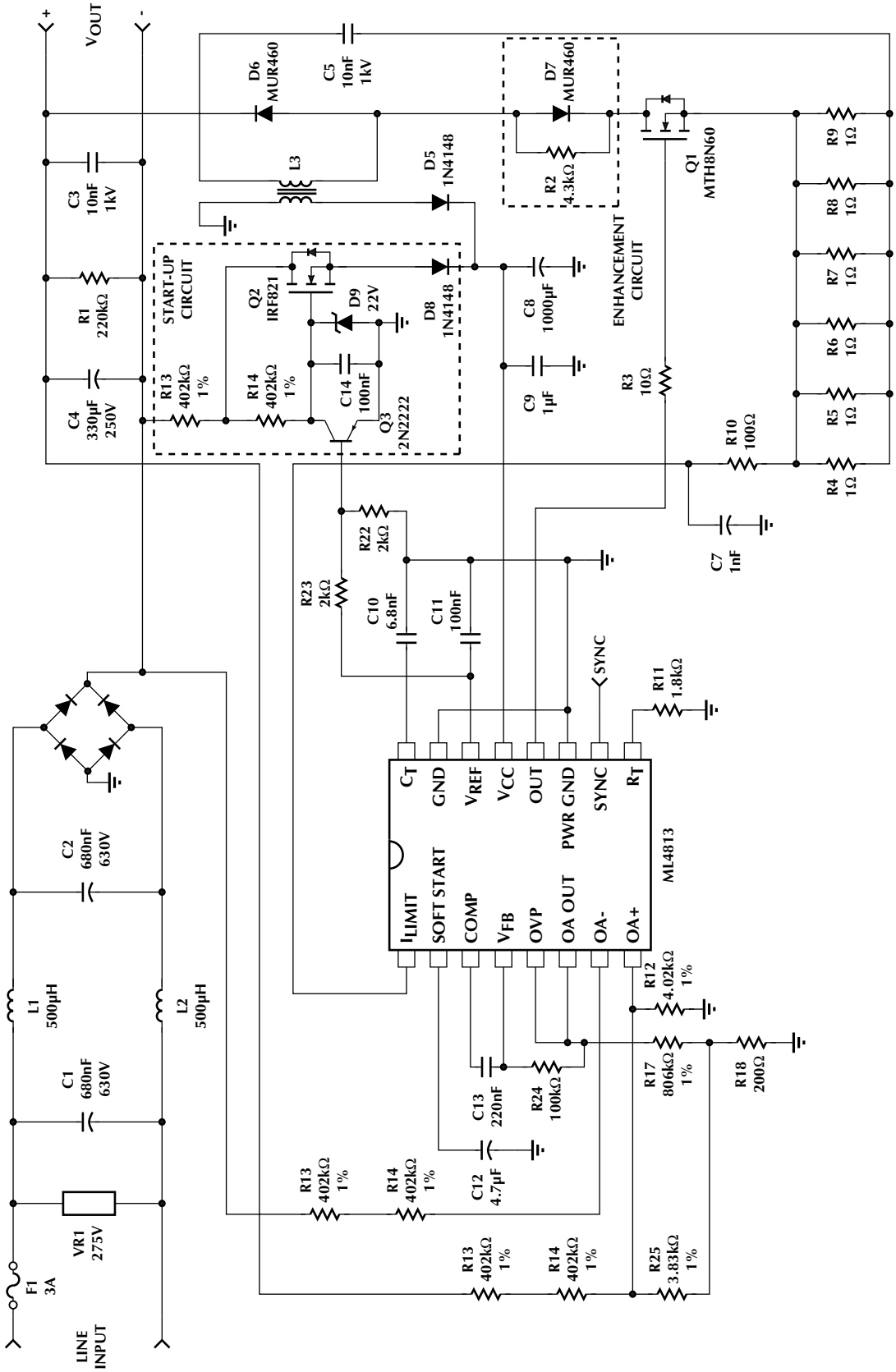


Figure 9. 80W Flyback Power Factor Regulator Using the ML4813

APPLICATIONS (Continued)

The output voltage "rides" on the input voltage when the (+) output is measured with respect to PWR GND as shown in Figure 10.

The extra op amp provided in the ML4813 can be used to sense the output voltage for regulation and overvoltage conditions. This op amp is connected as a difference amplifier with its output referenced to PWR GND. Resistors RH1, RH2, RL1, RL2 are used to scale down the voltage.

Normally, RH1 = RH2 = RH and RL1 = RL2 = RL. The voltage designated as V_S in Figure 7 is given by:

$$V_S = V_{OUT} \times \frac{RL}{RH + RL} \quad (16)$$

The output capacitance should be calculated such that it has the required output ripple at the worst case operating point. In addition, the ESR should be sufficiently low to prevent excessive dissipation due to RMS currents. The first criterion can be met by choosing the value of the output capacitor based on the following:

$$C_{OUT} \geq \frac{P_{IN}}{2\pi f_L \times \Delta V_R \times V_{OUT}} \quad (17)$$

Where:
C_{OUT} = Total output capacitance
P_{IN} = Total input power
ΔV_R = Peak output capacitor ripple voltage
f_L = Line frequency times 2 (120 for 60Hz line)

The second criterion for the selection of the output capacitor can be satisfied by choosing a component with adequately low ESR value that can safely bypass the RMS currents.

OUTPUT DIODE

The output diode can be a "fast" or ultrafast' type depending on the operating frequency. Reverse recovery losses are low since under normal operating conditions, the regulator operates in discontinuous current mode. The diode should be rated to handle the maximum output current. The resulting power dissipation will be the forward drop of the diode times the output current.

POWER SWITCH

If a power MOSFET is used, it should be sized for the required efficiency. Lower $R_{DS(ON)}$ devices will yield lower losses, but if they are operated at high frequencies (100kHz), higher charge dumping losses will be experienced. The RMS current value through the power FET and the sensing resistor is:

$$I_{RMS} = \sqrt{\frac{L \times I_P^3 \times f_L}{4.24 \times V_{RMS}}} \times \sqrt{\sum_{k=1}^{r} \sin^2 \frac{k\pi}{r}} \quad (15)$$

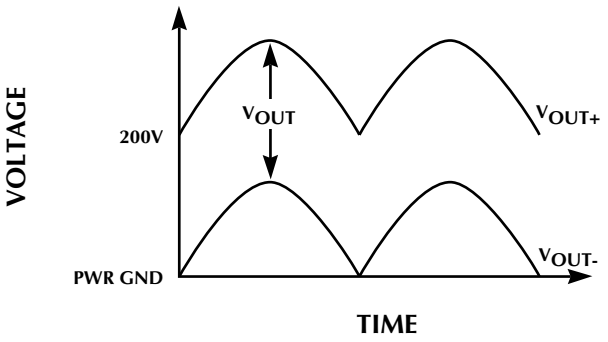


Figure 10. Output Voltage with Respect to PWR GND

Where:
I_{RMS} = Total RMS current through the power MOSFET
f_L = Line frequency times 2 (120 for 60Hz line)
$r = f_{SWITCH}/f_L$

Table 1 is provided to assist in calculating (18). When the power switch is a bipolar transistor (constant V_{CE} drop), then the power dissipation produced can be calculated by:

$$P_D = \frac{0.9 \times P_{IN}}{V_{RMS}} \times V_{CE} \quad (19)$$

Where:
P_D = Power dissipation in the transistor
V_{RMS} = RMS value of the minimum input voltage
V_{CE} = Forward drop of the power transistor

f_{SWITCH} (kHz)	r	$\sqrt{\sum_{k=1}^{r} \sin^2 \frac{k\pi}{r}}$
20	167	9.1
30	250	11.2
40	333	12.9
50	417	14.4
60	500	25.8
70	583	17.1
80	667	18.3
90	750	19.4
100	833	20.4
110	917	21.4
120	1000	22.4
130	1083	23.3
140	1167	24.2
150	1250	25.0
160	1333	25.7
170	1417	26.5
180	1500	27.3
190	1583	28.0
200	1667	28.9

Table 1. Constants for Calculating IRMS (Equation 18)

APPLICATIONS (Continued)

OFF-LINE START-UP AND BIAS SUPPLY GENERATION

A fast starting circuit is included in Figure 9. MOSFET Q2 quickly charges the ML4813 V_{CC} capacitor (C8) when the supply is initially turned on. This allows the supply to come on less than 1 second after AC power is applied. A simpler start-up circuit may be used which replaces the active circuit with a 39kΩ, 2W resistor but starts more slowly (up to 15 seconds under low line conditions). Systems which do not require quick starting can reduce cost with the latter start-up method.

POWER FACTOR ENHANCEMENT

Some combinations of line and load may exhibit distortion of the input current waveform. This distortion is usually caused by the inductor "ringing" with the C_{DS} of the power MOSFET, resulting in a non-zero inductor current at the beginning of the next cycle. This ringing can be dampened by using R2 and D7 as shown in Figure 9. Applications which can get by with slightly worse power factor can eliminate these components.

ADJUSTING THE OUTPUT VOLTAGE

The error amplifier creates an error voltage from the difference between the output voltage presented at OA OUT and the 5V internal reference. Since the output voltage is not ground referenced, the ML4813's internal op amp is connected as an instrumentation amplifier as shown in Figure 11.

The output voltage is set by resistors which determine the relationship between (V_{OUT+} - V_{OUT-}) and the output of the op amp. For the following discussion, R15' = R15 + R16 and R14' = R13 + R14. The differencing amplifier depends on the following relationships:

$$R14' = R15'$$

$$R12 = R25 + (R17 \,||\, R18)$$

Then:

$$V_{OUT} = \left(\frac{5V + R18}{R17 + R18}\right) \times \left(\frac{R15'}{R15' + R25}\right) \times \left(\frac{R14'}{R12} + 1\right) \quad (20)$$

Since R25 is a low value compared to R15', the second term reduces to approximately 1. The third term is set at approximately 200. Equation (20) can be reduced to:

$$V_{OUT} \cong 1000 \times \left(\frac{R18}{R17 + R18}\right) \quad (21)$$

The overvoltage comparator has a threshold that is set for 1.12 x V_{OUT} when OVP and OA OUT are connected directly. Figure 12 shows the connection for setting an OVP trip point higher than 1.12 x V_{OUT}, where:

$$V_{OVP} \cong 1.12 \times V_{OUT} \times \left(\frac{R_A + R_B}{R_B}\right) \quad (22)$$

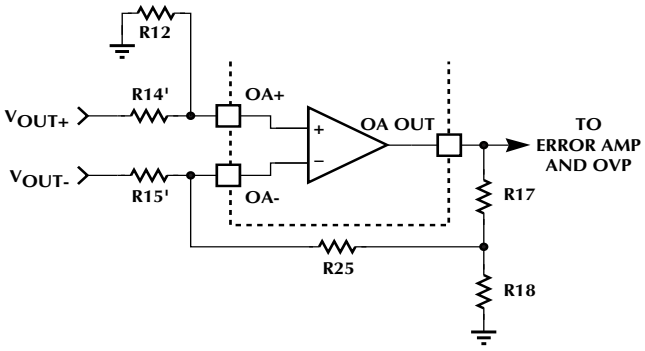


Figure 11. Ground Referencing the Op Amp Output

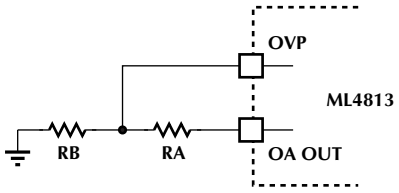


Figure 12. Setting OVP at > 1.12 x V_{OUT}

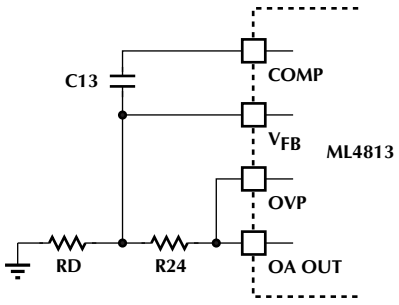


Figure 13. Setting OVP at < 1.12 x V_{OUT}

Figure 15 shows OVP set for a voltage lower than 1.12 x V_{OUT} where:

$$V_{OVP} \cong 1.12 \times V_{OUT} \times \left(\frac{RD + R24}{RD}\right) \quad (23)$$

APPLICATIONS (Continued)

INDUCTOR INFORMATION

L3 is the flyback inductor and also provides the operating power for the control circuitry. A gapped ferrite pot core was chosen for this application for it's modest high frequency losses with high ripple current operation. Some possible choices are:

Manufadurer	Part #	Total Gap	N_P
Magnetics Inc.	F43019	0.05"	32
Phillips	3019 PL00-3F3	0.05"	32
Phillips	3019 PA125-3C8	0.07"	38

The first 2 cores are sold ungapped and require the use of a .025. spacer to gap the center leg to yield a total gap length of 0.05". If an ungapped core is used, a "shorted turn" should be employed as shown in Figure 14 to prevent radiated EMI. The third core listed is sold with its center ieg pre-gapped (0.07" total) so that the outside of the core closes completely, providing shielding without a shorted turn. N_S should be 3 turns. All windings are #24AWG wire.

Inductors L1 and L2 are constructed using a powdered iron. This is a suitable material for these inductors since the high frequency ripple currents (and resulting flux excursions) are much less severe than for L3. The core selected is a MicroMetals T68-26D with 80 turns or #24AWG wire.

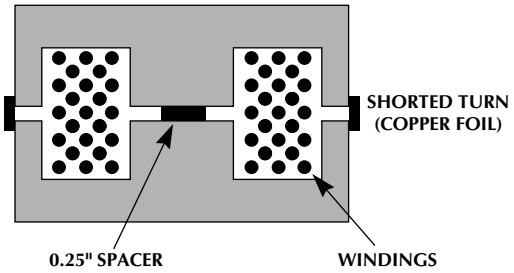
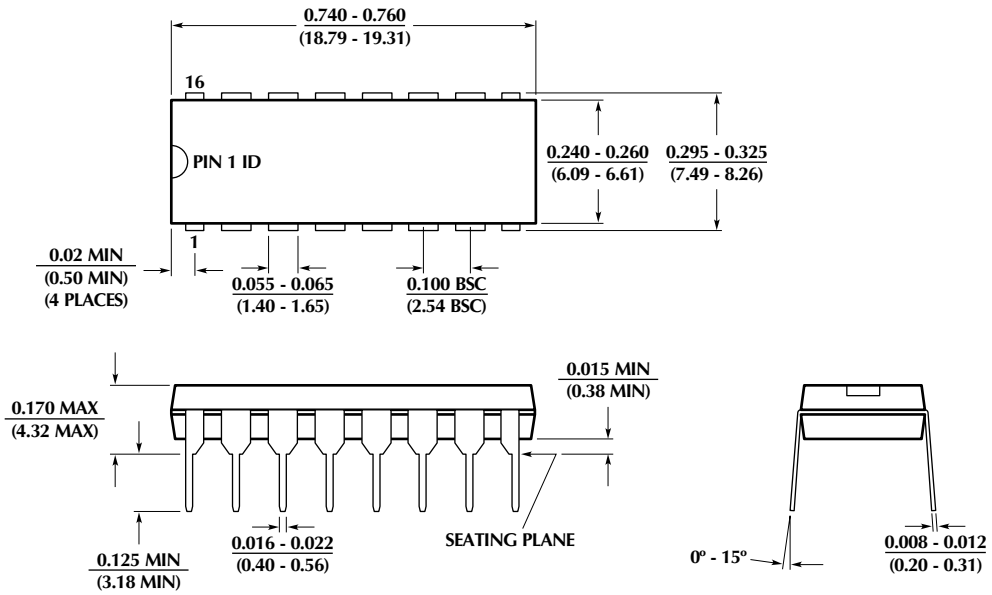


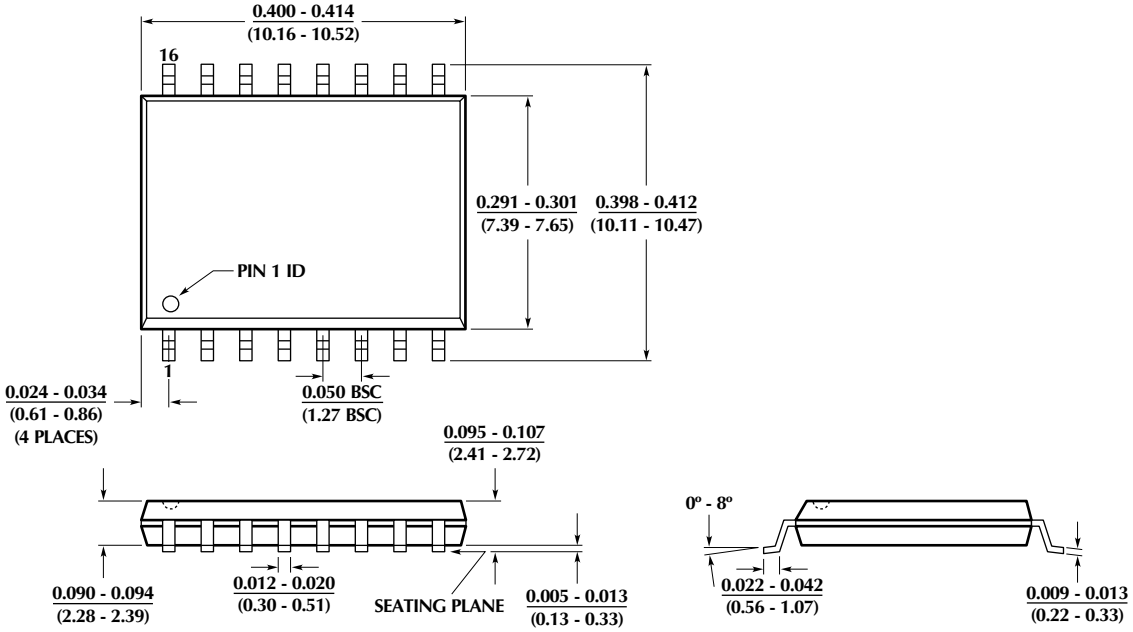
Figure 14. EMI Shielding for Ungapped Cores

PHYSICAL DIMENSIONS inches (millimeters)

Package: P16
16-Pin PDIP



Package: S16W
16-Pin Wide SOIC



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4813CP (EOL) ML4813CS (Obsolete)	0°C to 70°C 0°C to 70°C	16-Pin PDIP (P16) 16-Pin SOIC (S16W)
ML4813IP (Obsolete) ML4813IS (Obsolete)	-40°C to 85°C -40°C to 85°C	16-Pin PDIP (P16) 16-Pin SOIC (S16W)

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