Micro Linear

ML4828*

BiCMOS Phase Modulation/Soft Switching Controller

GENERAL DESCRIPTION

The ML4828 is a complete BiCMOS phase modulation control IC suitable for full bridge soft switching converters. Unlike conventional PWM circuits, the phase modulation technique allows for zero voltage switching (ZVS) transitions and square wave drive across the transformer. The IC modulates the phases of the two sides of the bridge to control output power.

The ML4828 can be operated in either voltage or current mode. Both cycle-by-cycle current limit, integrating fault detection, and soft start reset are provided. The under-voltage lockout circuit features a 1.5V hysteresis with a low starting current to allow off-line start up with a bleed resistor. A shutdown function powers down the IC, putting it into a low quiescent state.

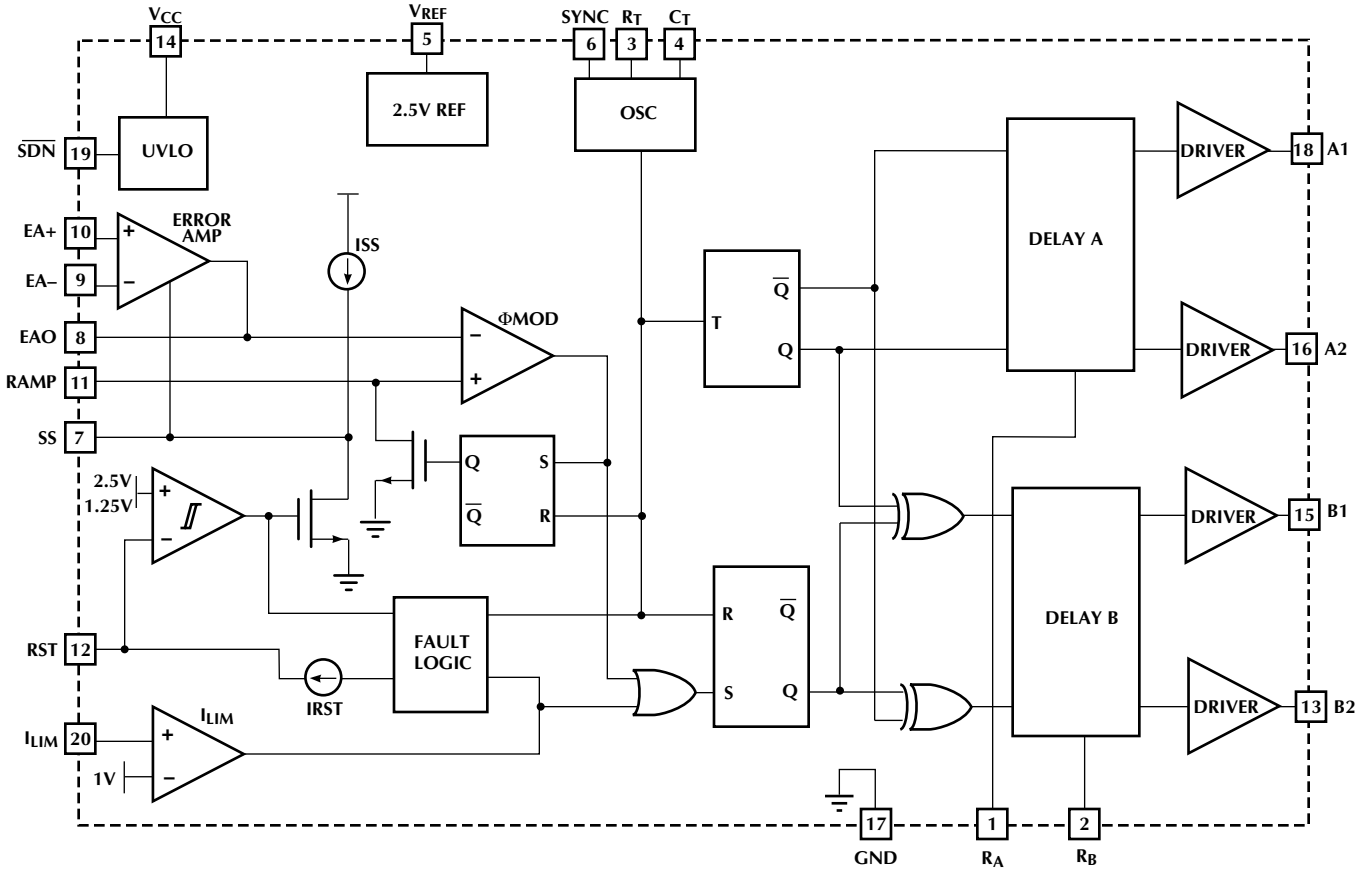
The circuit can be operated at frequencies up to 1MHz. The ML4828 contains four high current CMOS outputs which feature high slew rate with low cross conduction.

FEATURES

- 5V BiCMOS for low power and high frequency (1MHz) operation
- Full bridge phase modulation zero voltage switching circuit with independent programmable delay times
- Current or voltage mode operation capability
- Cycle-by-cycle current limiting with integrating fault detection and restart delay
- Can be externally synchronized
- Four 3Ω CMOS output drivers
- Under-voltage lockout circuit with 1.5V hysteresis

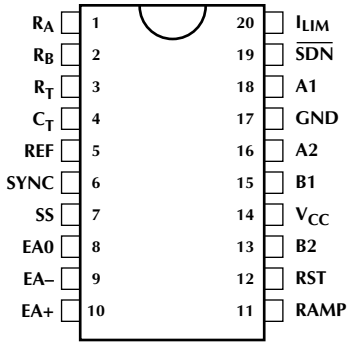
*Some Packages Are End Of Life

BLOCK DIAGRAM



PIN CONNECTION

ML4828
20-Pin DIP (P20)
20-Pin SOIC (S20)



TOP VIEW

PIN DESCRIPTION

PIN	NAME	DESCRIPTION
1	R_A	A1 and A2 delay programming resistor.
2	R_B	B1 and B2 delay programming resistor .
3	R_T	Oscillator charge current programming resistor.
4	C_T	Oscillator timing capacitor.
5	REF	2.5V reference voltage.
6	SYNC	Synchronization input to oscillator.
7	SS	Soft start capacitor connection.
8	EAO	Error amplifier output.
9	EA-	Error amplifier inverting input.
10	EA+	Error amplifier non-inverting input.

PIN	NAME	DESCRIPTION
11	RAMP	RC network for phase modulator ramp input.
12	RST	RC network for reset and integrating fault detect.
13	B2	B2 driver output.
14	V_{CC}	Power supply
15	B1	B1 driver output.
16	A2	A2 driver output.
17	GND	Ground.
18	A1	A1 driver output.
19	$\overline{SHDN}$	Active low device shutdown.
20	I_{LIMIT}	Current limit control input

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

V_{CC} 7V
Output Current, Source or Sink (A1, A2, B1, B2)
  Pulse (0.5 µs) 1.0A
Analog Inputs (EA+, EA–, EAO,
  RST, RAMP, RST) ..... –0.3V to V_{CC} + 0.3V
R_T Source Current ..... –1mA
Error Amplifier Output Current ..... ±2mA
Soft Start Discharge Current 5mA
C_T Charging Current ..... –1mA
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering 10 sec.) ..... 260°C
Thermal Resistance (θ_{JA})
  Plastic DIP ..... 67°C/W
  Plastic SOIC ..... 95°C/W

OPERATING CONDITIONS

Temperature Range
  ML4828CX ..... 0°C to 70°C
  ML4828IX ..... –40°C to 85°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $R_A = R_B = 33.3k\Omega$, $R_T = 16k\Omega$, $C_T = 270pF$, $V_{CC} = 5V$, T_A = Operation Temperature Range (Notes 1,2)

PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
OSCILLATOR					
Initial Accuracy	$T_A = 25°C$	340	360	380	kHz
Voltage Stability	$4.5V < V_{CC} < 5.5V$		4	5.3	%/V
Temperature Stability			2		%
Total Variation	Line, temp.	325		400	kHz
C_T Discharge Current	$V_{CT} = 2V$	1.15	1.5		mA
Ramp Peak			2.6		V
Ramp Valley			1.12		V
REFERENCE					
Initial Accuracy	$T_A = 25°C$, $I_O = 250µA$	2.475	2.5	2.525	V
Line Regulation	$4.5V < V_{CC} < 6.5V$		±0.2	±1	%/V
Load Regulation	100µA to 1mA		±0.5	±6	mV
Temperature Stability			0.45		%
Total Variation	Line, Load, & Temp	2.44		2.54	V
Long Term Stability	$T_J = 125°C$, 1000 hrs		5	25	mV
Short Circuit Current	$V_{REF} = 0V$	–10	–23	–35	mA
ERROR AMPLIFIER					
Input Offset Voltage		–20		20	mV
Input Common-Mode Range		0		1.75	V
Open Loop Gain	$1V < V_O < 2.7V$	60	80		dB
PSRR	$4.5V < V_{CC} < 6.5V$	60	80		dB
Output Sink Current	$V_O = 0.5V$	1.2	1.9		mA
Output Source Current	$V_O = 2.7V$	–0.35	–1.1		mA
Output High Voltage	$I_{SOURCE} = –500µA$	2.6	2.85		V
Output Low Voltage	$I_{SINK} = 500µA$		0.1	0.2	V
Unity Gain Bandwidth		7	10		MHz
Slew Rate		5	10		V/µs

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
PHASE MODULATOR					
EAO Zero Duty Cycle Threshold	V_{RT} = 0V	0	0.5	0.9	V
RAMP Delay to Output			50	80	ns
RAMP Discharge Current		48		95	mA
SOFT-START					
Charge Current	V_{SS} = 4V		–25	–50	µA
Discharge Current	V_{SS} = 1V	6	10	13.2	mA
CURRENT LIMIT/SHUTDOWN					
Current Limit Threshold		0.9	1.0	1.1	V
Pin 20 Delay to Output	(Note 1)		50		ns
Pin 12 Shutdown Threshold		1.0	1.1	1.5	V
Pin 12 Restart Threshold		2.2	2.4	2.6	V
Pin 12 Charging Current		–350	–460	–550	µA
$\overline{SDN}$ Shutdown Threshold		1.05	1.6	2.05	V
OUTPUT					
Output Low Level	I_{OUT} = 20 mA I_{OUT} = 100 mA		0.01 0.1	0.1 0.3	V V
Output High Level	I_{OUT} = –20 mA I_{OUT} = –100 mA	4.9 4.6	4.95 4.7		V V
Rise/Fall Time	C_L = 1000pF, (Note 1)		5	7	ns
ZVS Programmable Delay		240	280	315	ns
Delay Mismatch			0		ns
R_A/R_B Reference Voltage		2.45	2.5	2.55	V
UNDER VOLTAGE LOCKOUT					
Start Threshold		5.1	5.85	6.6	V
Stop Threshold		4.1	4.2	4.3	V
SUPPLY					
Start Up Current	V_{CC} < 6V		0.6	1	mA
Shutdown Current			100	500	µA
I_{CC}	V_{CC} = 5V, C_L = 1000pF, T_A = 25°C		5	7	mA

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.
Note 2: V_{CC} must be brought above the UVLO start voltage (6V) before dropping to V_{CC} = 5V to ensure start-up.

FUNCTIONAL DESCRIPTION

PHASE MODULATOR

The ML4828 controls the power of a full bridge power section by modulating the phases of the switches of the A and B sides (Figure 1). The power cycle starts with A2 and B1 high, as shown in the timing diagram (Figure 2).

1. With A2 and B1 high, Q1 and Q2 are ON. Current flows through the primary of the transformer, and power is delivered to the output through the secondary winding (not shown).
2. After either the ΦMOD or I_{LIM} comparator trips, B1 goes low, turning off Q2. Energy in the primary winding charges the parasitic capacitances of Q2 and Q3 to +VIN during t_{DB}.
3. B2 goes high after time t_{DB}, which is set by the resistor connected from RB (pin 2) to GND. t_{DB} should be set large enough such that the source of Q3 has been charged to +VIN. At this time, Q3 turns on at zero voltage. The transformer is now effectively shorted through Q1 and Q3, with the primary magnetizing current circulating in the loop formed by the transformer primary, Q1, and Q3.
4. CLOCK then goes high and A2 goes low, while A1 remains low for time t_{DA}, which is set by the resistor connected from RA (pin 1) to GND. During this time, both Q1 and Q4 are OFF. The primary magnetizing current discharges the parasitic capacitances of Q1 and Q4 to GND.
5. A1 goes high after time t_{DA}. At this point, the drain of Q4 is discharged to GND, and Q4 turns on at zero voltage. With both Q3 and Q4 ON, a new power cycle starts, and power is delivered to the output.

The above sequence is then repeated with the roles of side A and B interchanged.

The ML4828 can also be used in current mode by sensing the load current on the RAMP input (pin 11).

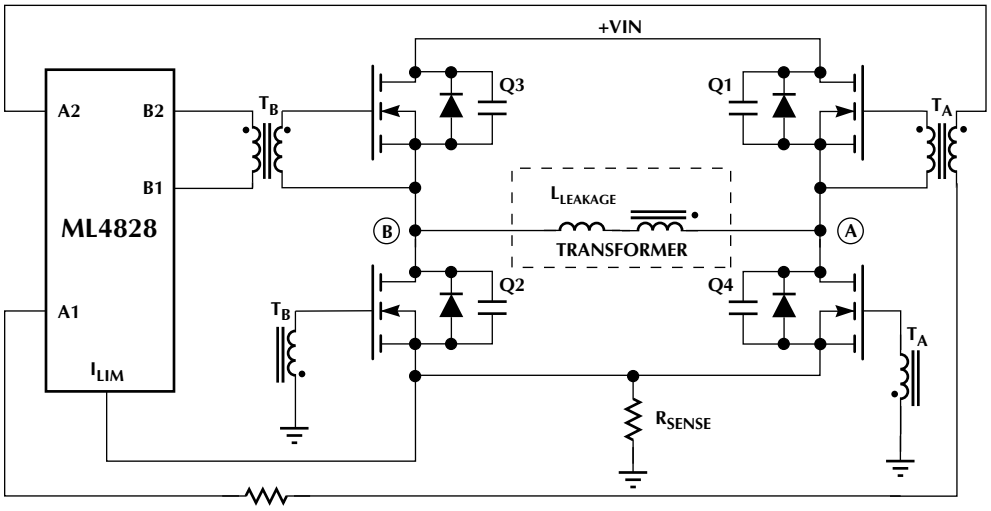


Figure 1. Simplified diagram of Phase Modulated power Outputs.

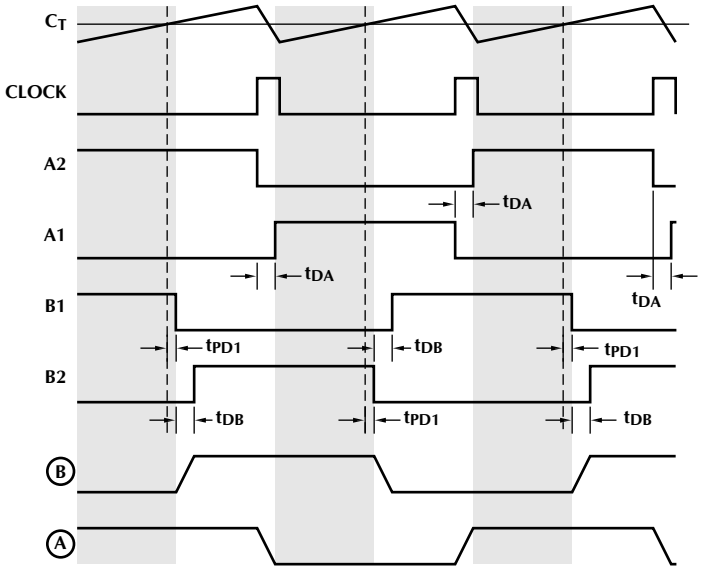


Figure 2. Phase Modulation control waveforms (Shaded areas indicate a power cycle).

SETTING THE OSCILLATOR FREQUENCY

The ML4828 switching frequency is determined by the charge and discharge times of the network connected to the R_T and C_T pins. Figure 3 shows the relationships between the internal clock and the charge and discharge times.

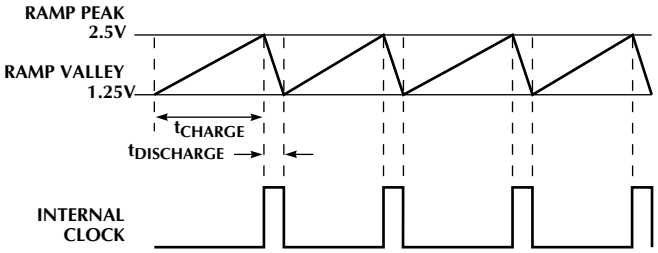


Figure 3. Internal Oscillator Timing.

The frequency of the oscillator is:

$$f_{OSC} = \frac{1}{t_{CHARGE} + t_{DISCHARGE}} \quad (1)$$

The ramp peak is 2.5V and the ramp valley is 1.25V, giving a ramp range of 1.25V. The charging current is set externally through the resistor R_T:

$$I_{CHARGE} = \frac{2.5V}{R_T} \quad (2)$$

while the discharging current is fixed at 1.4 mA. The charge and discharge times can be determined by:

$$t_{CHARGE} = \frac{C_T \times 1.25V}{I_{CHARGE}} = \frac{C_T \times R_T}{2} \quad (3)$$

$$t_{DISCHARGE} = \frac{C_T \times 1.25V}{I_{DISCHARGE}} = \frac{C_T \times 1.25V}{1.4mA} \quad (4)$$

The oscillator frequency can then be found by substituting the results of equations 3 and 4 into equation 1. This frequency activates a T flip-flop which generates the output pulses. The T flip-flop acts as a frequency divider (÷2), so the output frequency will be:

$$f_{OUT} = \frac{f_{OSC}}{2} \quad (5)$$

ERROR AMPLIFIER

The ML4828 error amplifier has a 10MHz bandwidth and a 10V/µs slew rate. Figure 4 gives the Bode plot of the error amplifier.

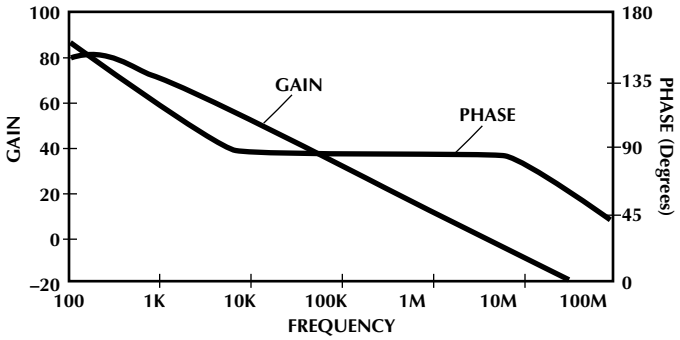


Figure 4. Error Amplifier Open-Loop Gain and Phase vs. Frequency.

OUTPUT DRIVERS

The ML4828 has four high-current CMOS output drivers, each capable of 1A peak output current. These outputs have been designed to quickly switch the gates of power MOSFET transistors via a gate drive transformer. For higher power applications, the outputs can be connected to external MOSFET drivers.

The output phase delay times are set by charging an internal 6.7pF capacitor up to the REF voltage (2.5V) via a current that is externally programmed through R_A and R_B, for the side A and side B drivers, respectively. The charging current and delay time for side A are given by:

$$I_A = \frac{2.5V}{R_A} \quad (6)$$

$$t_{DA} = 6.7pF \times R_A \quad (7)$$

The same equations can be applied to R_B. For example, with $R_A = 33k\Omega$:

$$t_{DA} = 6.7pF \times 33k\Omega = 220ns \quad (8)$$

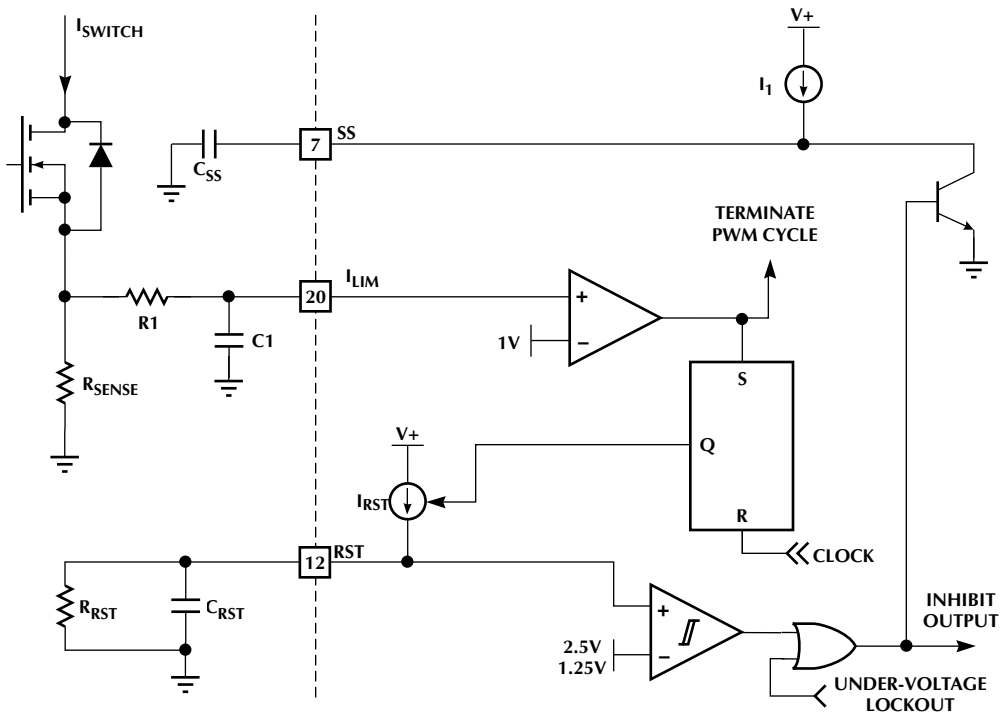


Figure 5. Over-Current, Soft-Start, and Integrating Fault Detect Circuits.

SOFT START TIME CONSTANT

During start up, the output voltage is much lower than the steady state value. Without soft start circuitry, the error amplifier output (EAO) would swing all the way to the upper limit and the phase modulator would issue pulses with full duty cycle, possibly causing output overshoot. To ensure smooth start up, EAO (pin 8) is pulled low and then gradually released through the charging of an external soft start capacitor connected to SS (pin 7). The soft start charging current is internally set at 25µA. Hence, EAO will rise with a time constant of:

$$\frac{dv}{dt} = \frac{25\mu A}{C_{SS}} \qquad (9)$$

For example, with C_{SS} = 25µF, the soft start rate of change will be:

$$\frac{dv}{dt} = \frac{25\mu A}{25\mu F} = 1\frac{V}{s} \qquad (10)$$

FAULT TIME CONSTANT AND RESTART DELAY

Figure 5 shows the internal circuitry and external components involved in fault detection. During normal operation, RST (pin 12) is discharged to ground through the external resistor R_{RST}. The I_{LIM} comparator has a threshold of 1V. R_{SENSE} is selected so that the voltage across it will be equal to the I_{LIM} threshold at the maximum desired I_{SWITCH} current. When the voltage across R_{SENSE} exceeds 1V, the I_{LIM} comparator trips, terminating the present power cycle, and at the same time activating the fault logic to turn on the 500µA current source I_{RST}. This current charges the reset capacitor C_{RST}. For proper design, R_{RST} should be very large (in the order of 100kΩ). This will cause nearly all of the I_{RST} current (approximately 500µA) to go into charging C_{RST} at a rate of:

$$\frac{dv}{dt} = \frac{500\mu A}{C_{RST}} \qquad (11)$$

in volts per second. I_{RST} will be turned off at the beginning of the next clock cycle. If the current limit condition is removed, RST will be gradually discharged to ground, and normal operation resumes as shown in Figure 6.

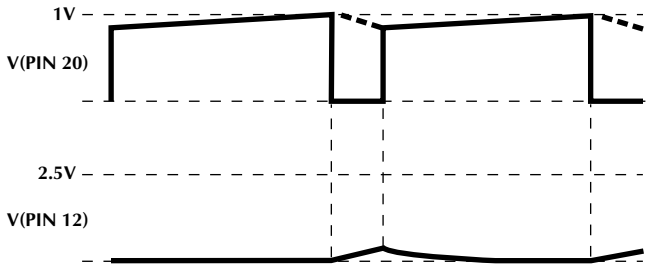


Figure 6. I_{LIM} and Resulting RC_{RST} Waveforms During Load Surge.

If the current limit condition persists, then I_{RST} will be reactivated, thus charging C_{RST} to a higher level as shown in Figure 7. Eventually, the voltage at RST will exceed 2.5V, and the soft start comparator will trip, shutting down all power drivers and inhibiting any further delivery of power. At the same time, the soft start capacitor C_{SS} is discharged to prepare for the next start up cycle.

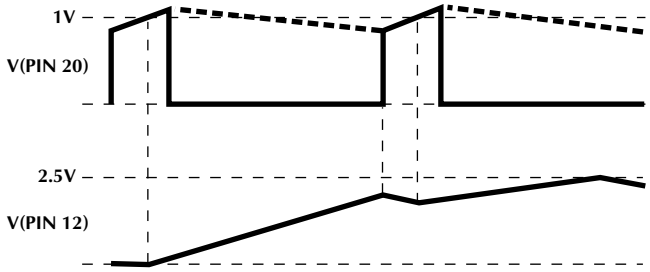


Figure 7. I_{LIM} and Resulting RC_{RST} Waveforms During Short Circuit.

During the I_{LIM} shutdown, I_{RST} is turned off, and C_{RST} is discharged through R_{RST} with a time constant of:

$$t_{RST} = R_{RST} \times C_{RST} \quad (12)$$

When the condition causing the current limit is removed, R_{RST} will discharge C_{RST} with a time constant of t_{RST}. When the voltage at RST (pin 12) drops to 1.25V, the soft start comparator and the converter will undergo a start up cycle. The restart delay ($t_{D(RST)}$) is given by:

$$t_{D(RST)} = t_{RST} \times 1.39 \quad (13)$$

For example, with C_{RST} = 25µF and R_{RST} = 240kΩ:

$$\frac{dv}{dt} = \frac{500\mu A}{25\mu F} = 20\frac{V}{s} \quad (14)$$

and

$$t_{D(RST)} = (240k\Omega \times 25\mu F) \times 1.39 = 8.3s \quad (15)$$

Since the threshold for shutdown is 2.5V, the controller will shut down after approximately 125ms. After the converter recovers form the current limit condition, the controller will reactivate after 8.3s.

UNDERVOLTAGE LOCKOUT

During start-up, the ML4828 draws very little current (typically 150µA) and V_{REF} is disabled. When V_{CC} rises above 6.0V, the internal circuitry and V_{REF} are enabled, and will stay enabled until V_{CC} falls below the 4.5V UV lockout threshold.

SHUTDOWN FUNCTION

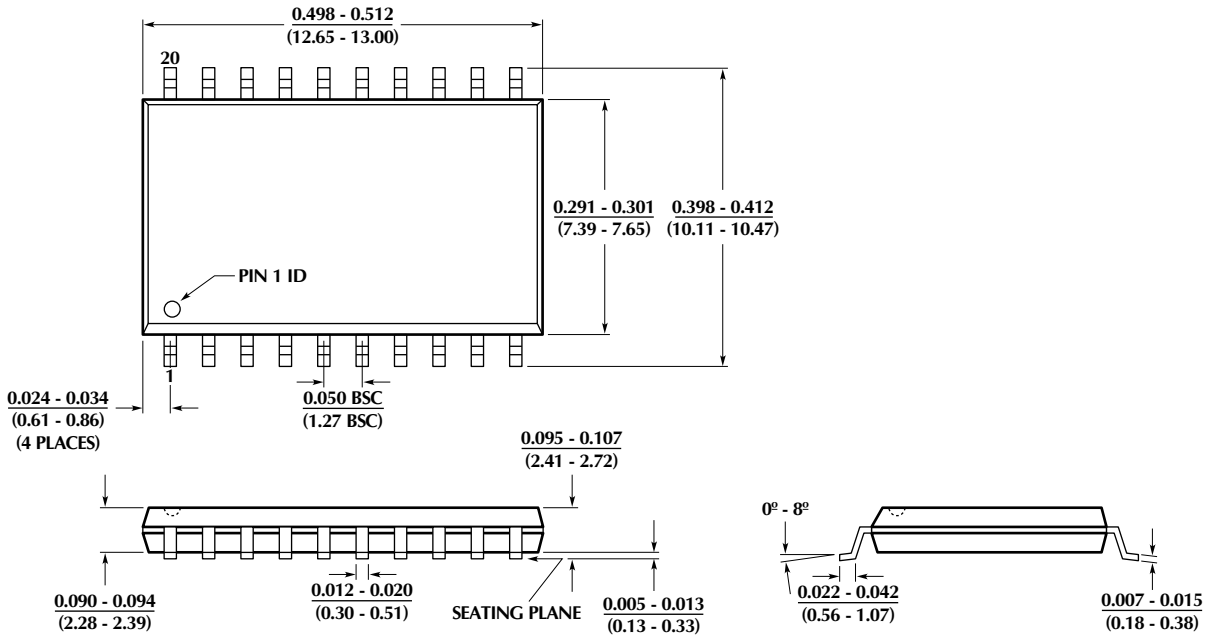
The ML4828 can be externally shut down by bringing SDN (pin 19) low. The shutdown threshold (V_{SD}) is given by

$$V_{SD} = 0.33 \times V_{CC} \quad (16)$$

For example, if V_{CC}= 5V, then V_{SD} = 1.67V. As long as 2.4V < V_{CC} < 6.0V, the SDN pin will be TTL compatible.

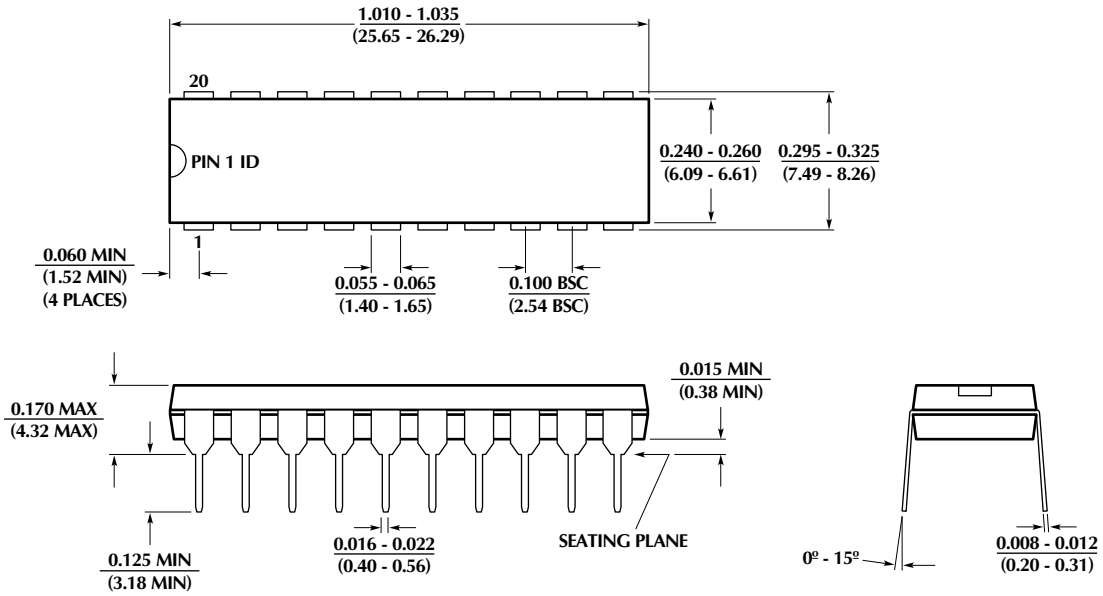
PHYSICAL DIMENSIONS inches (millimeters)

Package: S20
20-Pin SOIC



PHYSICAL DIMENSIONS inches (millimeters) (Continued)

Package: P20
20-Pin PDIP



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4828CP	0°C to 70°C	20-Pin DIP (P20)
ML4828CS	0°C to 70°C	20-Pin DIP (S20) (EOL)
ML4828IP	–40°C to 85°C	20- Pin DIP (P20) (EOL)
ML4828IS	–40°C to 85°C	20- Pin SOIC (S20) (EOL)

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