STRUCTURE Silicon Monolithic Integrated Circuit

FEATURE 1ch Pre-driver for 125KHz LF antenna (Built-in driving current adjustment function)

TYPE **BD6934FV**

FUNCTION
- Driving current adjustment function (Dependence power supply voltage)
- Stand-by current 0 μA (Typ.)

●Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	Rating	Unit
Supply voltage	VCC1,VCC2	12	V
Power dissipation	Pd	562 *	mW
Operating temperature range	T_{opr}	-40～85	℃
Storage temperature range	T_{stg}	-55～150	℃
Junction temperature	T_{jmax}	150	℃

* Reduced by 4.496mW/℃,when mounted on a glass epoxy board (70mm×70mm×1.6mm)

●Operating range (Ta=-40～85℃)

Parameter	Symbol	Operating range	Unit
Supply voltage	VCC1,VCC2	3.5～8.0	V
RP,RN voltage	Vrp,Vrn	VCC2	V
XOUT,RT,CT voltage	Vxout,Vrt,Vct	VCC1	V
Input voltage	V_{IN},V_{SEL},V_{XIN}	-0.3～VCC1	V

◎This product is not designed for protection against radioactive rays.

* This product described in this specification isn't judged whether it applies to COCOM regulations.
It should not be exported without authorization from the appropriate government.

* Status of this document
The Japanese version of this document is the formal specification.
A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences in translation version of this document, formal version takes priority.

●Electrical characteristics (Unless otherwise specified, VCC1=VCC2=3.5～8.0V,Ta=-40～85℃, RT=4.8kΩ, CT=1000pF)

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
[Circuit current]						
VCC drive current	Icc1	-	3.5	7	mA	IN=High
VCC stand-by current	Icc2	-	-	10	μA	IN=Low
[Output]						
Upper side output voltage H	V_{OHH}	VCC-04	VCC-0.2	-	V	Io=-5mA
Upper side output voltage L	V_{OHL}	-	0.2	0.4	V	Io=5mA
Lower side output voltage H	V_{OLH}	VCC-04	VCC-0.2	-	V	Io=-5mA
Lower side output voltage L	V_{OLL}	-	0.2	0.4	V	Io=5mA
Output leak current H	I_{LH}	-	-	10	μA	VCC1=VCC2=12V,Vo=0V
Output leak current L	I_{LL}	-	-	10	μA	VCC1=VCC2=12V,Vo=12V
ON Duty 3.5V	$D_{ON}3.5$	6.9	9.2	11.5	%	VCC1=VCC2=3.5V
ON Duty 4V	$D_{ON}4$	13	15	17	%	VCC1=VCC2=4V
ON Duty 7V	$D_{ON}7$	44	49	54	%	VCC1=VCC2=7V
Oscillating start time *	T_{OSC}	-	-	8	μsec	
[Input (IN,SEL)]						
Input voltage H	V_{IH}	VCC*0.8	-	-	V	
Input voltage L	V_{IL}	-	-	1.3	V	
Input current H	I_{IH}	10	-	150	μA	V_{IN}=VCC1
Input current L	I_{IL}	-	-	10	μA	V_{IN}=0V
[Under voltage lockout protection]						
UVLD ON voltage	V_{UVON}	2.7	3.0	3.3	V	
UVLD OFF voltage	V_{UVOFF}	2.9	3.2	3.5	V	

* Oscillating start time : Time till operating output, after UVLO turn off during oscillating ceramic resonator.

* Oscillating frequency tolerance : Please refer to the specification of ceramic resonator.
BD6934FV doesn't affect the operating frequency.

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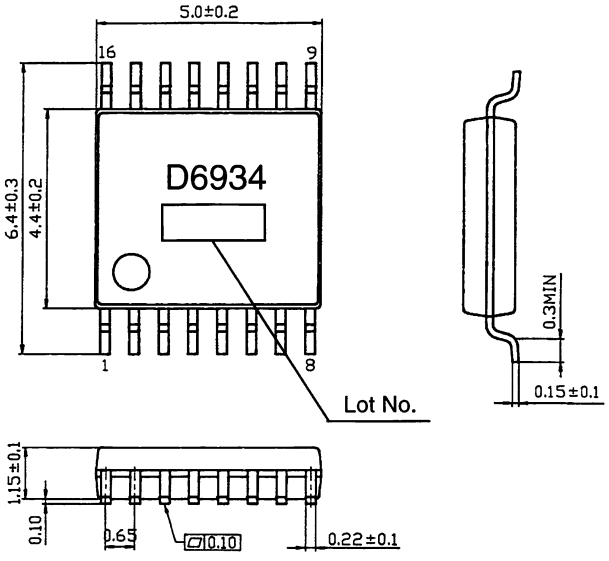
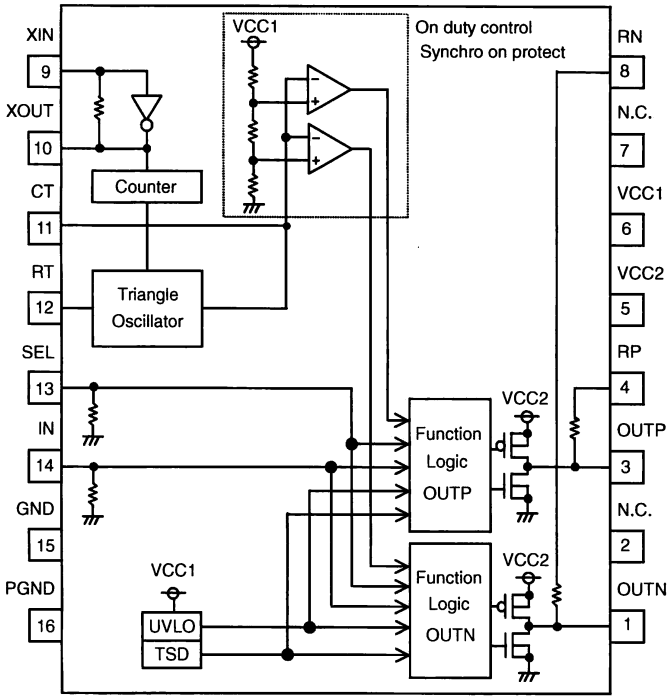
●Dimension



SSOP-B16 (UNIT : mm)

●Block diagram



●Pin name

Pin No.	Pin name
1	OUTN
2	N.C.
3	OUTP
4	RP
5	VCC2
6	VCC1
7	N.C.
8	RN
9	XIN
10	XOUT
11	CT
12	RT
13	SEL
14	IN
15	GND
16	PGND

● OPERATING NOTES

1) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a specialmode where the absolute maximum ratings may be exceeded is anticipated.

2) GND potential

Ensure a minimum GND pin potential in all operating conditions.

3) Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4) Pin short and mistake mounting

Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins and the power supply and GND pins caused by the presence of a foreign object may result in damage to the IC. Ensure a minimum GND pin potential in all operating conditions.

5) Actions in strong magnetic field

Keep in mind that the IC may malfunction in strong magnetic fields.

6) Testing on application boards

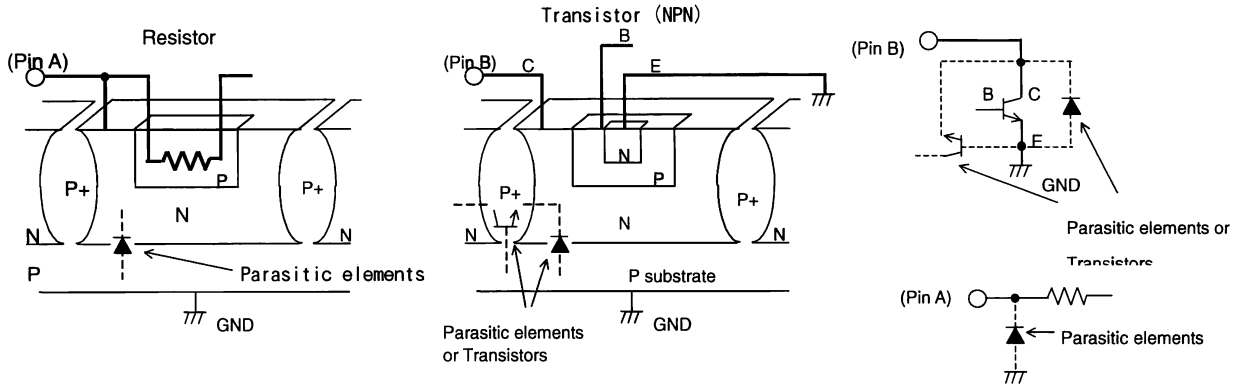
When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC.

7) This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements. For example, when the resistors and transistors are connected to the pins as shown in the following figure,

○The P/N junction functions as a parasitic diode when GND > Pin A for the resistor or GND > Pin B for the transistor(NPN).

○Similarly, when GND > Pin B for the transistor (NPN), the parasitic diode described above combines with the N layer of other adjacent elements to operate as a parasitic NPN transistor.

The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements, such as by the application of voltages lower than the GND (P substrate) voltage to input pins. Keep in mind that the IC may malfunction in strong magnetic fields.



8) Ground patterns

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external parts, either.

9) Thermal shutdown circuit (TSD)

This IC incorporates a built-in TSD circuit for the protection from thermal destruction. The IC should be used within the specified power dissipation range. However, in the event that the IC continues to be operated in excess of its power dissipation limits, the attendant rise in the junction temperature (Tj) will trigger the TSD circuit to turn off all output power elements. The circuit automatically resets once the junction temperature (Tj) drops. Operation of the TSD circuit presumes that the IC's absolute maximum ratings have been exceeded. Application designs should never make use of the TSD circuit.

10) External parts

Driving current adjustment function in use low accuracy parts (Especially, RT terminal connection resistance, CT terminal connection capacitor and resonator) may malfunction.

The external parts use highly accuracy, and be careful additional impedance and capacitor for wiring pattern.

11) RP, RN terminal

The resistance is built in between OUTP and RP, and OUTN and RN to turn off external MOS - FET in stand - by.

Please wire with RP=VCC2 and RN =PGND.

Improper wiring may result in damage for the penetration current.

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