

STRUCTURE Silicon monolithic integrated circuit

PRODUCT SERIES Motor driver for ink jet printer

(H-bridge driver 2ch, switching regulator 1ch, reset output)

TYPE BD64560EUV

FUNCTION • External reset input terminal function

· Built-in thermal shut down circuit

· Built-in UVLO circuit

OAbsolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limit	Unit	
Supply voltage	V <sub>M</sub>	-0.4~40.0	V	
Logic input voltage	$V_L$	-0.4~5.5	V	
RNF voltage (DC)	$V_{RNF}(DC)$	0.5	V	
Dower dissination	Pd	1.70 <sup>*1</sup>	W	
Power dissipation		4.32 <sup>**2</sup>	] VV	
Operating temperature range	T <sub>opt</sub>	-25~+85	Ĵ	
Storage temperature range	T <sub>stg</sub>	-55 <b>~</b> +150	Ĵ	
Junction temperature	T <sub>jmax</sub>	150	Ĵ	
Motor driver maximum output current (peak500ns)	I <sub>out</sub> (peak)	8.0	А	
Motor driver maximum output current (DC)	I <sub>out</sub> (DC)	2.5 <sup>**3</sup>	Α	
Switching Reg maximum output current (DC)	l <sub>out</sub>	1.5	А	

<sup>\*1 70</sup>mm×70mm×1.6mm glass epoxy board. Derating in done at 13.6mW/°C for operating above Ta=25°C.

## ORecommended operating conditions (Ta= -25~+85°C)

Parameter	Symbol	Limit	Unit
Supply voltage	$V_{M}$	7~36	٧
CLK input frequency	f <sub>CLK</sub>	1~25	MHz
Switching Reg output voltage range	V <sub>OUT</sub>	1~V <sub>M</sub> ×0.5	V

This product isn't designed for protection against radioactive rays.

#### Status of this document

If there are any differences in translation version of this document, formal version takes priority.

<sup>\*\*2 4-</sup>layer recommended board. Derating in done at 34.6mW/°C for operating above Ta=25°C.

<sup>&</sup>lt;sup>\*\*3</sup> Do not, however exceed Pd, ASO and Tjmax=150°C.

The Japanese version of this document is the formal specification.

A customer may use this translation version only for a reference to help reading the formal version.

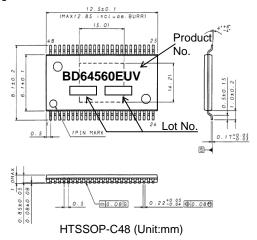


OElectrical characteristics (Unless otherwise specified, Ta=25°C, V<sub>M</sub>=32V)

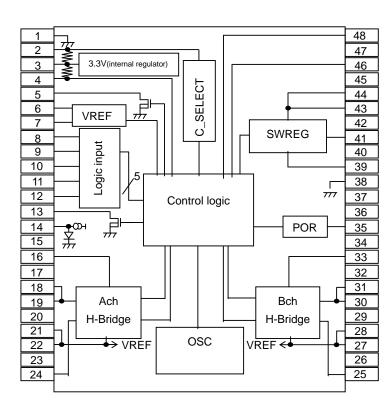
Dansonto	cs (Unless otherwise specified, 1a=25 C, V <sub>M</sub> =32V)  mater  Sumbol  Limit			11.2	Conditions	
Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Overall						
VM current 1	I <sub>M1</sub>	-	-	2	mA	SLEEP=L SWREG=OFF
VM current 2	I <sub>M2</sub>	-	-	15	mA	SLEEP=H SWREG=Max Duty
Control logic (C_SELECT, IRT, SLEE	P. STROBE/E	NABLE /	A. CLK/P	HASE A	. DATA	
High input voltage	V <sub>LINH</sub>	2.0	-	5.5	V	
Low input voltage	V <sub>LINL</sub>	0	-	0.8	V	
Input current	I <sub>LIN</sub>	15	33	50	uA	Input voltage=3.3V
C_SELECT Low input voltage	V <sub>CSELL</sub>	0	-	0.8	V	1
C_SELECT Middle input voltage	V <sub>CSELM</sub>	1.20	1.65	2.10	V	
C_SELECT High input voltage	V <sub>CSELH</sub>	2.5	3.3	-	V	
C_SELECT input current	I <sub>CSEL</sub>	-45	-33	-21	uA	C_SELECT=0V
IRT High input voltage	V <sub>IRTH</sub>	2.0	-	5.5	V	
IRT Low input voltage	V <sub>IRTL</sub>	0	-	0.8	V	
IRT input current	I <sub>IRT</sub>	-50	-33	-15	uA	IRT=0V
H bridge	1					
Output on resistance (High side)	Ronh	-	0.70	0.84	Ω	I <sub>OUT</sub> =1A
Output on resistance (Low side)	R <sub>ONL</sub>	-	0.50	0.60	Ω	I <sub>OUT</sub> =1A
Output leak current (High side)	I <sub>LEAKH</sub>	-1	-	1	uA	V <sub>M</sub> =40V、OUTxx=0V
Output leak current (Low side)	I <sub>LEAKL</sub>	-1	-	1	uA	V <sub>M</sub> =OUTxx=40V
RNF pin outflow current	I <sub>RNF</sub>	10	20	30	uA	
VREF-RNF offset voltage	V <sub>OFST</sub>	-5	0	5	%	VREF=2V GAIN=1/10 or 1/20
	<b>※</b> V <sub>OEST</sub> ={(V	RFF x GA	IN-RNE	thresho	ld volta	ige) / (VREF × GAIN)} × 100
VREF voltage range	V <sub>VREF</sub>	0.8	-	3.0	V	Solve Critical and
VREF pin outflow current	I <sub>VREF</sub>	-1	0	1	uA	VREF=2V
High motor UVLO voltage	V <sub>UVLOH</sub>	13.5	15.0	16.5	V	VICE1 - 2 V
Low motor UVLO voltage	VUVLOL	12.5	14.0	15.5	V	
Switching regulator	VOVLOL	12.0	1 1.0	10.0	•	
FB threshold voltage	$V_{FB}$	0.873	0.900	0.927	V	
FB pin outflow current	I <sub>FB</sub>	-1	0	1	uA	
Output on resistance		-	0.70	0.84	Ω	I <sub>OUT</sub> =0.5A
Leak current	R <sub>ONSW</sub>	-1	0.70	1	uA	$V_{M}=40V$ , SWOUT=0V
FB over voltage protection	V <sub>FBOVP</sub>	1.10	1.20	1.30	V	Disabled at turn on
FB under voltage protection	VFBUVP	0.55	0.60	0.65	V	Disabled at turn on
ORT pin	V FBUVP	0.55	0.00	0.00	V	Disabled at talli on
Output voltage	V <sub>ORT</sub>	_	_	0.4	V	I <sub>DRAIN</sub> =5mA
Leak current	I <sub>LEAKORT</sub>	-1	0	1	uA	IDRAIN-OTTIV
VM threshold voltage					V	No hystorosis
	$V_{POR}$	5.9	6.3	6.7	V	No hysteresis
L_OUT pin	W			0.5	V	I –5mΛ
Output voltage	V <sub>LOUT</sub>	-	-	0.5	-	I <sub>DRAIN</sub> =5mA
Leak current	I <sub>LEAKLOUT</sub>	-1	0	1	uA	



## OPackage outline



# OBlock diagram



OPin No. / Pin name

)Pin No. / Pin name					
Pin name	Pin	Pin name			
LGND		TEST2			
	_	NC			
		TEST1			
	45	NC			
	44	VMSW			
VREFA	43	VMSW			
VREFB	42	NC			
SLEEP	41	SWOUT			
STROBE /ENABLE_A	40	NC			
CLK /PHASE_A	39	FB			
DATA /PHASE_B	38	AGND			
ENABLE_B	37	NC			
L_OUT	36	NC			
TJMON	35	VM			
NC	34	NC			
OUTAM	33	OUTBM			
NC	32	NC			
VMA	31	VMB			
VMA	30	VMB			
NC	29	NC			
RNFA	28	RNFB			
RNFA	27	RNFB			
NC	26	NC			
OUTAP	25	OUTBP			
	Pin name  LGND  C_SELECT  CC  IRT  ORT  VREFA  VREFB  SLEEP  STROBE /ENABLE_A  CLK /PHASE_A  DATA /PHASE_B  ENABLE_B  L_OUT  TJMON  NC  OUTAM  NC  VMA  VMA  VMA  NC  RNFA  RNFA  RNFA  NC	Pin name         Pin No.           LGND         48           C_SELECT         47           CC         46           IRT         45           ORT         44           VREFA         43           VREFB         42           SLEEP         41           STROBE /ENABLE_A         40           CLK /PHASE_A         39           DATA /PHASE_B         37           L_OUT         36           TJMON         35           NC         34           OUTAM         33           NC         32           VMA         31           VMA         30           NC         29           RNFA         28           RNFA         27           NC         26			

NC: Non Connection



#### **OOperation Notes**

#### (1) Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

### (2) Power supply lines

As return of current regenerated by back EMF of motor happens, take steps such as putting capacitor between power supply and GND as an electric pathway for the regenerated current. Be sure that there is no problem with each property such as emptied capacity at lower temperature regarding electrolytic capacitor to decide capacity value. If the connected power supply does not have sufficient current absorption capacity, regenerative current will cause the voltage on the power supply line to rise, which combined with the product and its peripheral circuitry may exceed the absolute maximum ratings. It is recommended to implement a physical safety measure such as the insertion of a voltage clamp diode between the power supply and GND pins.

## (3) GND potential

The potential of GND pin must be minimum potential in all operating conditions.

(4) Metal on the backside (Define the side where product markings are printed as front)

The metal on the backside is shorted with the backside of IC chip therefore it should be connected to GND. Be aware that there is a possibility of malfunction or destruction if it is shorted with any potential other than GND.

## (5) Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions. This IC exposes its frame of the backside of package. Note that this part is assumed to use after providing heat dissipation treatment to improve heat dissipation efficiency. Try to occupy as wide as possible with heat dissipation pattern not only on the board surface but also the backside.

(6) Actions in strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

(7) ASO

When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO.

(8) Thermal shutdown circuit

The IC has a built-in thermal shutdown circuit (TSD circuit). If the chip temperature becomes Tjmax=150°C, and higher, coil output to the motor and regulator output will be OFF, and reset output will be L. The TSD circuit is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect or indemnify peripheral equipment. Do not use the TSD function to protect peripheral equipment.

(9) Ground Wiring Pattern

When using both large current and small signal GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

(10) TEST pin

Be sure to leave TEST1 pin open and connect TEST2 pin to GND.

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Appendix-Rev4.0