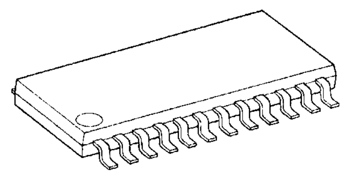
TOSHIBA Bi−CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

TB6504F/FG

PWM CHOPPER TYPE BIPOLAR STEPPING MOTOR DRIVER

The TB6504F/FG is PWM chopper type sinusoidal micro step bipolar stepping motor driver.
Sinusoidal micro step operation is accomplished only a clock signal inputting by means of built−in hard ware.



SSOP24-P-300-1.00

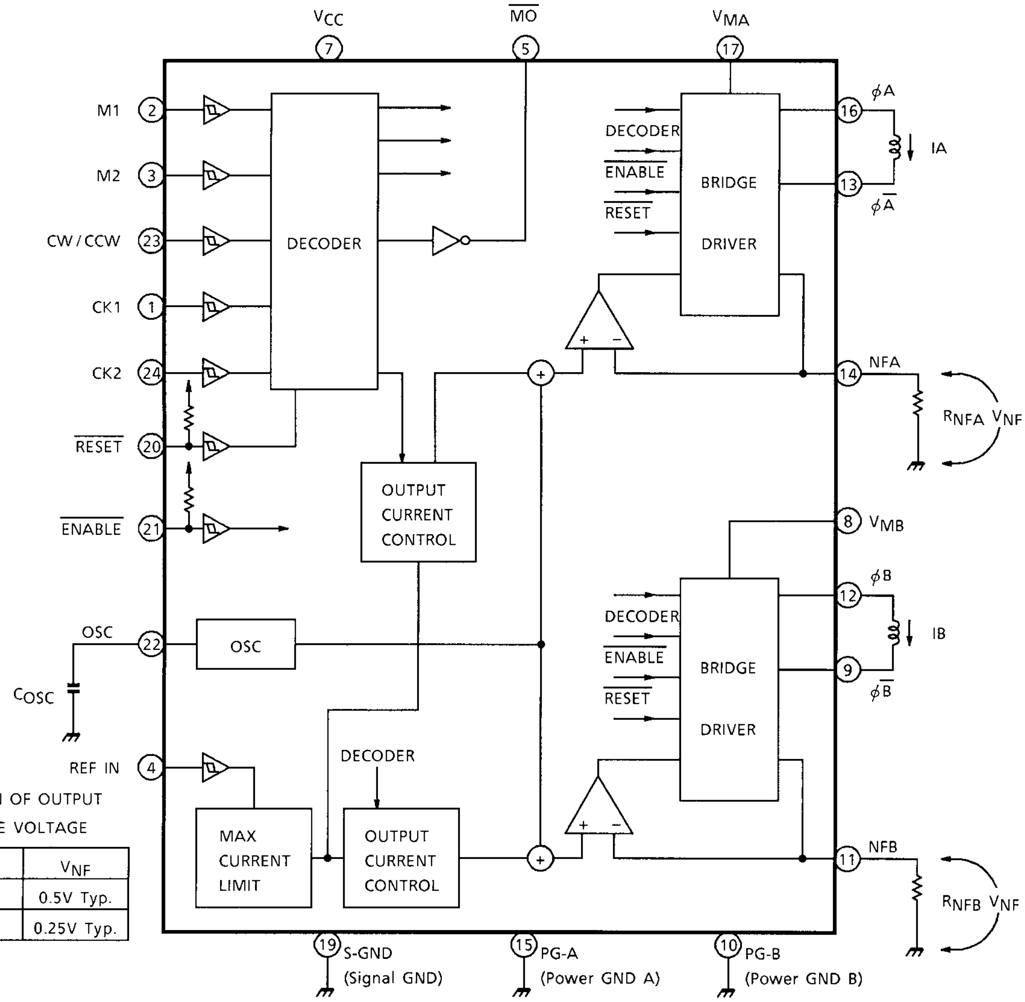
Weight : 0.32 g (Typ.)

FEATURES

- 1 chip bipolar sinusoidal micro step stepping motor driver.
- Output Current up to 150 mA
- PWM chopper type.
- Structured by high voltage Bi−CMOS process technology.
- Forward and reverse rotation are available.
- 2, 1−2, W1−2, 2W1−2 phase 1 or 2 clock drives are selectable.
- Package : SSOP24−P−300−1.00
- Input Pull−Up Resistor equipped with RESET and ENABLE Terminal : R = 200 kΩ (Typ.)
- Output Monitor available with $\overline{MO}$.$I_{O(\overline{MO})}$= ±2 mA MAX.
- Reset and Enable are available with $\overline{RESET}$ and $\overline{ENABLE}$.

TB6504FG:
The TB6504FG is a Pb-free product.
The following conditions apply to solderability:
*Solderability
1. Use of Sn-37Pb solder bath
   *solder bath temperature = 230°C
   *dipping time = 5 seconds
   *number of times = once
   *use of R-type flux
2. Use of Sn-3.0Ag-0.5Cu solder bath
   *solder bath temperature = 245°C
   *dipping time = 5 seconds
   *the number of times = once
   *use of R-type flux

BLOCK DIAGRAM



SELECTION OF OUTPUT REFERENCE VOLTAGE

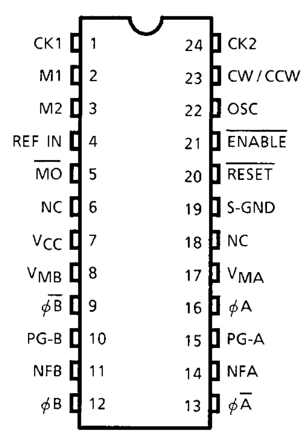
REF IN	V_{NF}
H	0.5V Typ.
L	0.25V Typ.

Pull−up Resistance pin (20), (21) : 200 kΩ (Typ.)
pin (6), (18) : Non Connection

PIN FUNCTION

PIN No.	SYMBOL	FUNCTIONAL DESCRIPTION	
1	CK1	Clock signal input terminal.	TRUTH TABLE A
2	M1	Excitation control input.	TRUTH TABLE B
3	M2	Excitation control input.	
4	REF IN	V_{NF} control input. High Level ; V_{NF} = 0.5 V, Low Level ; V_{NF} = 0.25 V	
5	$\overline{MO}$	Monitor output.	
6	NC	No connection.	
7	V_{CC}	Supply voltage terminal for contol circuit.	
8	V_{MB}	Supply voltage terminal for Motor Drive.	
9	$\varphi\overline{B}$	Output $\overline{B}$	
10	PG−B	Power GND	
11	NFB	B−ch current detection terminal.	
12	φB	Output B	
13	$\varphi\overline{A}$	Output $\overline{A}$	
14	NFA	A−ch current detection terminal.	
15	PG−A	Power GND	
16	φA	Output A.	
17	V_{MA}	Supply voltage terminal for Motor Drive.	
18	NC	No connection.	
19	S−GND	Signal GND.	
20	$\overline{RESET}$	Reset signal input terminal.	TRUTH TABLE A
21	$\overline{ENABLE}$	Enable signal input terminal.	
22	OSC	Sawtooth oscilation terminal.	
23	CW / CCW	Forward rotation / Reverse rotation input terminal.	TRUTH TABLE A
24	CK2	Clock signal input terminal.	

PIN CONNECTION (Top view)



Note: NC : No connection

TRUTH TABLE A

INPUT					MODE
CK1	CK2	CW / CCW	$\overline{\text{RESET}}$	$\overline{\text{ENABLE}}$	
↑	H	L	H	L	CW
⎍	L	L	H	L	INHIBIT (Note)
H	↑	L	H	L	CCW
L	⎍	L	H	L	INHIBIT (Note)
↑	H	H	H	L	CCW
⎍	L	H	H	L	INHIBIT (Note)
H	↑	H	H	L	CW
L	⎍	H	H	L	INHIBIT (Note)
X	X	X	L	L	INITIAL
X	X	X	X	H	Z

Z : High impedance
X : Don't care
Note: Please don't use INHIBIT mode.

TRUTH TABLE B

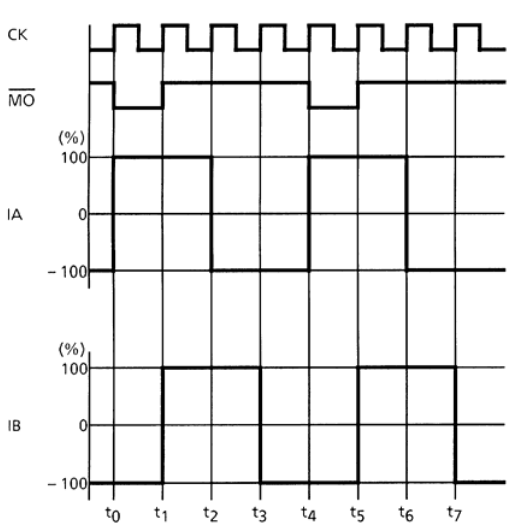
INPUT		MODE (EXCITATION)
M1	M2	
L	L	2 Phase
H	L	1−2 Phase
L	H	W1−2 Phase
H	H	2W1−2 Phase

INITIAL MODE

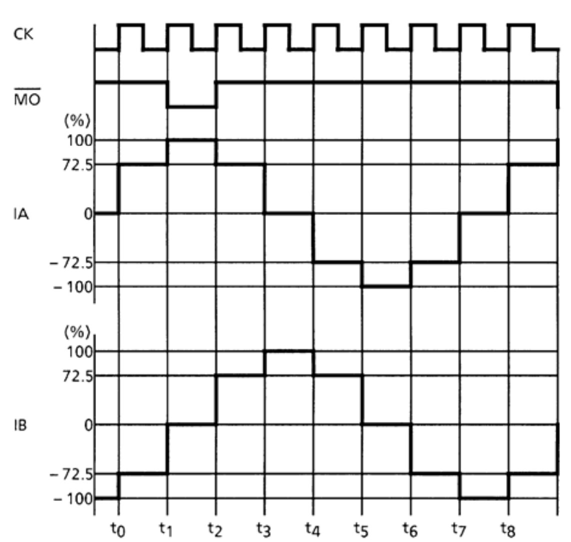
MODE	I_{OUT} (A)	I_{OUT} (B)
2 Phase	100%	−100%
1−2 Phase	100%	0%
W1−2 Phase	100%	0%
2W1−2 Phase	100%	0%

EXCITATION

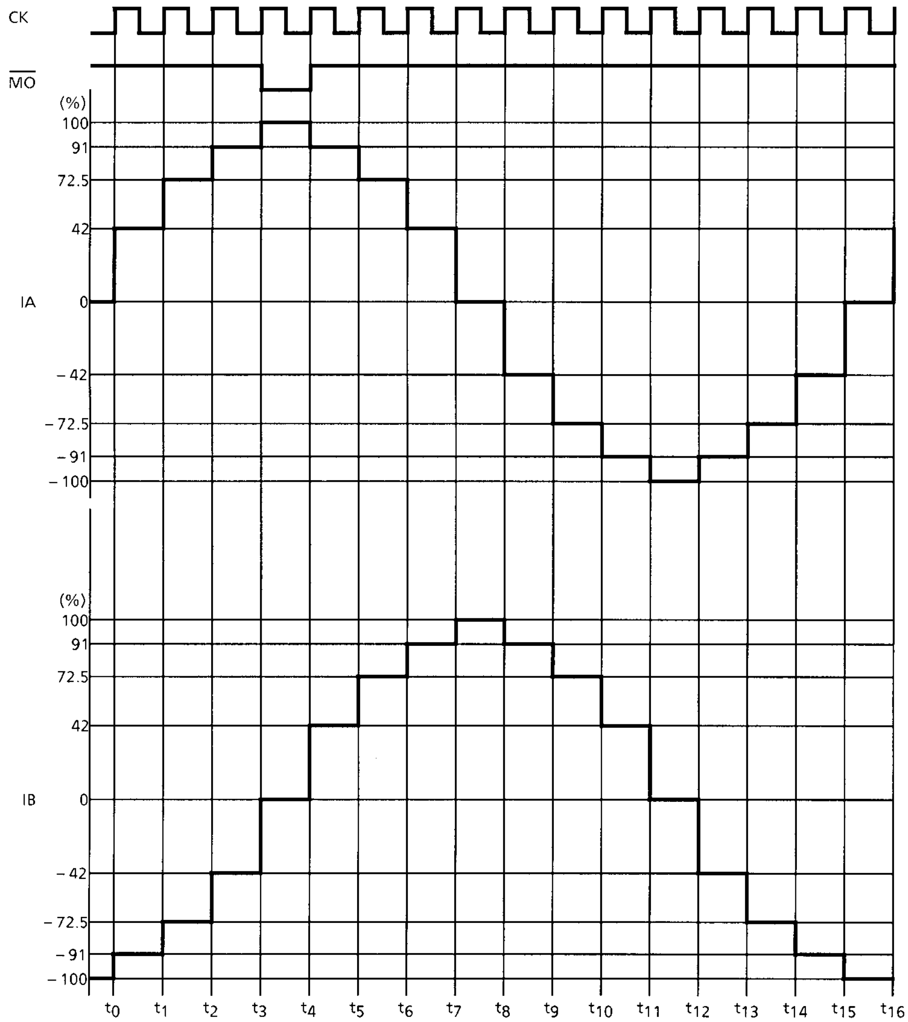
2 Phase excitation (M1 : L, M2 : L, CW MODE)



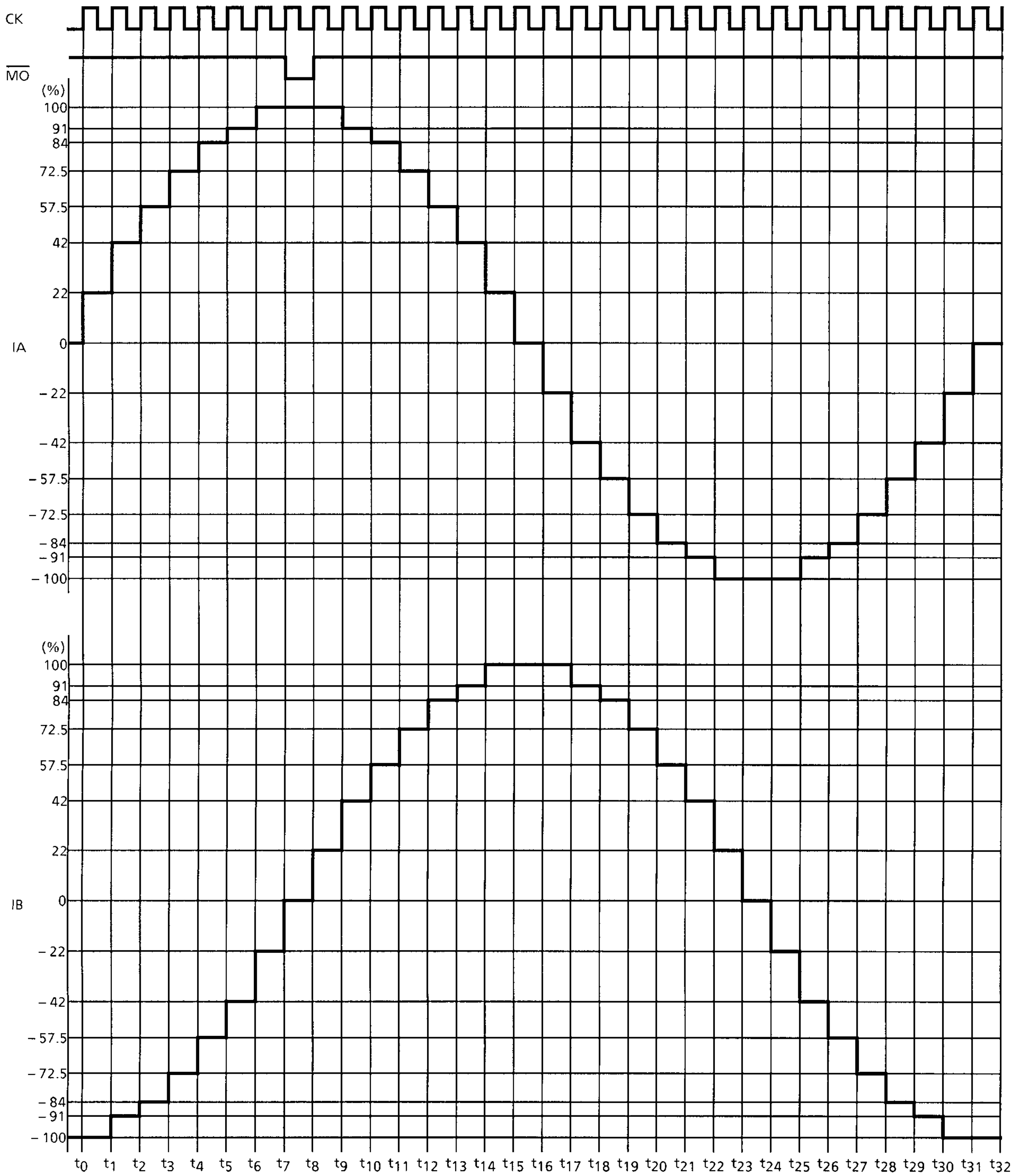
1−2 Phase excitation (M1 : H, M2 : L, CW MODE)



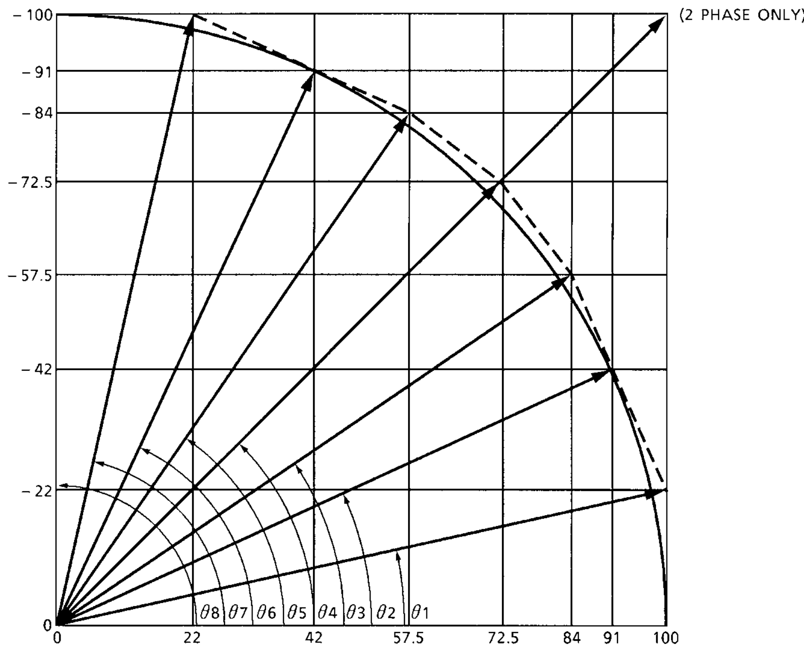
W1−2 Phase excitation (M1 : L, M2 : H, CW MODE)



2W1−2 Phase excitation (M1 : H, M2 : H, CW MODE)

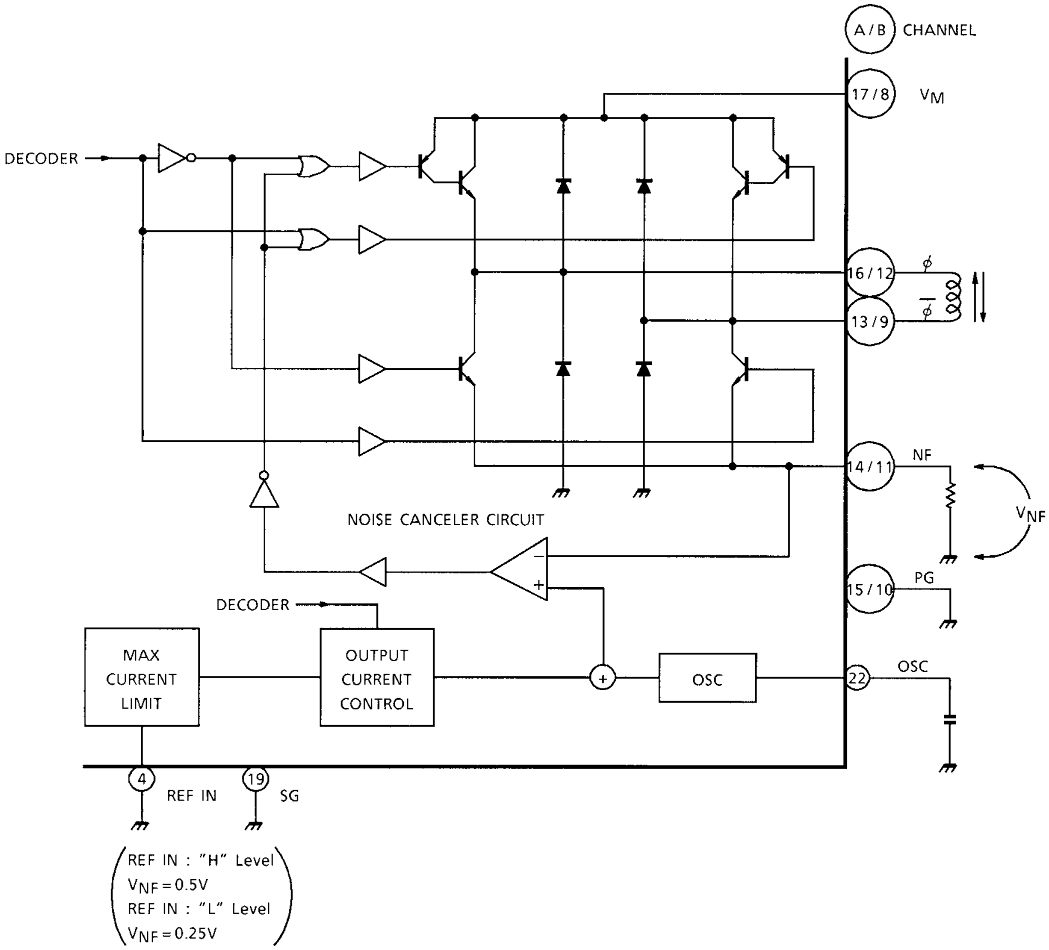


OUTPUT CURRENT VECTOR ORBIT (Normalize to 90° for each one step)



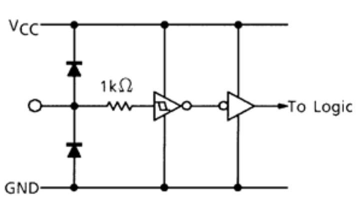
θ	ROTATION ANGLE		VECTOR LENGTH		
	IDEAL	TB6504F/FG	IDEAL	TB6504F/FG	
θ0	0°	0°	100	100.00	—
θ1	11.25°	12.41°	100	102.39	—
θ2	22.5°	27.78°	100	100.22	—
θ3	33.75°	34.39°	100	101.80	—
θ4	45°	45°	100	102.53	141.42
θ5	56.25°	55.61°	100	101.81	—
θ6	67.5°	65.22°	100	100.22	—
θ7	78.75°	77.59°	100	102.39	—
θ8	90°	90°	100	100.00	—
			1−2, W1−2, 2W1−2, Phase		2 Phase

OUTPUT CIRCUIT

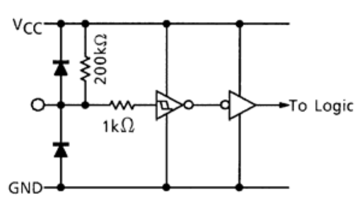


INPUT CIRCUIT

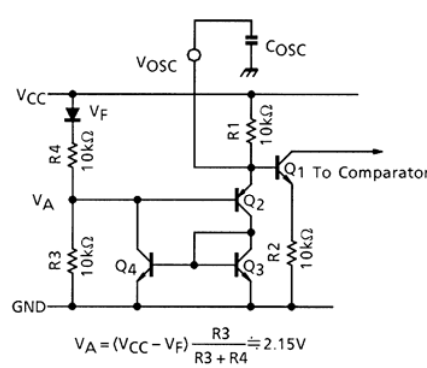
CK1, CK2, CW / CCW, M1, M2, REF IN : Terminals



$\overline{\text{RESET}}$, $\overline{\text{ENABLE}}$: Terminal



OSC : Terminal



OSC FREQUENCY CALCULATION

Sawtooth OSC circuit consists of Q_1 through Q_4 and R1 through R4.
Q_2 is turned "off" when V_{OSC} is less than the voltage of 2.5 V + V_{BE} Q_2 approximately equal to 2.85 V.
V_{OSC} is increased by C_{OSC} charging through R1.
Q_3 and Q_4 are turned "on" when V_{OSC} becomes 2.85 V (Higher level.)
Lower level of V (22) pin is equal to V_{BE} Q_2 + V_{SAT} Q_4 approximately equal to 1.4 V.
V_{OSC} is calculated by following equation.

$$V_{OSC} = 5 \times [1 - \exp(-\frac{t}{C_{OSC} \times R1})] \quad \cdots\cdots (1)$$

Assuming that V_{OSC} = 1.4 V (t = t_1) and = 2.85 V (t = t_2)
C_{OSC} is external capacitance connected to pin (22) and R1 is on−chip 10 kΩ resistor.
Therefore, OSC frequency is calculated as follows.

$$t_1 = -C_{OSC} \times R1 \times \ell n\ (1 - \frac{1.4}{5}) \quad \cdots\cdots (2)$$

$$t_2 = -C_{OSC} \times R1 \times \ell n\ (1 - \frac{2.85}{5}) \quad \cdots\cdots (3)$$

$$f_{OSC} = \frac{1}{t_2 - t_1} = \frac{1}{C_{OSC}\,(R1 \times \ell n (1 - \frac{1.4}{5}) - R1 \times \ell n (1 - \frac{2.85}{5}))}$$

$$= \frac{1}{5.15 \times C_{OSC}} \ (\text{kHz}) \ (C_{OSC}: \mu F)$$

$\overline{\text{ENABLE}}$ AND $\overline{\text{RESET}}$ FUNCTION AND $\overline{\text{MO}}$ SIGNAL

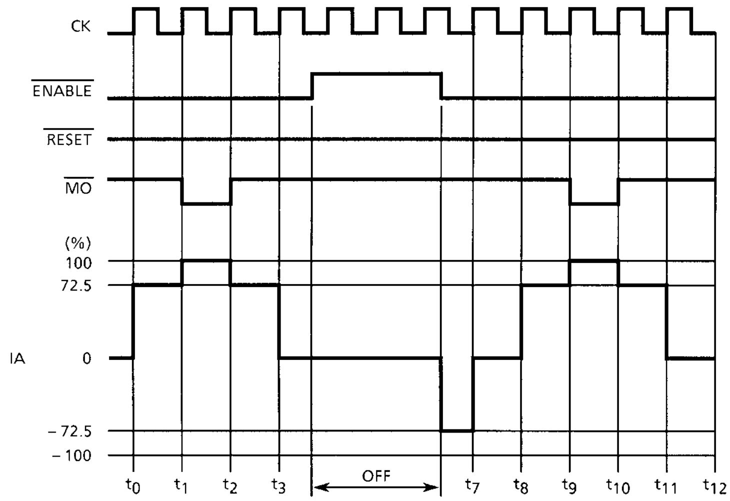


Fig.1 1−2 Phase drive mode (M1 : H, M2 : L)

$\overline{\text{ENABLE}}$ Signal disables only Output Signal.
Internal logic functions are proceeded by CK signal without regard to $\overline{\text{ENABLE}}$ signal.
Therefore, Output Current is initiated from the proceeded timing point of internal logic circuit after release of disable mode.
Fig.1 shows the $\overline{\text{ENABLE}}$ functions, when the system is selected in 1−2 Phase drive mode.
As $\overline{\text{RESET}}$ is low, the decoder is initialized and $\overline{\text{MO}}$ is low.
After $\overline{\text{RESET}}$ is high, the motion is resumed from next clock as shown in Fig.2.

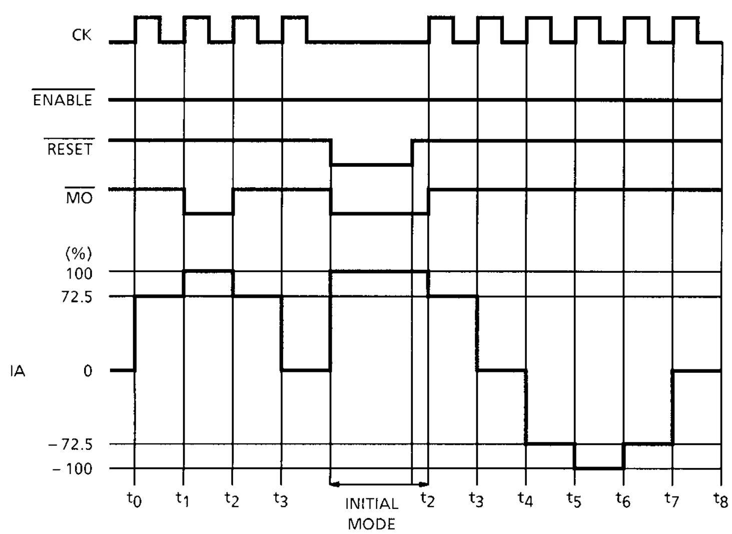


Fig.2 1−2 Phase drive mode (M1 : H, M2 : L)

$\overline{\text{MO}}$ (Monitor Output) Signals is used as rotation and initial signal for stable rotation checking.

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	5.5	V
	$V_{M\ (opr)}$	V_{CC} − 0.3~10	
	$V_{M\ (MAX)}$	18	
Output Current	$I_{O\ (MAX)}$	150	mA
	$I_{O\ (\overline{MO})}$	±2	
Input Voltage	V_{IN}	~V_{CC}	V
Power Dissipation	P_D	0.59 (Note 1)	W
		0.83 (Note 2)	
Operating Temperature	T_{opr}	−10~70	°C
Storage Temperature	T_{stg}	−55~150	°C
Feed Back Voltage	V_I	1.0	V

Note 1: No heat sink
Note 2: With heat sink (50 × 50 × 1.6 mm Cu 10%)

RECOMMENDED OPERATING CONDITIONS (Ta = −10~70°C)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Supply Voltage	$V_{CC\ (opr)}$	—	—	4.5	5.0	5.5	V
Output Voltage	$V_{M\ (opr)}$	—	—	5.5	—	8.0	V
Output Current	I_{OUT}	—	—	—	—	120	mA
Input Voltage	V_{IN}	—	—	—	—	V_{CC}	V
Clock Frequency	f_{CLOCK}	—	—	—	—	5	kHz
OSC Frequency	f_{OSC}	—	—	15	—	80	kHz

ELECTRICAL CHARACTERISTICS
(Unless otherwise specified, Ta = 25°C, V_{CC} = 5 V, V_M = 8 V)

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Input Voltage	High	$V_{IN\ (H)}$	1	M1, M2, CW / CCW, REF IN $\overline{\text{ENABLE}}$, CK1, CK2, $\overline{\text{RESET}}$	3.5	—	V_{CC} +0.4	V
	Low	$V_{IN\ (L)}$			GND −0.4	—	1.5	
Input Hysteresis Voltage		V_H			—	600	—	mV
Input Current		$I_{IN-1\ (H)}$	1	M1, M2, REF IN, V_{IN} = 5.0 V	—	—	100	nA
		$I_{IN-1\ (L)}$		$\overline{\text{ENABLE}}$, V_{IN} = 0 V, $\overline{\text{RESET}}$ INTERNAL PULL−UP RESISTOR	5	25	50	μA
		$I_{IN-2\ (L)}$		SOURCE TYPE, V_{IN} = 0 V	—	—	100	nA
Quiescent Current V_{CC} Terminal		I_{CC1}	2	Output Open $\overline{\text{RESET}}$: H $\overline{\text{ENABLE}}$: L (2, 1−2 Phase excitation)	—	10	18	mA
		I_{CC2}		Output Open (W1−2, 2W1−2 Phase excitation) $\overline{\text{RESET}}$: H $\overline{\text{ENABLE}}$: L	—	10	18	
		I_{CC3}		$\overline{\text{RESET}}$: L, $\overline{\text{ENABLE}}$: H	—	5	—	
		I_{CC4}		$\overline{\text{RESET}}$: H, $\overline{\text{ENABLE}}$: H	—	5	—	
Comparator Reference Voltage	High	$V_{NF\ (H)}$	3	REF IN H R_{NF} = 5 Ω, C_{OSC} = 0.0033 μF	0.45	0.5	0.55	V
	Low	$V_{NF\ (L)}$		REF IN L R_{NF} = 2.5 Ω, C_{OSC} = 0.0033 μF	0.22	0.25	0.28	
Output Differential		ΔV_O	—	B / A, C_{OSC} = 0.0033 μF R_{NF} = 2.5 Ω, REF IN = L	−10	—	10	%
$V_{NP\ (H)}$−$V_{NF\ (L)}$		ΔV_{NF}	—	$V_{NF\ (L)}$ / $V_{NF\ (H)}$ C_{OSC} = 0.0033 μF	43	50	57	%
Maximum OSC Frequency		$f_{OSC\ (MAX.)}$	—	—	100	—	—	kHz
Minimum OSC Frequency		$f_{OSC\ (MIN.)}$	—	—	—	—	10	kHz
OSC Frequency		f_{OSC}	—	C_{OSC} = 0.0033 μF	31	44	70	kHz
Output Voltage		$V_{OH\ (MO)}$	—	I_{OH} = −40 μA	4.5	4.9	V_{CC}	V
		$V_{OL\ (MO)}$	—	I_{OL} = 40 μA	GND	0.1	0.5	

OUTPUT BLOCK

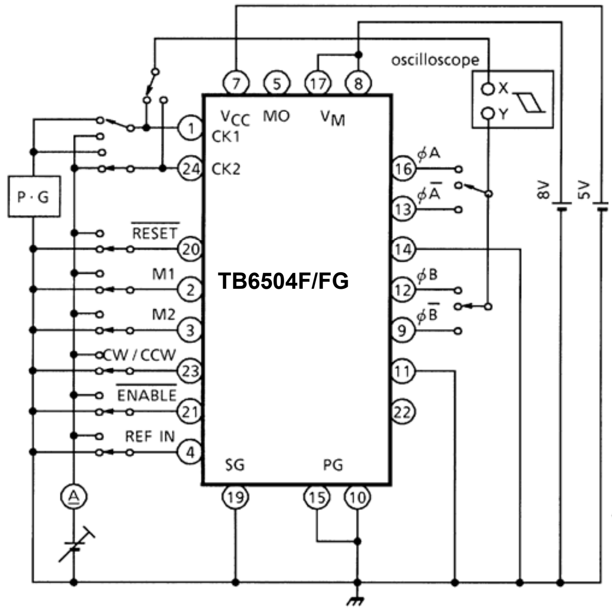
CHARACTERISTIC				SYMBOL	TEST CIRCUIT	TEST CONDITION		MIN	TYP.	MAX	UNIT
Output Saturation Voltage	Upper Side			$V_{SAT\ U1}$	4	I_{OUT} = 0.12 A		—	0.90	1.25	V
	Lower Side			$V_{SAT\ L1}$				—	0.22	0.37	
	Upper Side			$V_{SAT\ U2}$		I_{OUT} = 0.06 A		—	0.83	—	
	Lower Side			$V_{SAT\ L2}$				—	0.12	—	
Diode Forward Voltage	Upper Side			$V_{F\ U1}$	5	I_{OUT} = 0.12 A		—	1.18	1.8	V
	Lower Side			$V_{F\ L1}$				—	0.92	1.6	
Output Dark Current (A + B Channels)				I_{M1}	2	$\overline{ENABLE}$: "H" Level $\overline{RESET}$: "L" Level Output Open		—	—	50	μA
				I_{M2}		$\overline{ENABLE}$: "L" Level $\overline{RESET}$: "H" Level Output Open, 2 Phase excitation mode		—	8	28	mA
NF Terminal Current				I_{NF}		$\overline{ENABLE}$: "L" Level $\overline{RESET}$: "H" Level Output Open		1	2.5	7	
A−B Chop−ping Current (Note)	2W1−2φ	W1−2φ	1−2φ	VECTOR	3	θ = 0	REF IN : L RNF = 2.5 Ω C_{OSC} = 0.0033 μF L = 10 mH/R = 0.5 Ω	—	100	—	%
	2W1−2φ	—	—			θ = 1 / 8		—	100	—	
	2W1−2φ	W1−2φ	—			θ = 2 / 8		86	91	96	
	2W1−2φ	—	—			θ = 3 / 8		79	84	89	
	2W1−2φ	W1−2φ	1−2φ			θ = 4 / 8		67.5	72.5	77.5	
	2W1−2φ	—	—			θ = 5 / 8		52.5	57.5	62.5	
	2W1−2φ	W1−2φ	—			θ = 6 / 8		37	42	47	
	2W1−2φ	—	—			θ = 7 / 8		17	22	27	
	2 Phase Excitation Mode VECTOR			—	—	—		—	100	—	

Note: Maximum current (θ = 0) : 100%
2W1−2φ : 2W1, 2 phase excitation mode
W1−2φ : W1, 2 phase excitation mode
1−2φ : 1, 2 phase excitation mode

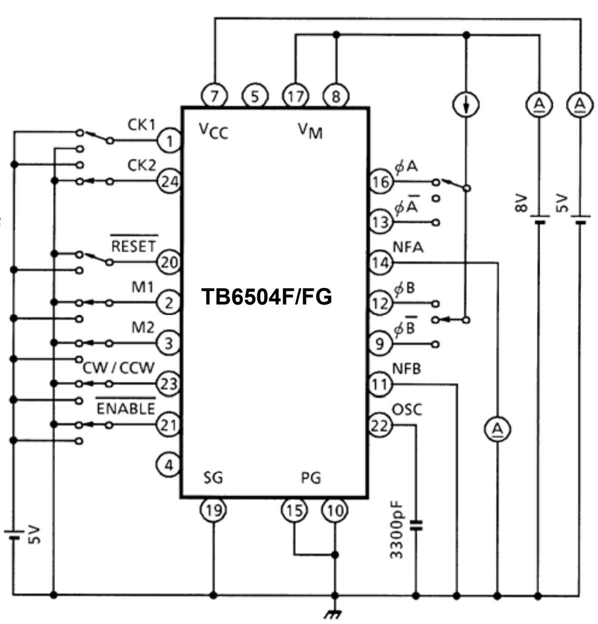
CHARACTERISTIC				SYMBOL	TEST CIRCUIT	TEST CONDITION		MIN	TYP.	MAX	UNIT
A−B Chop−ping Current (Note)	2W1−2φ	W1−2φ	1−2φ	VECTOR	3	θ = 0	REF IN : L RNF = 3.3 Ω COSC = 0.0033 μF L = 20 mH/R = 60 Ω	—	100	—	%
	2W1−2φ	—	—			θ = 1 / 8		—	100	—	
	2W1−2φ	W1−2φ	—			θ = 2 / 8		—	91.2	—	
	2W1−2φ	—	—			θ = 3 / 8		—	84.2	—	
	2W1−2φ	W1−2φ	1−2φ			θ = 4 / 8		—	73.6	—	
	2W1−2φ	—	—			θ = 5 / 8		—	59	—	
	2W1−2φ	W1−2φ	—			θ = 6 / 8		—	44.6	—	
	2W1−2φ	—	—			θ = 7 / 8		—	25.6	—	
	2 Phase Excitation Mode VECTOR					—		—	100	—	
Feed Back Voltage Step				ΔV_{NF}	—	Δθ = 0 / 8−1 / 8	REF IN : L RNF = 2.5 Ω C_{OSC} = 0.0033 μF	—	0	—	mV
						Δθ = 1 / 8−2 / 8		10	22.5	35	
						Δθ = 2 / 8−3 / 8		5	17.5	30	
						Δθ = 3 / 8−4 / 8		16.25	28.75	41.25	
						Δθ = 4 / 8−5 / 8		25	37.5	50	
						Δθ = 5 / 8−6 / 8		26.25	38.75	51.25	
						Δθ = 6 / 8−7 / 8		37.5	50	62.5	
Output Tr Switching Characteristics				t_r	7	R_L = 2 Ω, V_{NF} = 0 V, C_L = 15 pF		—	0.3	—	μs
				t_f				—	2.2	—	
				t_{pLH}		CK ~ Output		—	1.5	—	
				t_{pHL}				—	2.7	—	
				t_{pLH}		OSC ~ Output		—	5.4	—	
				t_{pHL}				—	6.3	—	
				t_{pLH}		$\overline{\text{RESET}}$ ~ Output		—	2.0	—	
				t_{pHL}				—	2.5	—	
				t_{pLH}		$\overline{\text{ENABLE}}$ ~ Output		—	5.0	—	
				t_{pHL}				—	6.0	—	
Output Leakage Current	Upper Side			I_{OH}	6	V_M = 18 V		—	—	50	μA
	Upper Side			I_{OL}				—	—	50	

Note: Maximum current (θ = 0) : 100%
2W1−2φ : 2W1, 2 phase excitation mode
W1−2φ : W1, 2 phase excitation mode
1−2φ : 1, 2 phase excitation mode

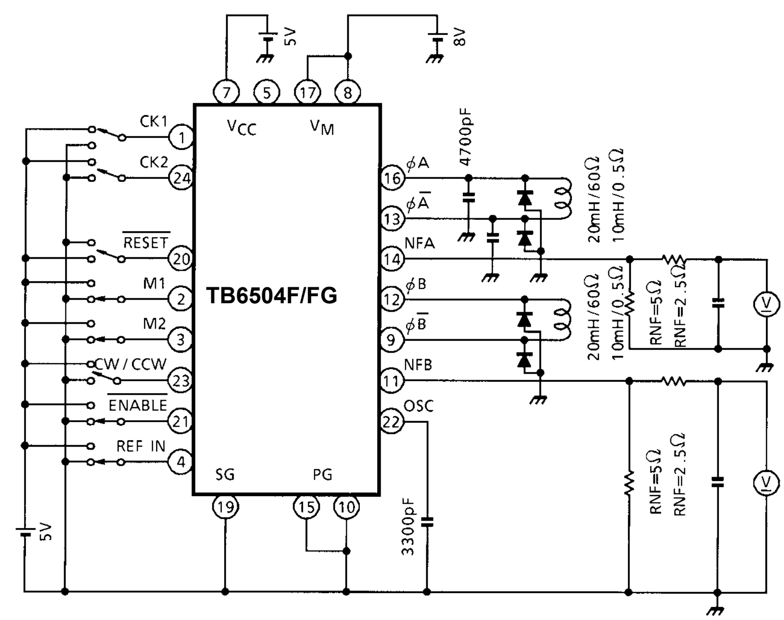
TEST CIRCUIT 1. : $V_{IN\ (H),\ (L)}$, $I_{IN\ (H),\ (L)}$



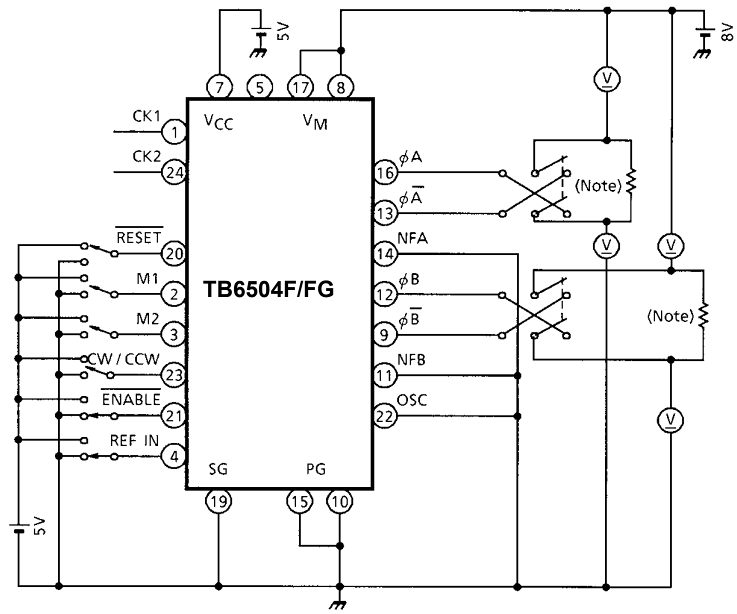
TEST CIRCUIT 2. : I_{CC}, I_M, I_{NF}



TEST CIRCUIT 3. : $V_{NF\ (H),\ (L)}$

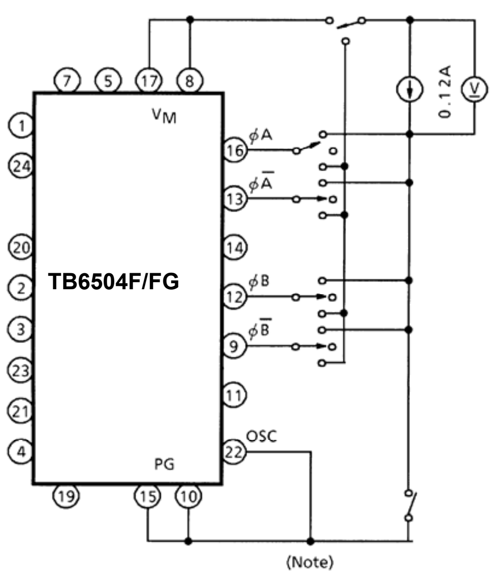


TEST CIRCUIT 4. : $V_{CE\ (SAT)}$ Upper, Lower

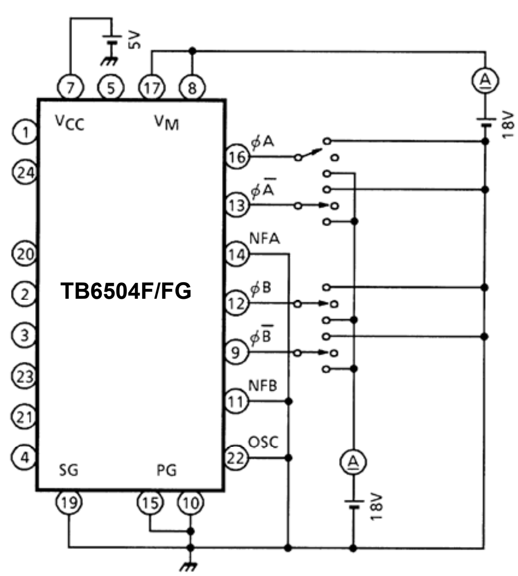


Note: Calibrate Output Current becomes 0.06 A (or 0.12 A) with this resistor.

TEST CIRCUIT 5. : V_{F-U}, V_{F-L}



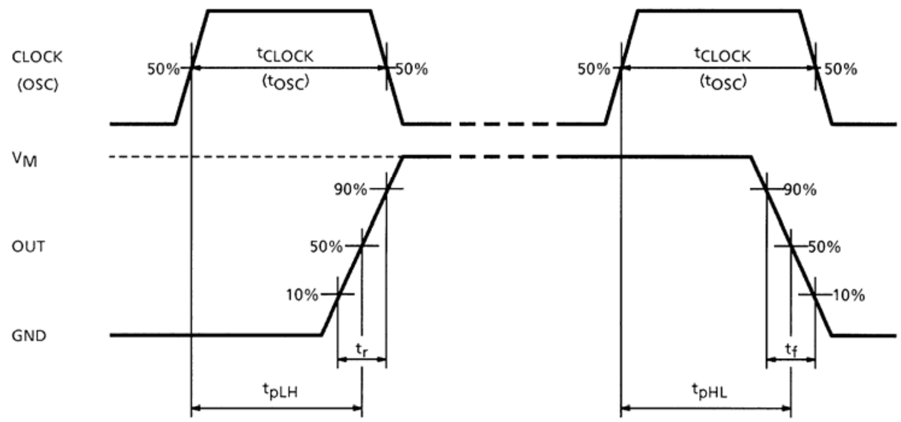
TEST CIRCUIT 6. : I_{OH}, I_{OL}

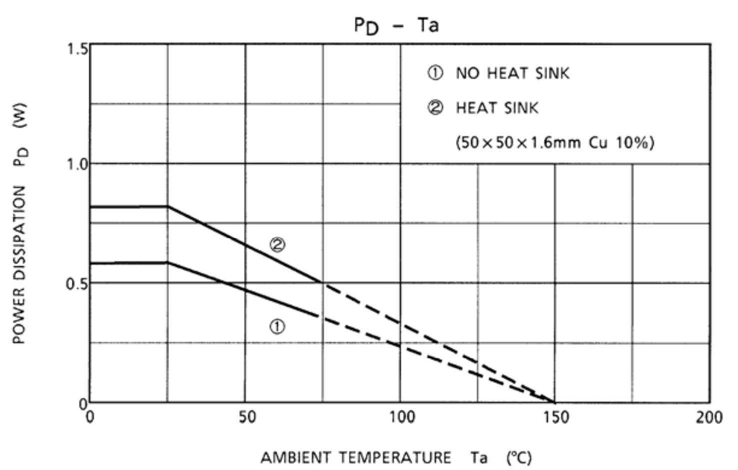


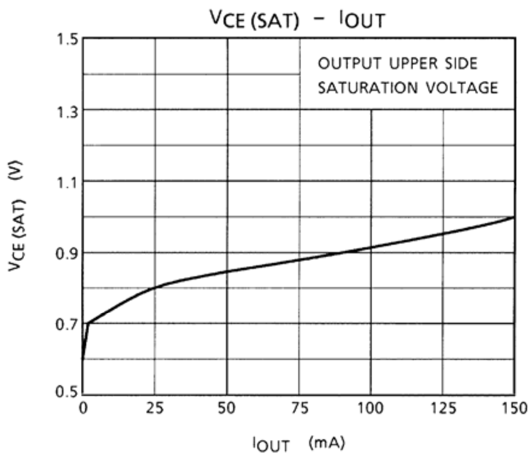
Note: Not to take a GND with any non−connecting Pins.

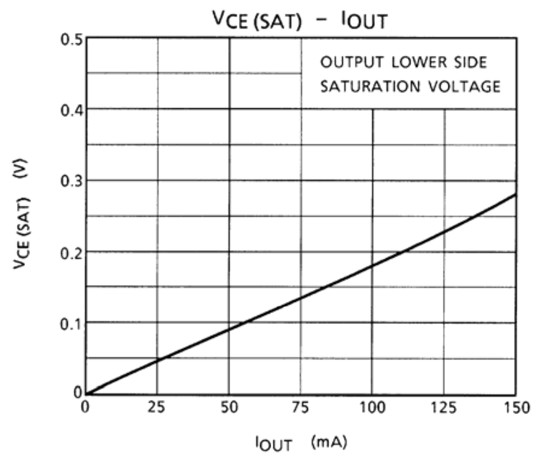
AC ELECTRICAL CHARACTERISTIC, TEST CIRCUIT

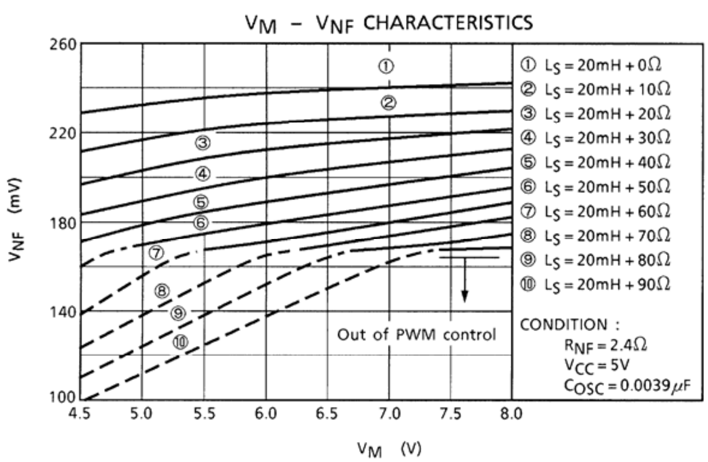
CK (OSC)−OUT



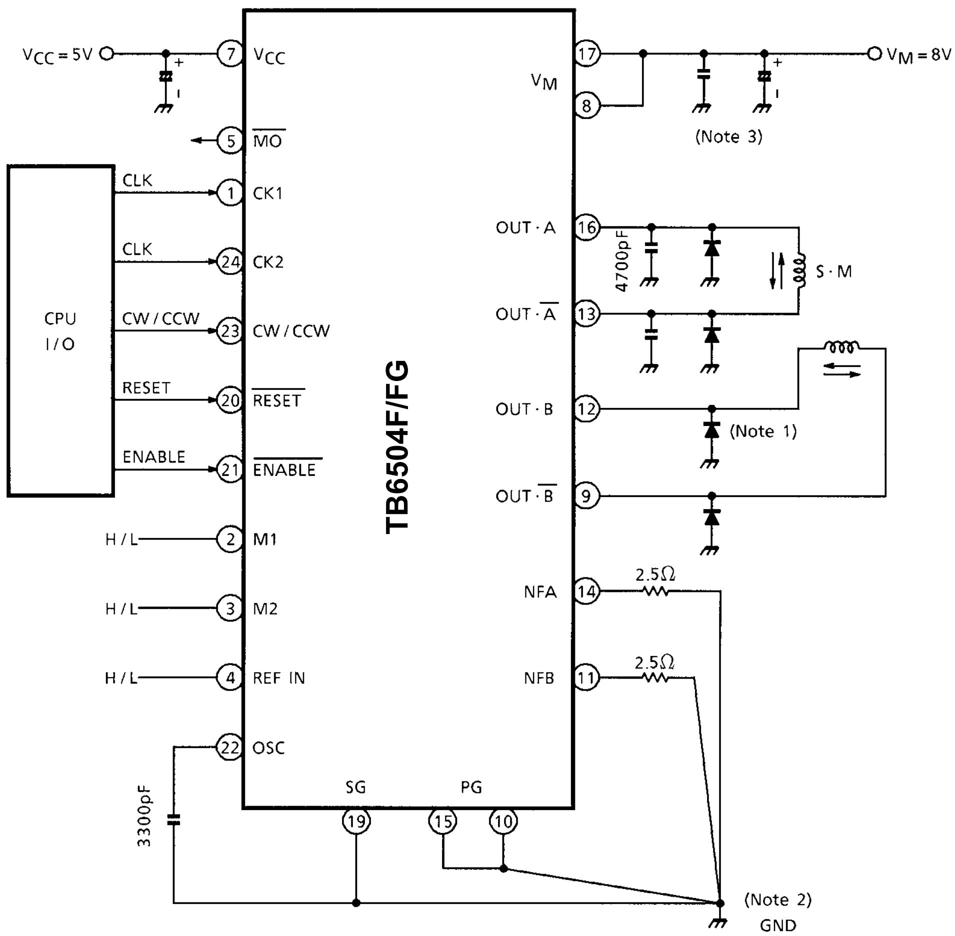



VCE (SAT) – IOUT
OUTPUT UPPER SIDE
SATURATION VOLTAGE
VCE (SAT) (V)
IOUT (mA)
1.5
1.3
1.1
0.9
0.7
0.5
0
25
50
75
100
125
150


VCE (SAT) – IOUT
OUTPUT LOWER SIDE
SATURATION VOLTAGE
VCE (SAT) (V)
IOUT (mA)
0.5
0.4
0.3
0.2
0.1
0
0
25
50
75
100
125
150


VM – VNF CHARACTERISTICS
① LS = 20mH + 0Ω
② LS = 20mH + 10Ω
③ LS = 20mH + 20Ω
④ LS = 20mH + 30Ω
⑤ LS = 20mH + 40Ω
⑥ LS = 20mH + 50Ω
⑦ LS = 20mH + 60Ω
⑧ LS = 20mH + 70Ω
⑨ LS = 20mH + 80Ω
⑩ LS = 20mH + 90Ω
CONDITION :
RNF = 2.4Ω
VCC = 5V
COSC = 0.0039μF
Out of PWM control
VNF (mV)
VM (V)
260
220
180
140
100
4.5
5.0
5.5
6.0
6.5
7.0
7.5
8.0

APPLICATION CIRCUIT



Note 1: Schottky diode (U1GWJ49) to be connected additionally between each output (pin 16 / 13 / 12 / 9) and GND for preventing Punch−through Current.

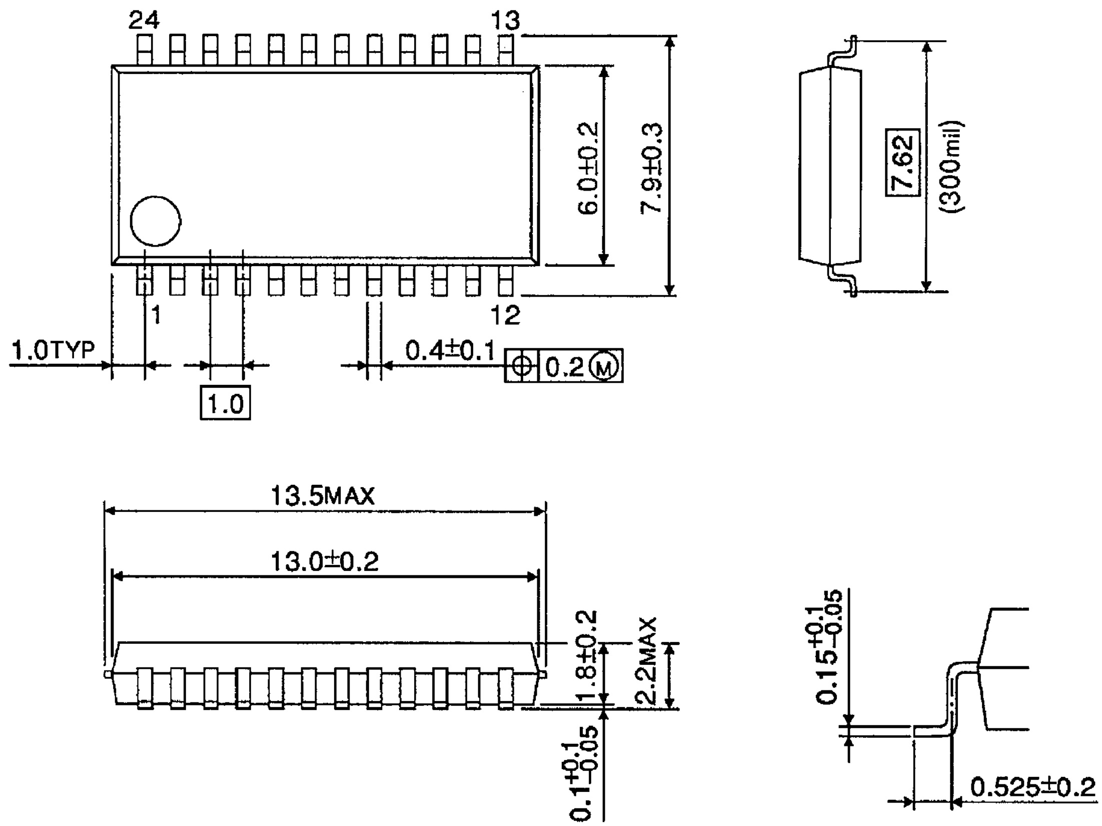
Note 2: GND pattern to be laid out at one point in order to prevent common impedance.

Note 3: Capasitor for noise suppression to be connected between the Power Supply (V_{CC}, V_M) and GND to stabilize the operation.

Note 4: Utmost care is necessary in the design of the output, V_{CC}, V_M, and GND lines since the IC may be destroyed by short-circuiting between outputs, air contamination faults, or faults due to improper grounding, or by short-circuiting between contiguous pins.

PACKAGE DIMENSIONS

SSOP24−P−300−1.00 Unit : mm



Weight : 0.32 g (Typ.)

Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.
Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on handling of ICs

[1] The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

[2] Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

[3] If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

[4] Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

Points to remember on handling of ICs

(1) Heat Radiation Design

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_J) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(2) Back-EMF

When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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