

TOSHIBA BI-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

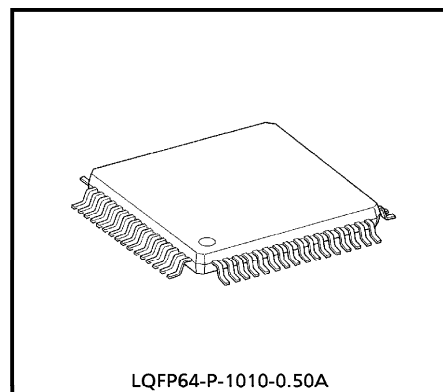
T B 6 5 1 3 A F

VIDEO CAMERA CYLINDER MOTOR CONTROLLERS AND CAPSTAN MOTOR CONTROLLERS

The TB6513AF is a single-chip IC for video camera cylinder motor controllers and capstan motor controllers. The cylinder section is a soft-switching pre-driver based on 3 phase full-wave sensorless drive and 180°-trapezoidal wave drive control. The capstan section is a soft-switching predriver based on 3 phase full-wave drive and pseudo-sine wave drive control.

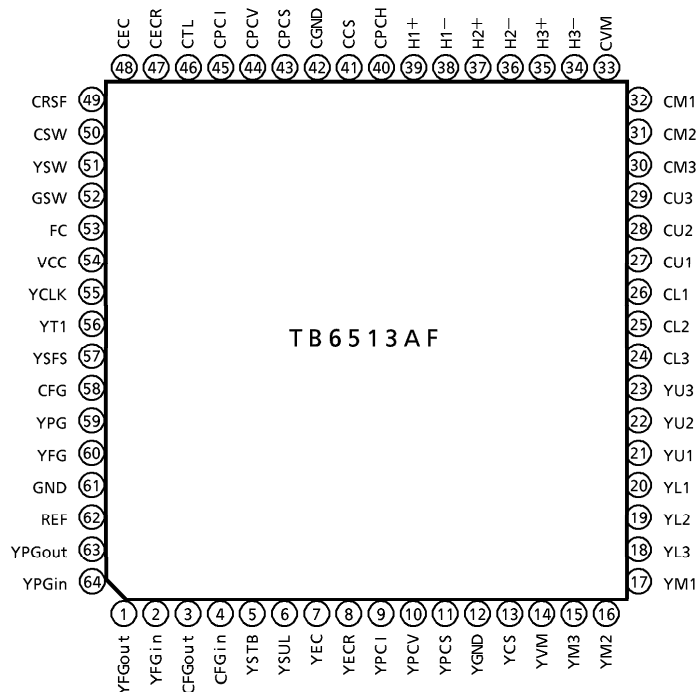
FEATURES

- Output Current : 10mA (MIN.) (at $V_{CC} = 3.5V$)
- Operating Voltage : $V_{CC} = 3.0V \sim 5.5V$
- Output Voltage : $V_M = 3.0 \sim 12V$



Weight : 0.34g (Typ.)

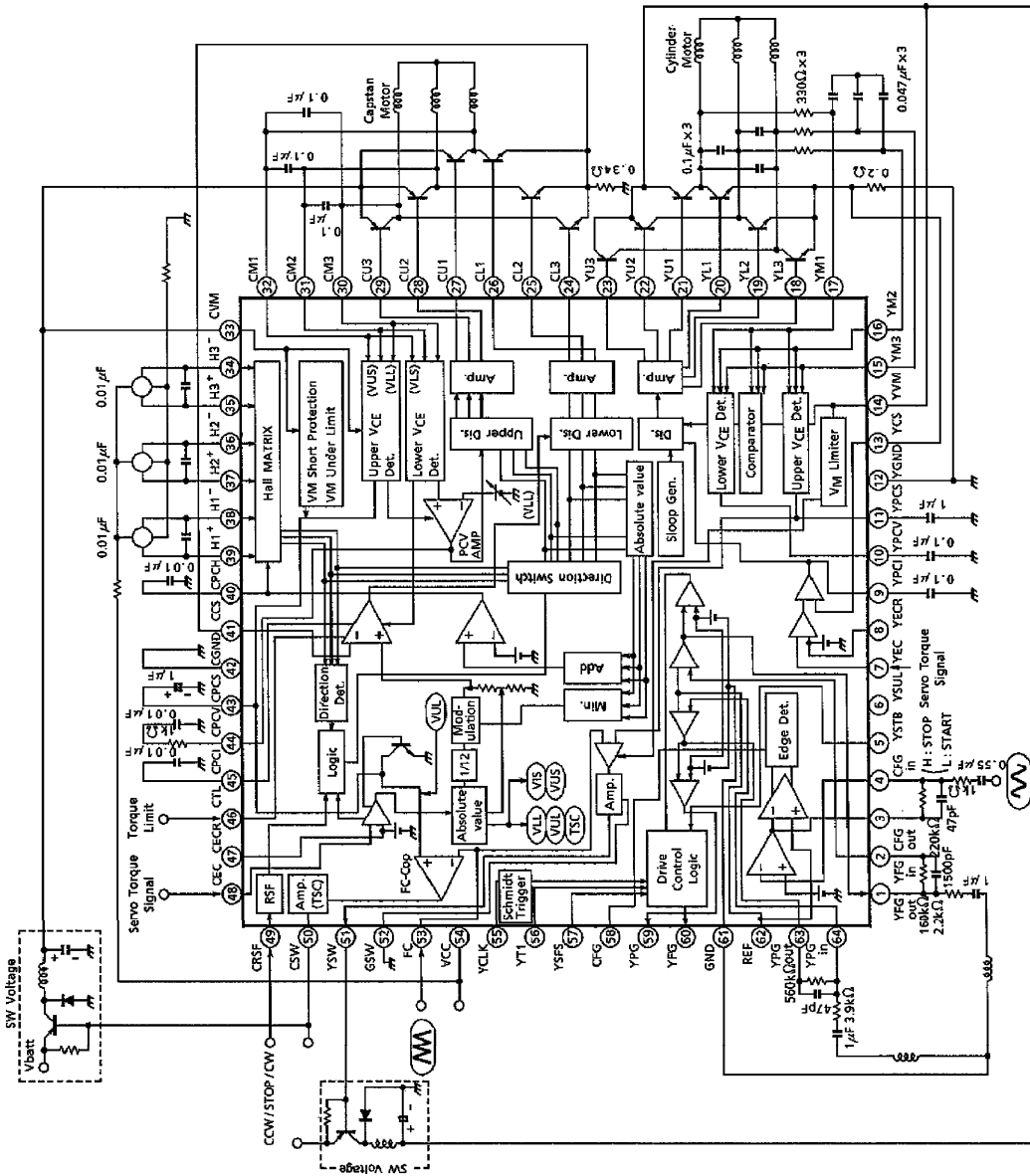
PIN CONNECTION



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BLOCK DIAGRAM



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- The information contained herein is subject to change without notice.

PIN FUNCTION

PIN No.	SYMBOL	FUNCTIONAL DESCRIPTION	PIN No.	SYMBOL	FUNCTIONAL DESCRIPTION
1	YFGout	Cylinder part FG Amp. output terminal	34	H3-	Capstan Motor Hall element Input terminal
2	YFGin	Cylinder part FG Input terminal	35	H3+	∕
3	CFGout	Capstan part FG Amp. output terminal	36	H2-	∕
4	CFGin	Capstan part FG Input terminal	37	H2+	∕
5	YSTB	Cylinder part Stand-by Switch Input terminal	38	H1-	Capstan Motor Hall element Input terminal
6	YSUL	Cylinder part Sloop Voltage terminal	39	H1+	∕
7	YEC	Cylinder part Torque control Input terminal	40	CPOCH	Capstan part Hall Amp. phase compensation
8	YECR	Cylinder part torque control reference voltage Input terminal	41	CCS	Capstan part current detective input terminal
9	YPCI	Cylinder part current feedback phase compensation	42	CGND	Capstan part GND terminal
10	YPCV	Cylinder part voltage feedback phase compensation	43	CPCS	Capstan part switching voltage control terminal
11	YPCS	Cylinder part switching voltage control output terminal	44	CPCV	Capstan part voltage feedback phase compensation
12	YGND	Cylinder part GND terminal	45	CPCI	Capstan part current feedback phase compensation
13	YCS	Cylinder part current detective	46	CTL	Capstan part torque Limit
14	YVM	Cylinder Motor Power Voltage terminal	47	CECR	Capstan part torque control reference voltage
15	YM3	Cylinder Motor Coil terminal	48	CEC	Capstan part torque control input terminal
16	YM2	∕	49	CRSF	Capstan part direction control input terminal
17	YM1	∕	50	CSW	Capstan part switching pre driver output terminal
18	YL3	Cylinder Motor Low side Pre driver output terminal	51	YSW	Cylinder part switching pre-driver output terminal
19	YL2	∕	52	GSW	Switching voltage part GND terminal
20	YL1	∕	53	FC	Switching comparator triangular-wave input terminal
21	YU1	Cylinder Motor Upper side Pre driver output terminal	54	VCC	Power voltage supply terminal for Logic
22	YU2	∕	55	YCLK	Cylinder part clock input terminal
23	YU3	∕	56	YT1	Cylinder part testmode switch input terminal
24	CL3	Capstan Motor Low side Pre driver output terminal	57	YSFS	Cylinder part start frequency selecter
25	CL2	∕	58	CFG	Capstan part FG wave output terminal
26	CL1	∕	59	YPG	Cylinder part PG wave output terminal
27	CU1	Capstan Motor Upper side Pre driver output terminal	60	YFG	Cylinder part FG wave output terminal
28	CU2	∕	61	GND	FG, PG part GND terminal
29	CU3	∕	62	REF	FG, PG part reference voltage terminal
30	CM3	Capstan Motor Coil terminal	63	YPGout	Cylinder part PG Amp. output terminal
31	CM2	∕	64	YPGin	Cylinder part PG input terminal
32	CM1	∕			
33	CVM	Capstan Motor Power voltage terminal			

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{CC}	6	V
Motor Supply Voltage (Note 1)	V _M	14	V
Supply Input/Output Voltage (Note 2)	V _{SWB}	14	V
Output Terminal Voltage (Note 3)	V _N	14	V
Input Terminal Voltage (Note 4)	V _I	-0.3 ~V _{CC} + 0.3	V
Power Dissipation	P _D	0.95 (Note 5)	W
Operating Temperature	T _{opr}	-20~75	°C
Storage Temperature	T _{stg}	-55~125	°C

(Note 1) Pin No. = 14, 33

(Note 2) Pin No. = 50, 51

(Note 3) Pin No. = 15, 16, 17, 21, 22, 23, 27, 28, 29, 30, 31, 32

(Note 4) Pin No. = 2, 4, 5, 7, 8, 13, 41, 46, 47, 48, 49, 53, 55, 56,
57, 62, 64

(Note 5) NO HEAT SHINK

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta = 25°C, V_{CC} = 3.5V)

Cylinder part

No.	CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
1	Supply Current (1)	I _{CC} (1)	1	Operational, Cylinder, Capstan part	—	17.9	30	mA
2	Supply Current (2)	I _{CC} (2)	1	STB mode STOP (CAP) mode	—	10.6	20	mA
3	ECR Voltage	V _{ECR}	1		2.14	2.24	2.54	V
4	Torque Control Input Current	I _{IEC}	1	YEC = 0V	-5	-0.5	—	μA
5	Torque Cont, Input Offset Voltage	ΔEC	2		-100	-15	100	mV
6	Input/Output Gain	Y _{Gio}	2		0.13	0.15	0.17	
7	Max Output Voltage	Y _{CSmax}	2	R _{YCS} = 0.27Ω	145	160	183	mV
8	Lower Side Output Voltage (1)	V _L (1)	3	YCS = 54mV	0.2	0.39	0.6	V
9	Lower Side Output Voltage (2)	V _L (2)	3	YECR = 2.24V, YEC = 0V	0.45	0.66	0.85	V
10	Upper Side Drive Current	I _U	4		—	—	-10	mA
11	Lower Side Drive Current	I _L	4		10	—	—	mA
12	PCS Operation Point (1)	V _{PCS} (1)	5	YEC = YECR = 2.24V V _{PCS} = 1.75V	0.36	0.47	0.58	V
13	PCS Operation Point (2)	V _{PCS} (2)	5	YEC = 0V, YECR = 2.24V V _{PCS} = 1.75V	0.60	0.79	0.98	V
14	PCS Gain	Y _{GPCS}	5		4.5	6.5	8.5	
15	SW Reg Drive Current (1)	I _{SW} (1)	5	VM1 = 6V, YEC = YECR = 2.24V	3	4.5	—	mA

Cylinder part

No.	CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
16	SW Reg Drive Current (2)	I _{SW} (2)	5	VM1 = 6V YEC = 0V, YECR = 2.24V	11	16.6	—	mA
17	SW Reg Comparator Offset Voltage	ΔV _{FC}	5		-5	15	25	mV
18	FG Amp. Gain	G _{FG}	6	V _{p-p} = 1.5mV, f = 1kHz	45	—	—	dB
19	YFG High Level	YFG (H)	7	I _{YFG} = -100μA	2.0	3.4	—	V
20	YFG Low Level	YFG (L)	7	I _{YFG} = 100μA	—	0.1	1.5	V
21	PG Amp. Gain	G _{PG}	6	V _{p-p} = 1.5mV, f = 1kHz	45	—	—	dB
22	PG Amp. Offset Voltage	ΔP _{Gin}	7		0.45	0.5	0.6	V
23	YPG High Level	YPG (H)	7	I _{YPG} = -10μA	2.0	3.0	—	V
24	YPG Low Level	YPG (L)	7	I _{YPG} = 100μA	—	0.03	1.0	V
25	Stand-by Voltage	STB _{on}	8		2.15	—	—	V
26	Stand-by Release Voltage	STB _{off}	8		—	—	1.0	V
27	Stand-by Input Current	I _{STB}	8	V _{STB} = 0V	-100	-35	—	μA
28	Starting Frequency Selector Control Voltage f = 15Hz	SFS (L)	9		—	—	1.05	V
29	Starting Frequency Selector Control Voltage f = 30Hz	SFS (H)	9		2.45	—	—	V
30	YVM Under Limit	YVML	5		1.87	2.5	3.13	V
31	YVM Short Protection	YVMS	5		0.26	0.76	1.00	V
32		I _{ML}	10	YVM = 6V	—	3	10	μA
33	Output Idel Voltage	YCS _{idle}	2	R _{YCS} = 0.27Ω	—	0	5	mV

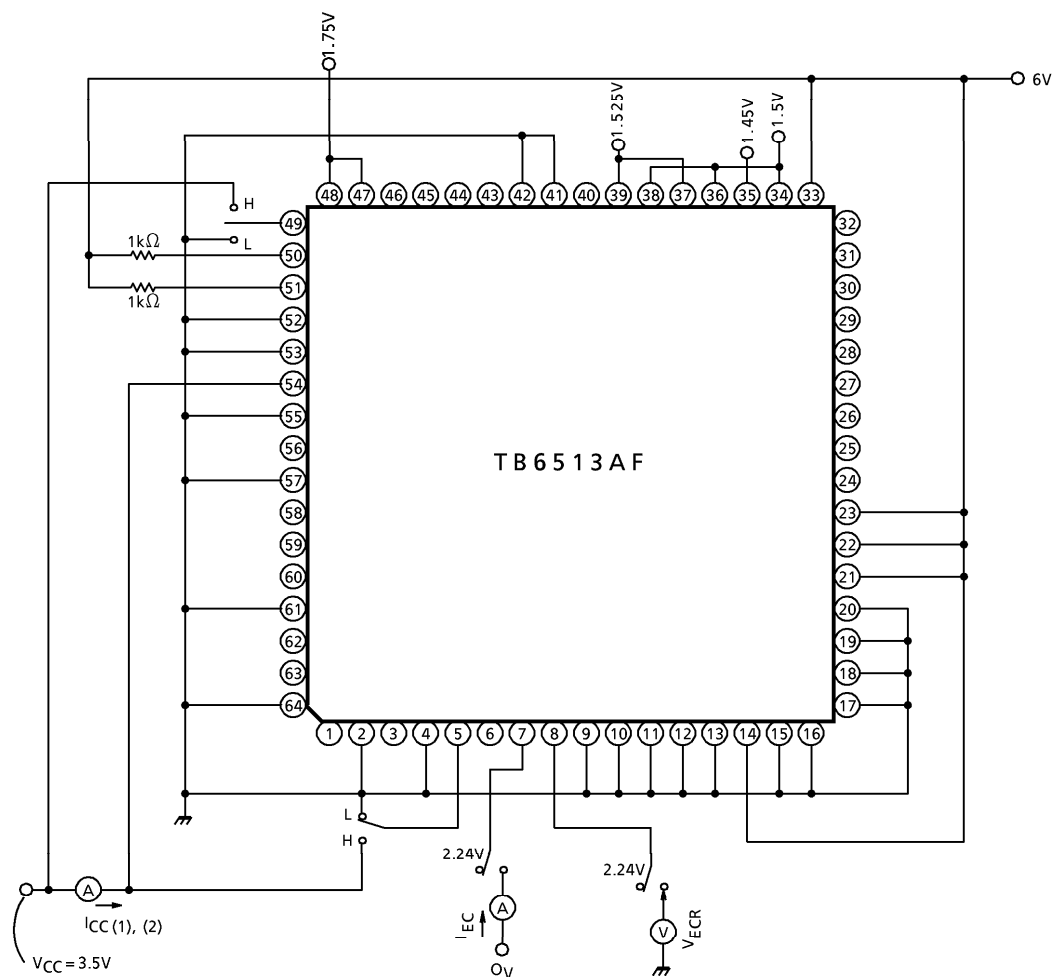
Capstan part

No.	CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
34	Torque Control Input Current	CI _{EC}	11	CEC = CECR = 1.75V	-2	-1	—	μA
35	Torque Control Reference Voltage	CE _{CR}	11		1.55	1.73	1.95	V
36	Torque Control Input Voltage	CEC	12		0.5	—	3.0	V
37	Output MAX. Voltage	CCS _{max}	12	R _{CCS} = 0.34Ω	0.19	0.23	—	V
38	Torque Control Input/ Output Gain	CG _{io}	12		0.21	0.24	0.27	
39	Output Idle Voltage	CCS _{idle}	12		—	0	4	mV
40	Torque Control Input Offset	CEC _{ofs}	12		-100	15	100	mV

Capstan part

No.	CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
41	Torque Control Dead Zone	CECdz	12		30	77	130	mV
42	Low Side V_{CE} Voltage (1)	CVLL (1)	13	CCS = 60mV	0.22	0.28	0.50	V
43	Low Side V_{CE} Voltage (2)	CVLL (2)	13	CEC = 0V, CTL = 1.0V	0.40	0.50	0.80	V
44	Hall Element Input	Hin	14		1.2	—	2.0	V
45	Hall Element Input	Hofs	15		-8	-1	8	mV
46	TL-CS Offset	TLofs	16	CTL = 20mV	6	9.5	14	mV
47	Forward Rotation Control Voltage	Vf	17		—	—	0.87	V
48	Stop Control Voltage	Vs	17		1.27	—	2.23	V
49	Reverse Rotation Control Voltage	Vr	17		2.90	—	—	V
50	Ripple Channel	R	18	CCS = 60mV	8	8.5	18	%
51	Upper Side Drive MAX. Current	CI _U	19		10	24	—	mA
52	Low Side Drive MAX. Current	CI _L	19		—	-16	-10	mA
53	SW Power Voltage Input Offset	CSWofs	21		-20	11	20	mV
54	SW Power Voltage Control Output Gain	CGPCS	20		6	8	10	
55	SW Power Voltage Control Output Voltage (1)	VUD (1)	20	CEC = CECR, CPCS = 1.7V	0.3	0.40	0.65	V
56	SW Power Voltage Control Output Voltage (2)	VUD (2)	20	CEC = 0V, CTL = 0.2V CPCS = 1.7V	0.47	0.62	1.10	V
57	SW Power Voltage Output MAX. Current	CI _{SWB}	20	CEC = 0V, CTL = 0.2V	15	22	—	mA
58	FG Amp. Reference Voltage	CFG _{ref}	11		1.7	2.0	2.3	V
59	FG Amp. Loop Gain	CGFG	22	External 1k Ω , 220k Ω Input 3mV _{p-p} , 1kHz	45	50	—	dB
60	FG Amp. Output Voltage High Level	CFG _H	22		3	3.5	—	V
61	FG Amp. Output Voltage Low Level	CFG _L	22		—	0.01	0.5	V
62	V _M Under Limit	CV _{ML}	23		1.13	1.52	1.88	V
63	V _M Short Protection	CV _{MS}	23		0.26	0.45	1.00	V

TEST CIRCUIT 1. $I_{CC}(1)$, $I_{CC}(2)$, V_{ECR} , YI_{EC}



No.1 $I_{CC}(1)$

Set $YSTB = 0V$, $YEC = 2.24V$, $YECR = 0V$ and $CRSF = 0V$, then measure the current to the V_{CC} terminal.

No.2 $I_{CC}(2)$

Set $YSTB = 3.5V$, $YEC = YECR = 2.24V$ and $CRSF = OPEN$, then measure the current to the V_{CC} terminal.

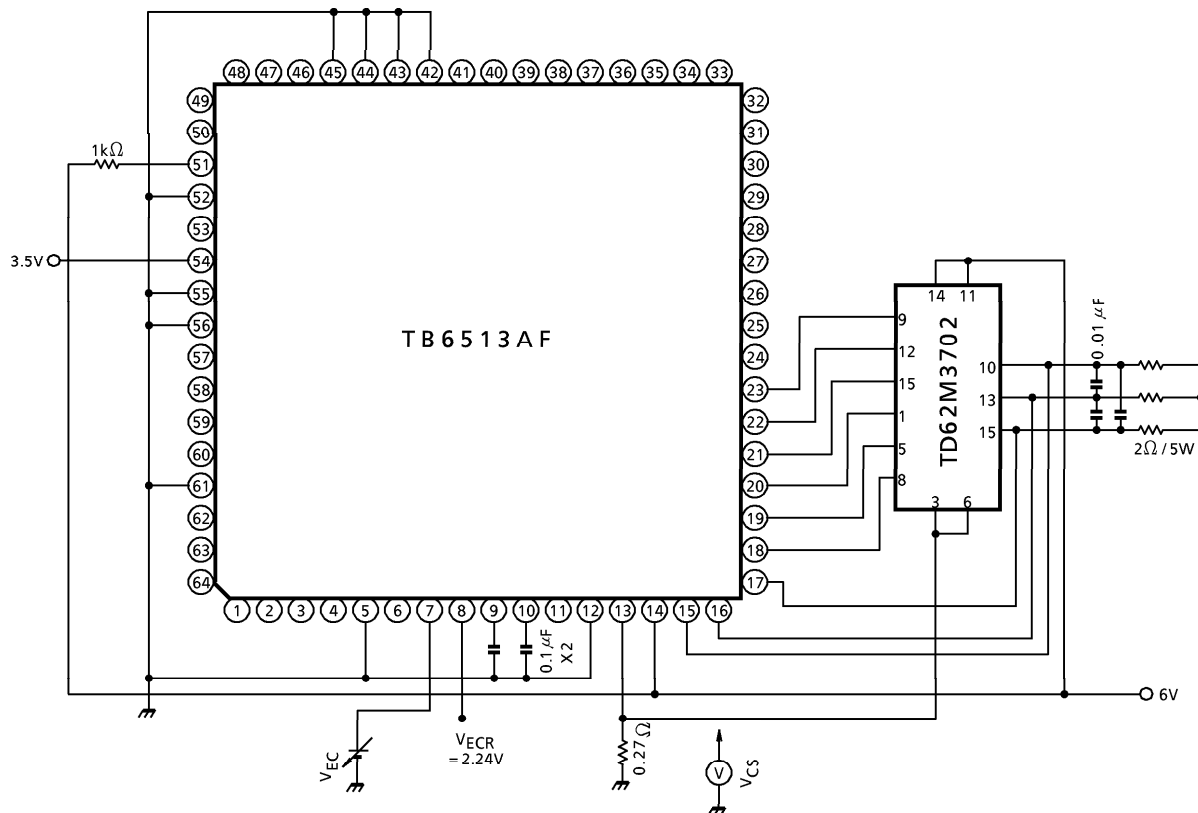
No.3 V_{ECR}

Measure the potential of pin ⑧.

No.4 YI_{EC}

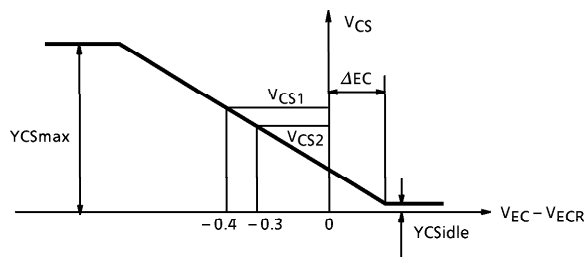
Set $YEC = 0V$ and $YECR = 2.24V$, then measure the current to pin ⑦.

TEST CIRCUIT 2. ΔEC , YG_{io}, YCS_{max}, YCS_{side}



No.5 ΔEC , No.6 YG_{io}, No.7 YCS_{max}, No.33 YCS_{side}

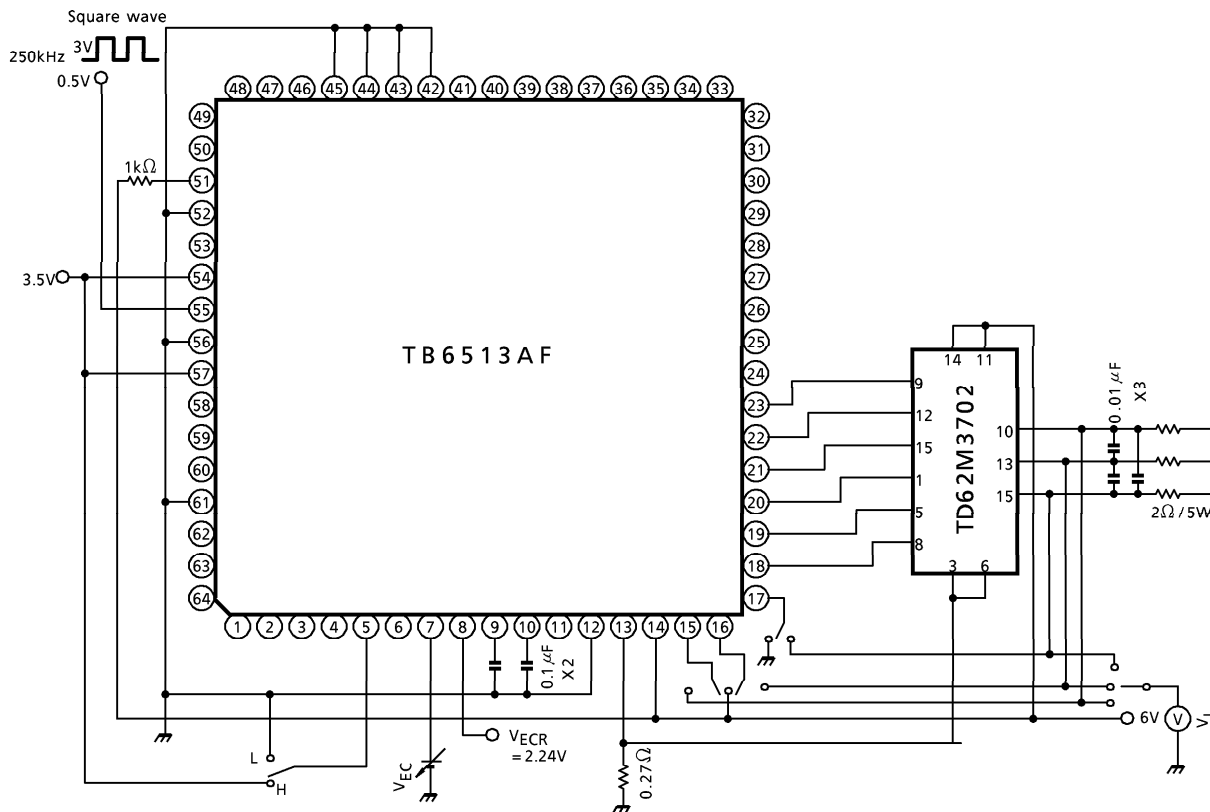
Set YECR = 2.24V, change YEC from 0V to 3V, then measure the potential of pin 13.



$$\Delta EC = V_{EC} - V_{ECR} \quad (V_{CS} \approx 0V)$$

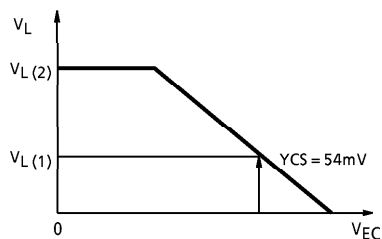
$$YG_{io} = \frac{V_{CS1} - V_{CS2}}{0.1V}$$

TEST CIRCUIT 3. $V_L(1)$, $V_L(2)$



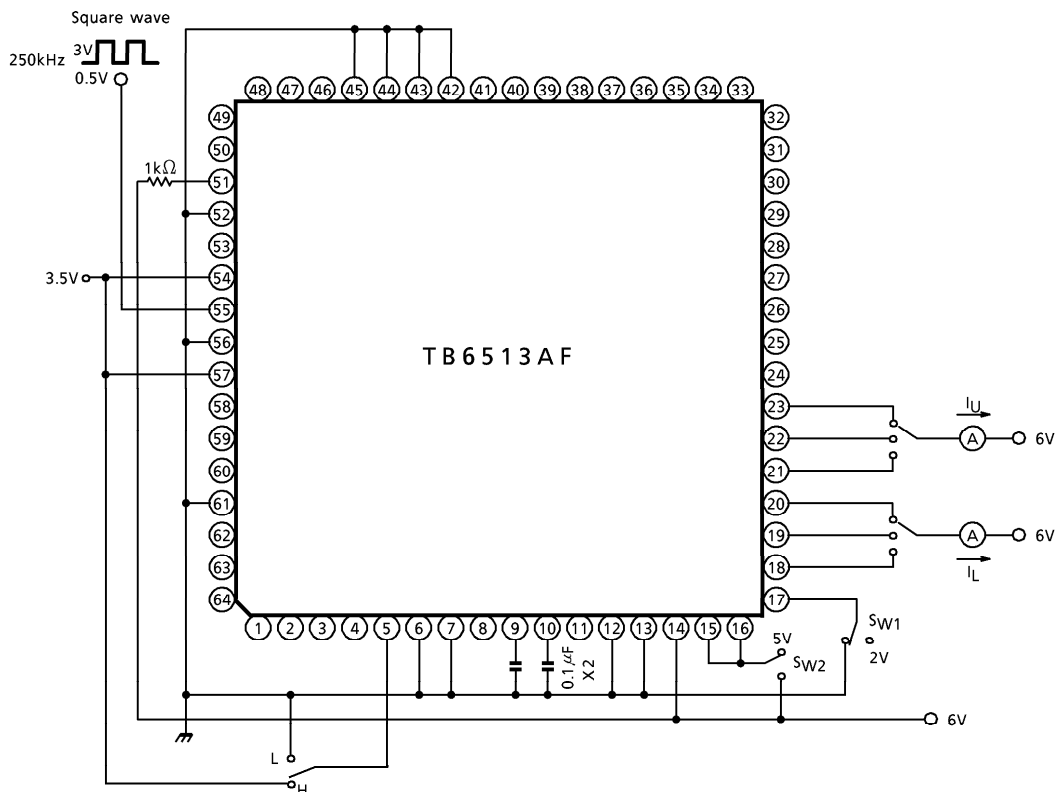
No.8 $V_L(1)$, No.9 $V_L(2)$

To set the drive angle, change the YSTB pin from high to low with $Y_{M1} = 0V$, $Y_{M2} = 6V$, and $Y_{M3} = 6V$. Then input the number of clocks indicated below to the YCLK terminal. After setting the drive angle, connect the Y_{M1} , Y_{M2} , and Y_{M3} pins to PWTR and measure voltages at these terminals.



CLOCK	80	150	270
Terminal	Y_{M3}	Y_{M1}	Y_{M2}

TEST CIRCUIT 4. I_U, I_L

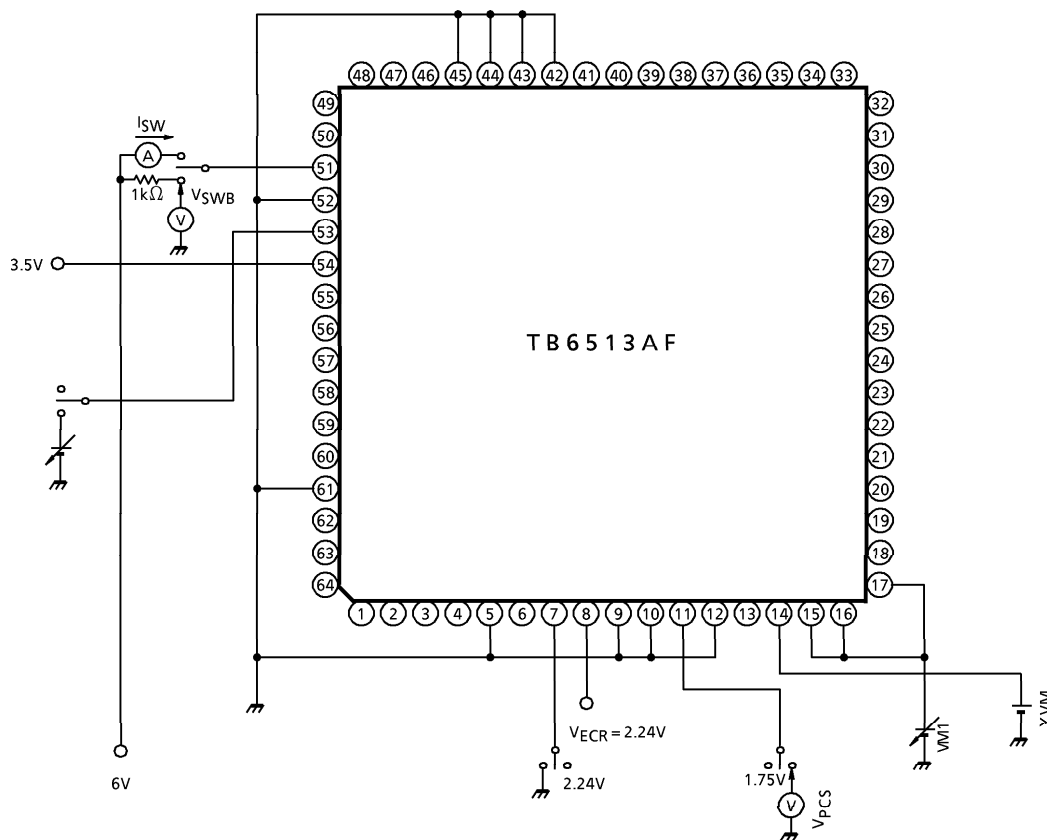


No.10 I_U , No.11 I_L

To set the drive angle, first change the YSTB terminal from high to low, then input the number of clocks indicated below to the YCLK terminal.

CLOCK	50		150		280	
Terminal	YU1	YL3	YU2	YL1	YU3	YL2
SW1	0V	2V	0V	2V	0V	2V
SW2	5V	6V	5V	6V	5V	6V

TEST CIRCUIT 5. V_{PCS} (1), V_{PCS} (2), $Y_{G_{PCS}}$, I_{SW} (1), I_{SW} (2), ΔV_{FC} , Y_{VML} , Y_{VMS}



No.12 V_{PCS} (1)

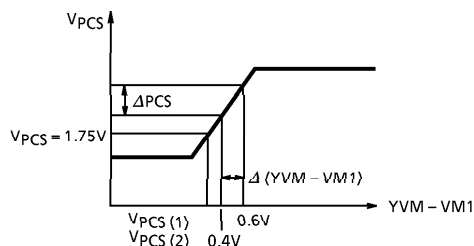
Set $Y_{VM} = 6V$ and $Y_{EC} = 2.24V$, then measure $VM1$ when $V_{PCS} = 1.75V$.

No.13 V_{PCS} (2)

Set $Y_{VM} = 6V$ and $Y_{EC} = 0V$, then measure $VM1$ when $V_{PCS} = 1.75V$.

No.14 $Y_{G_{PCS}}$

Set $Y_{VM} = 6V$ and $Y_{EC} = 2.24V$, then determine $Y_{G_{PCS}}$ from the amount that V_{PCS} voltage varies when $(Y_{VM} - VM1)$ changes from $0.4V$ to $0.6V$.



$$Y_{G_{PCS}} = \frac{\Delta PCS}{\Delta (Y_{VM} - VM1)}$$

No.15 I_{SW} (1)

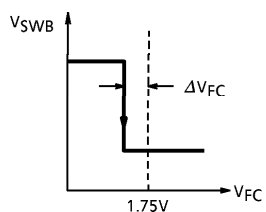
Set FC = 3V and YEC = 2.24V, then measure the current to the YSW terminal. (YVM = VM1 = 6V)

No.16 I_{SW} (2)

Set FC = 3V and YEC = 0V, then measure the current to the YSW terminal. (YVM = VM1 = 6V)

No.17 ΔV_{FC}

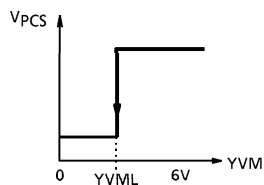
Set YPCS = 1.75V, then change FC from 0V and measure the difference between V_{FC} and V_{PCS} when V_{SWB} changes from high to low. (YVM = VM1 = 6V)



$$\Delta V_{FC} = V_{PCS} - V_{FC}$$

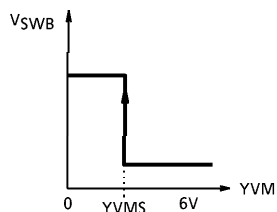
No.30 YVML

When FC = 3V, YEC = 2.24V, and VM1 = YVM - 1V, change YVM from 6V and measure YVML when V_{PCS} changes from high to low.

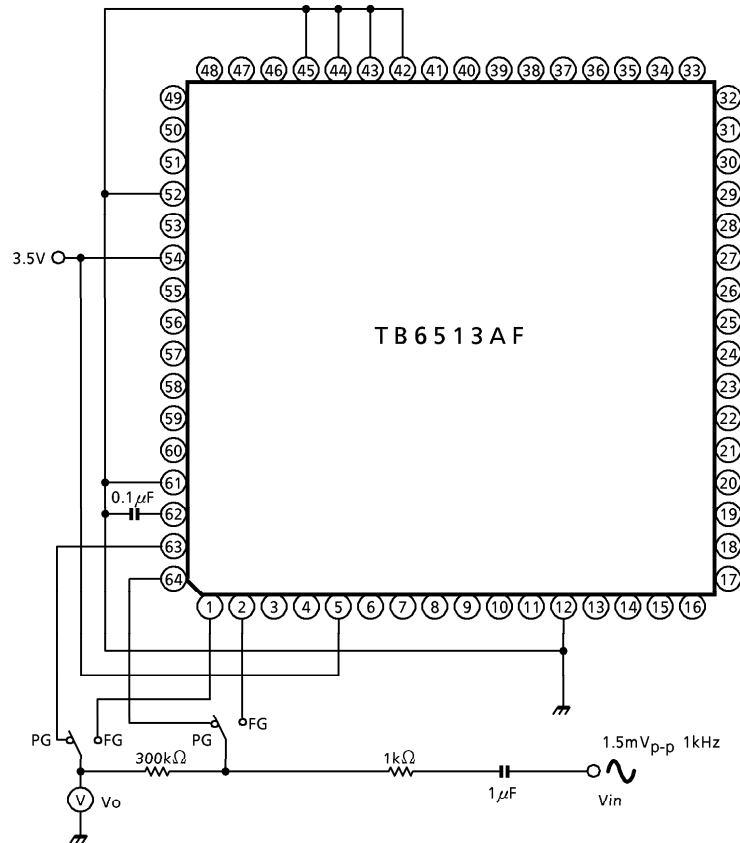


No.31 YVMS

Set FC = 3V, YEC = 0V, and VM1 = 6V, then change YVM from 6V and set YVMS when V_{SWB} changes from low to high.



TEST CIRCUIT 6. G_{FG} , G_{PG}



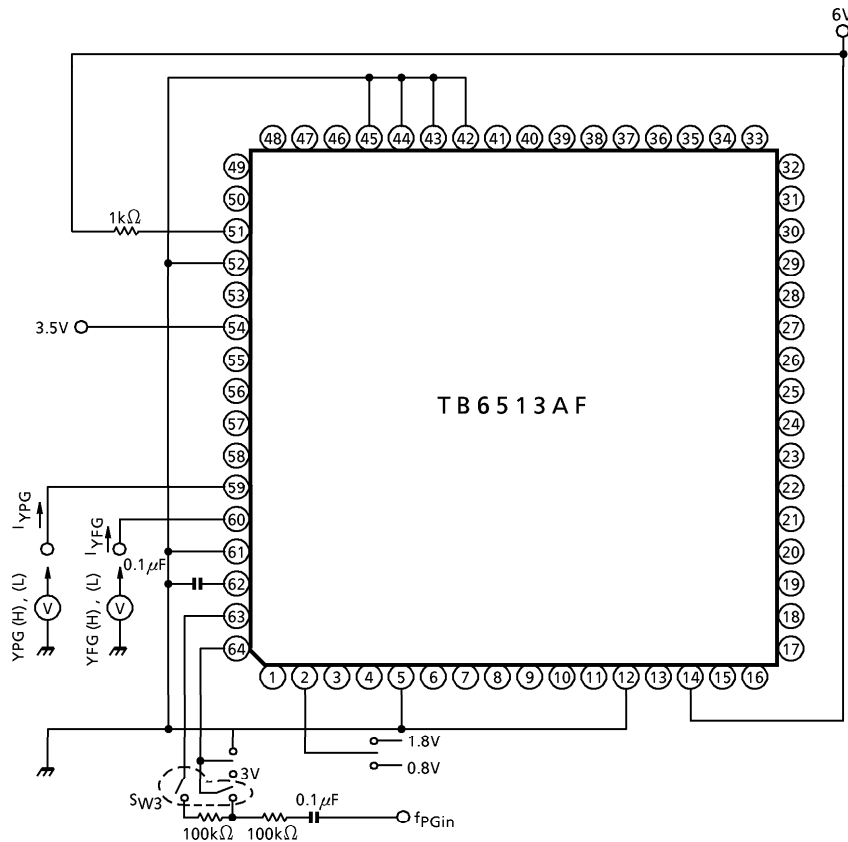
No.18 G_{FG}

Set SW to FG, then determine $G_{FG} = 20 \log (V_o / V_{in})$ by measuring V_o when $V_{in} = 1.5mV_{p-p}$, 1kHz.

No.21 G_{PG}

Set SW to PG, then determine $G_{PG} = 20 \log (V_o / V_{in})$ by measuring V_o when $V_{in} = 1.5mV_{p-p}$, 1kHz.

TEST CIRCUIT 7. YFG (H), YFG (L), ΔPGin, YPG (H), YPG (L)



No.19 YFG (H)

Apply 1.8V to YFGin and set YFG to high. Then measure the YFG potential when $-100\mu A$ is input to IYFG.

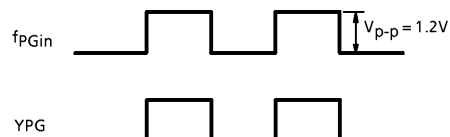
No.20 YFG (L)

Apply 0.8V to YFGin and set YFG to low. Then measure the YFG potential when $100\mu A$ is input to IYFG.

No.22 Δ PGin

Turn SW3 on and input a 10kHz square wave from fPGin. Set fPGin to 1.2V_{p-p} (Δ PGin = 0.6V) and check that pin 59 is active.

Also, set V_{p-p} to 0.9V (Δ PGin = 0.45V) and check that terminal YPG is not active.



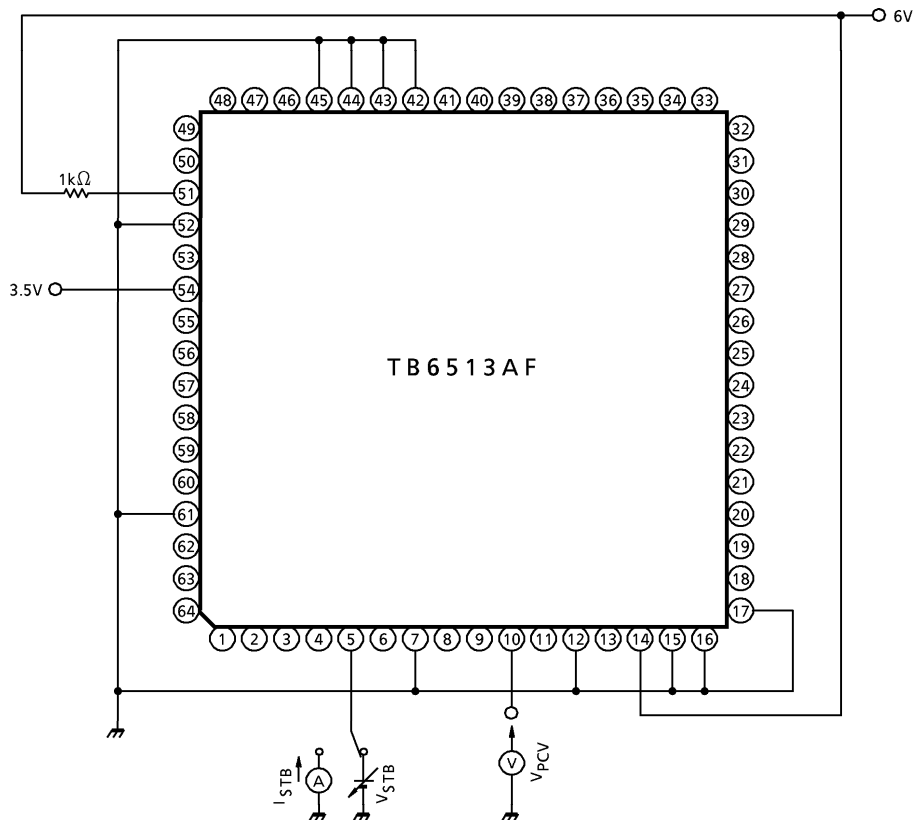
No.23 YPG (H)

Apply 3V to YPGin and set YPG to high. Then measure the YPG potential when a current of $I_{YPG} = -10\mu A$ is obtained.

No.24 YPG (L)

Apply 0V to YPGin and set YPG to low. Then measure the YPG potential when a current of $I_{YPG} = 100\mu A$ is obtained.

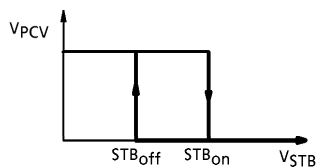
TEST CIRCUIT 8. STB_{on} , STB_{off} , I_{STB}



No.25 STB_{on} , No.26 STB_{off}

Change V_{STB} from 0V to 3.5V, and from 3.5V to 0V, and measure V_{PCV} .

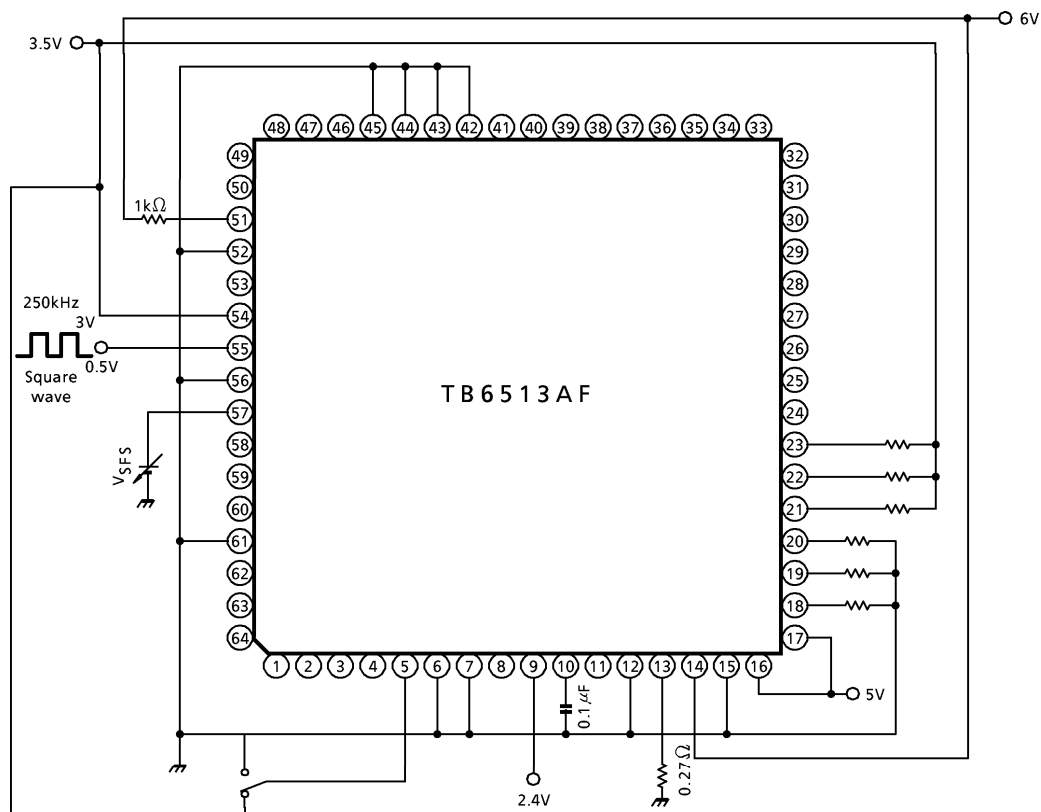
V_{STB} is STB_{on} when V_{PCV} changes from high to low. V_{STB} is STB_{off} when V_{PCV} changes from low to high.



No.27 I_{STB}

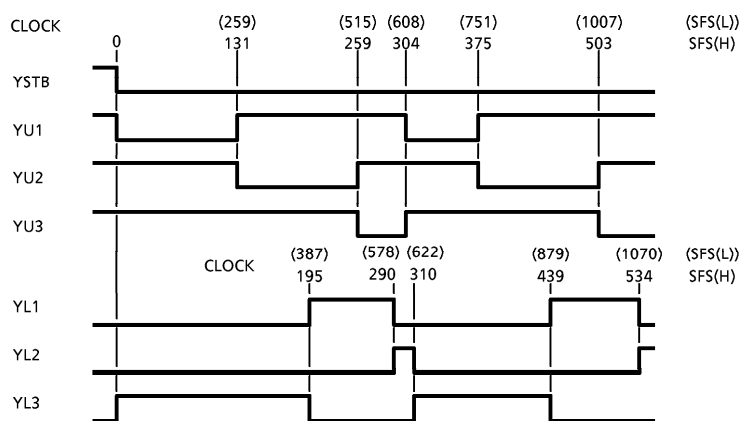
Measure I_{STB} when $V_{STB} = 0V$.

TEST CIRCUIT 9. SFS (L), SFS (H)

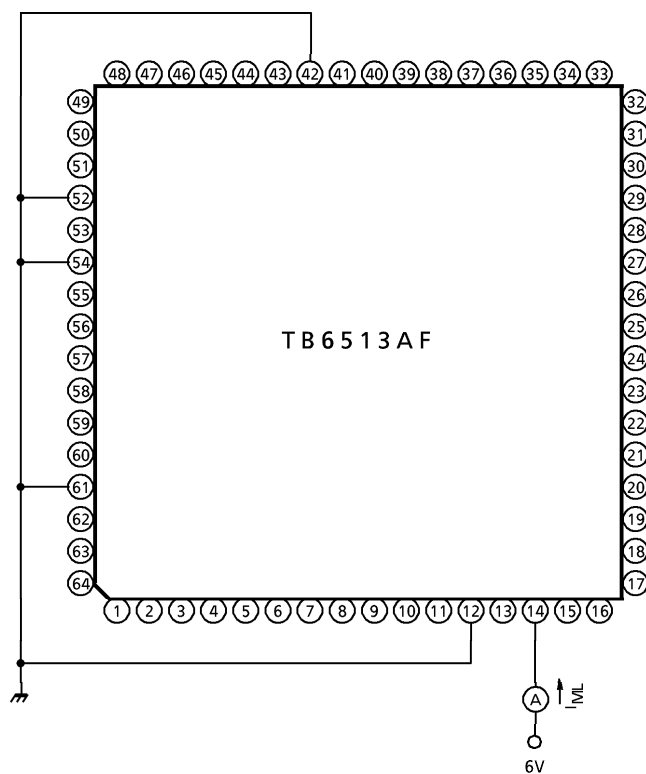


No.28 SFS (L), No.29 SFS (H)

Change V_{SFS} to 0V and to 3.5V, then measure the potential of YU1~3 and YL1~3.

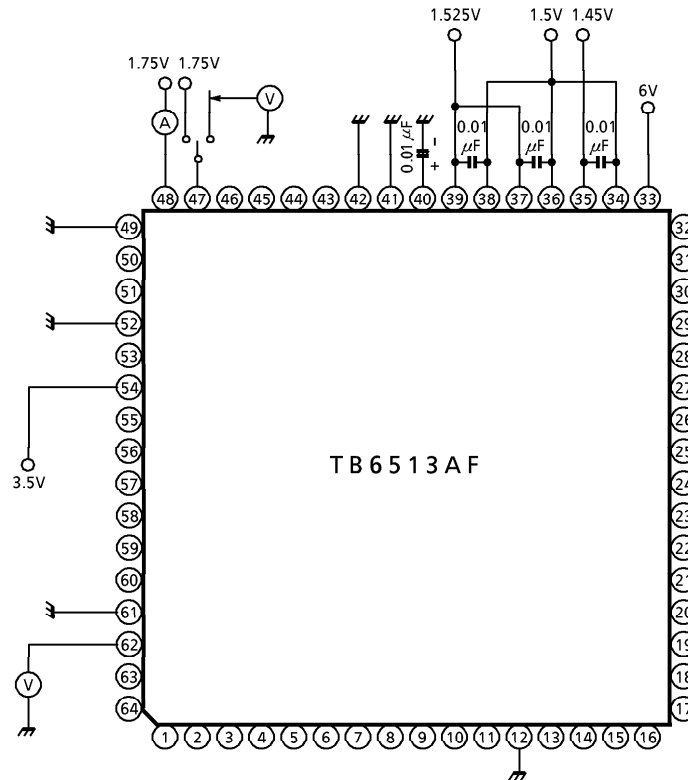


TEST CIRCUIT 10. I_{ML}



No.32 I_{ML}
 Set YVM = 6V, then measure the current to pin⑭.

TEST CIRCUIT 11. C_{IEC} , C_{ECR} , C_{Gref}



No.34 C_{IEC}

Set $C_{EC} = 1.75$ and $C_{ECR} = 1.75V$, then measure the current to the C_{EC} terminal.

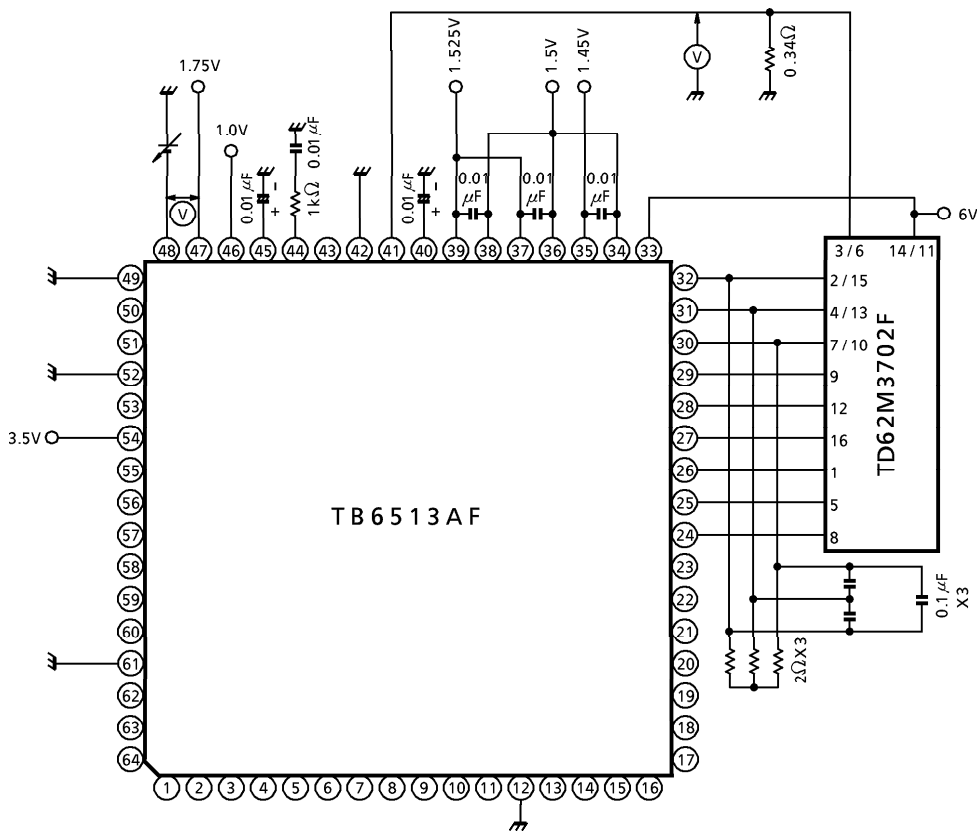
No.35 C_{ECR}

Measure the voltage of the C_{ECR} terminal.

No.58 C_{Gref}

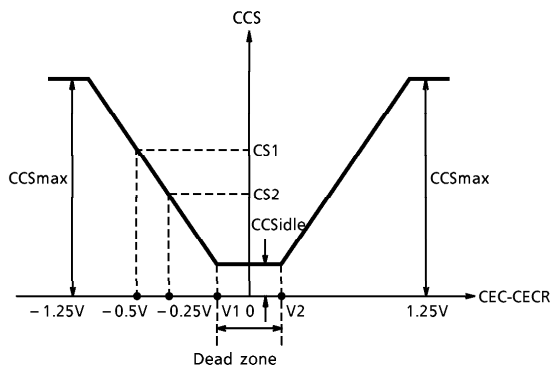
Measure the voltage of the REF terminal.

TEST CIRCUIT 12. CEC, CCSmax, CGio, CCSidle, CECofs, CECdz



No.36 No.37 No.38 No.39 No.40 No.41

Set CTL=1.0V and CECR=1.75V, change CEC from 0V to 3.5V, measure the potential of the CCS terminal, and check the voltage characteristics.



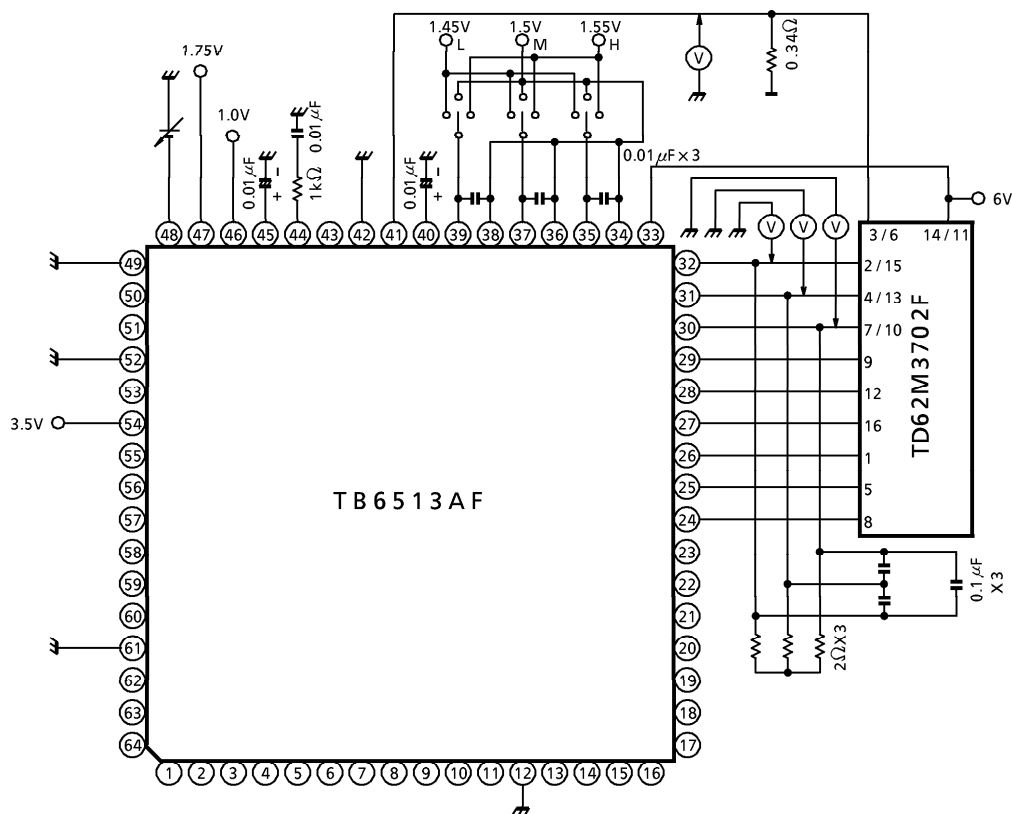
$$CGio = \frac{CS1 - CS2}{0.25V}$$

CCSide : CS potential inside the dead zone

$$CECofs = \frac{V1 + V2}{2}$$

$$CECdz = V2 - V1$$

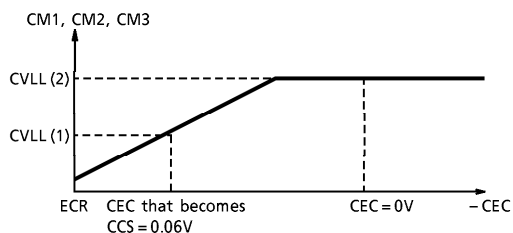
TEST CIRCUIT 13. CVLL (1), CVLL (2)



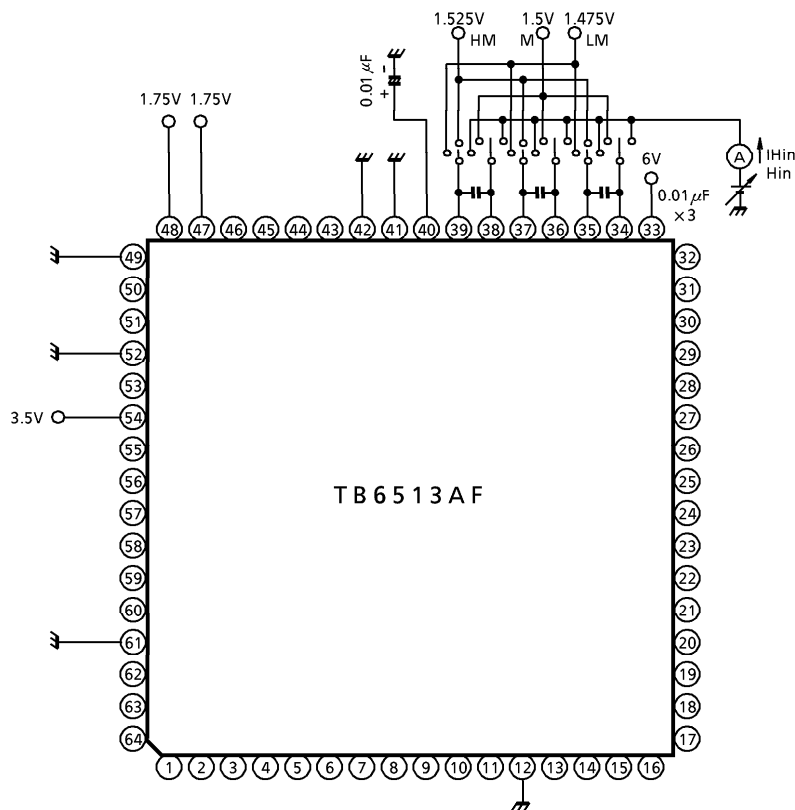
No.42 CVLL (1), No.43 CVLL (2)

Make the settings listed in the following table. Measure the potential at the CM1, CM2, and CM3 terminals when the CEC voltage is adjusted to 0V so that CCS=0.06V, and when CEC = 0V.

	H1 +	H2 +	H3 +	PIN
1	H	L	M	CM1
2	M	H	L	CM2
3	L	M	H	CM3



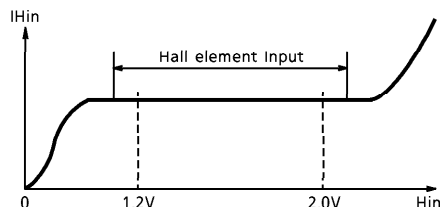
TEST CIRCUIT 14. Hin



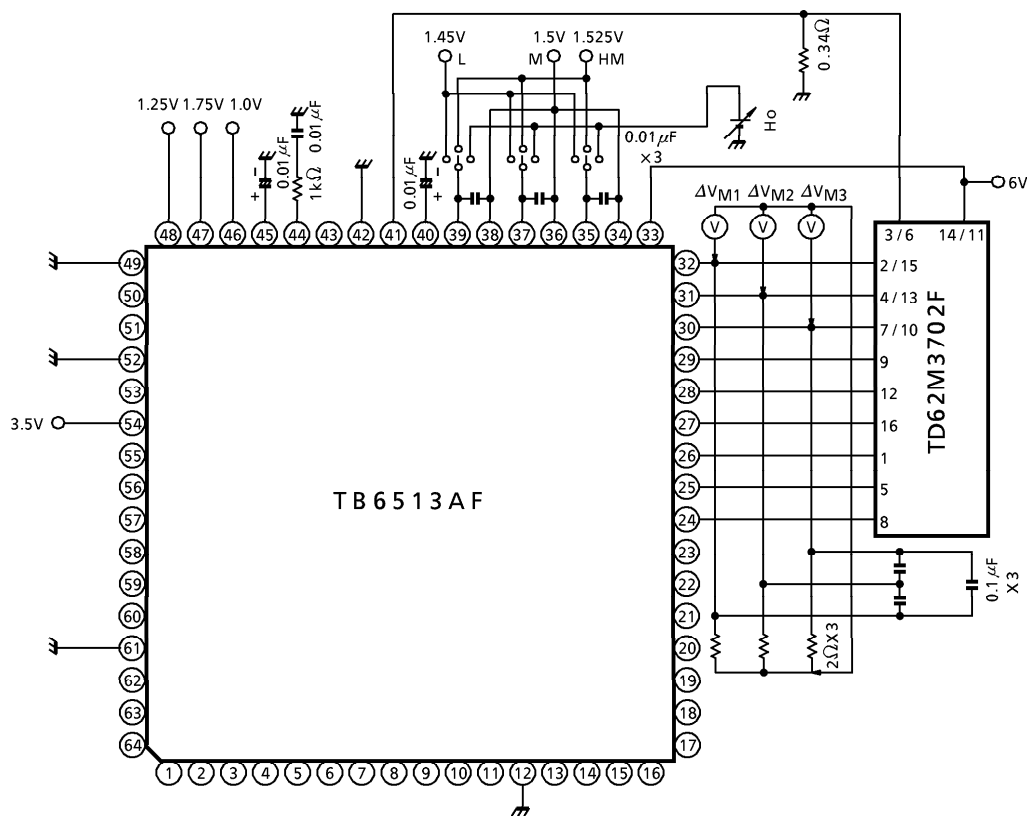
No.44 Hin

Make the settings listed in the following table. Measure the Hin voltage range in which IHin does not change rapidly versus the change in Hin.

	H1 +	H1 -	H2 +	H2 -	H3 +	H3 -
1	Hin	Hin	HM	M	LM	M
2	LM	M	Hin	Hin	HM	M
3	HM	M	LM	M	Hin	Hin



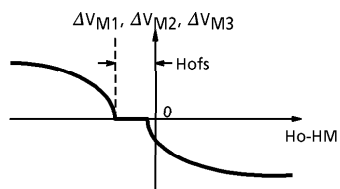
TEST CIRCUIT 15. HofS



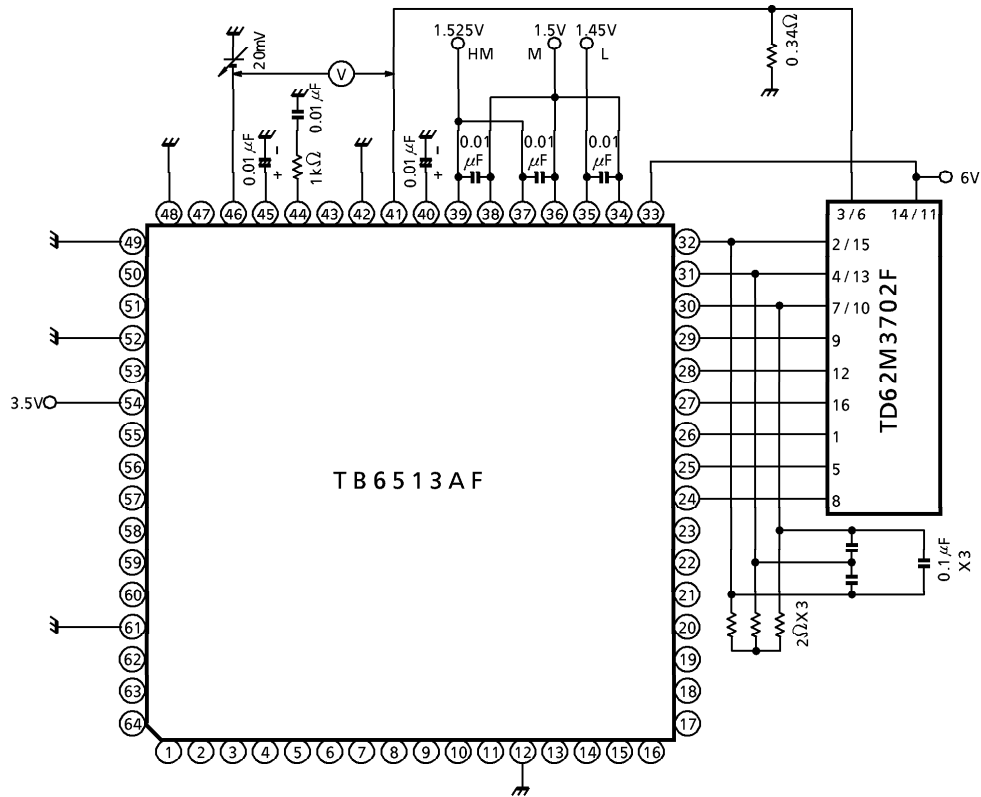
No.45 HofS

Make the settings listed in the following table, and measure the Hall element input conversion offset.

	H1 +	H2 +	H3 +	OFFSET
1	Ho	HM	L	$\Delta V_{M1} = 0$ distance between H1 + and H2 +
2	L	Ho	HM	$\Delta V_{M2} = 0$ distance between H2 + and H3 +
3	HM	L	Ho	$\Delta V_{M3} = 0$ distance between H3 + and H1 +

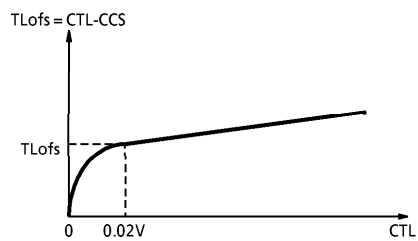


TEST CIRCUIT 16. TLofs

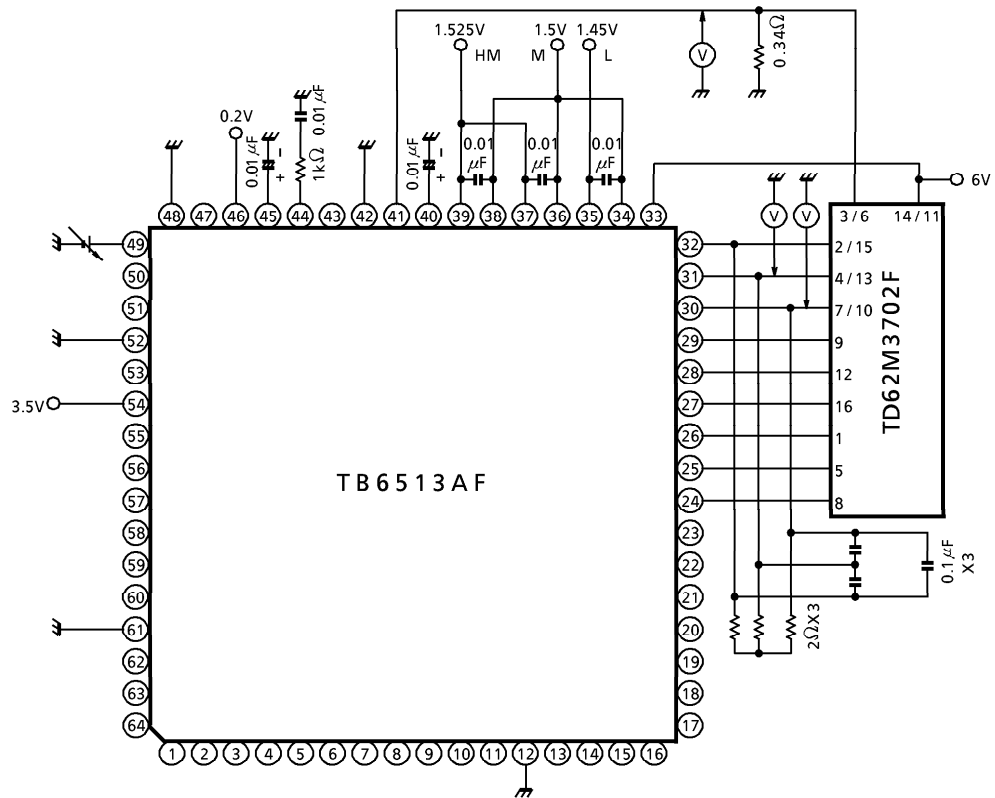


No.46 TLofs

Measure the potential differential (CTL-CCS) of the CTL and the CCS terminals when CTL = 0.02V.

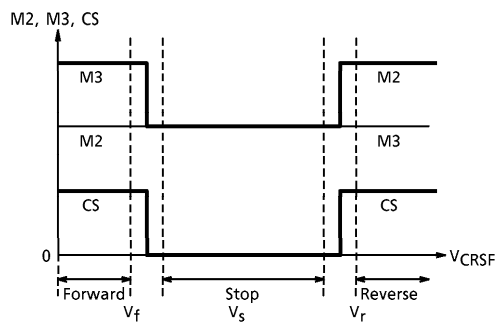


TEST CIRCUIT 17. V_f , V_s , V_r

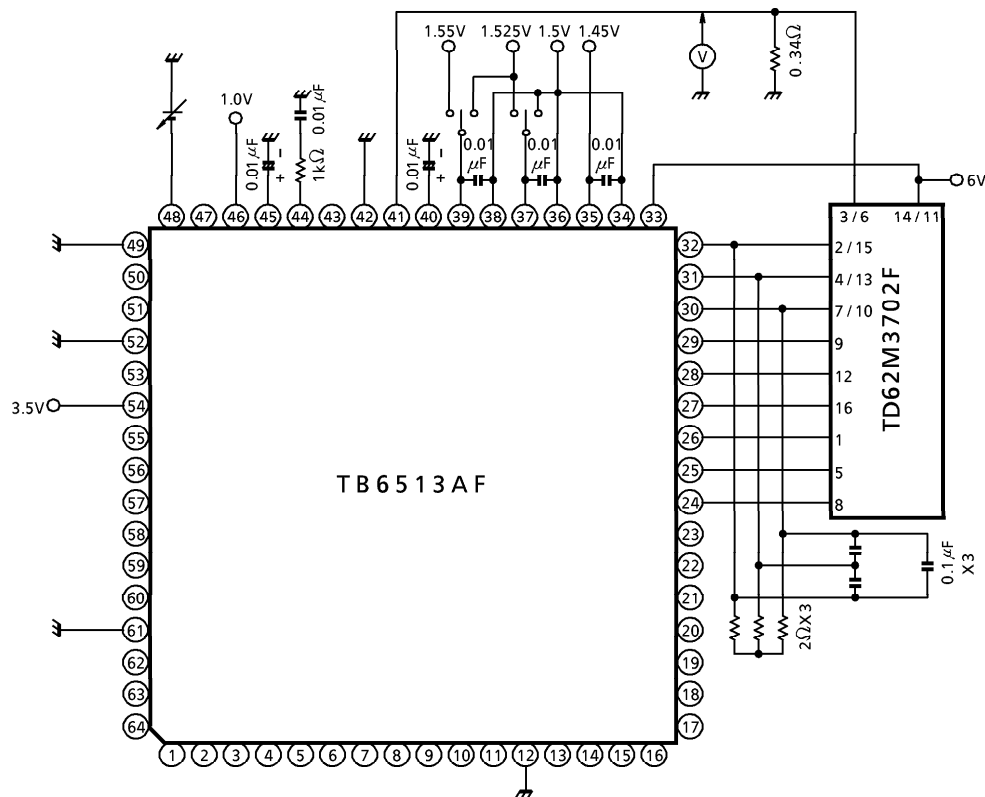


No.47 V_f , No.48 V_s , No.49 V_r

Change CRSF from 0V to 3.5V, obtain the characteristics in the following diagram, and measure the threshold voltage.



TEST CIRCUIT 18. R



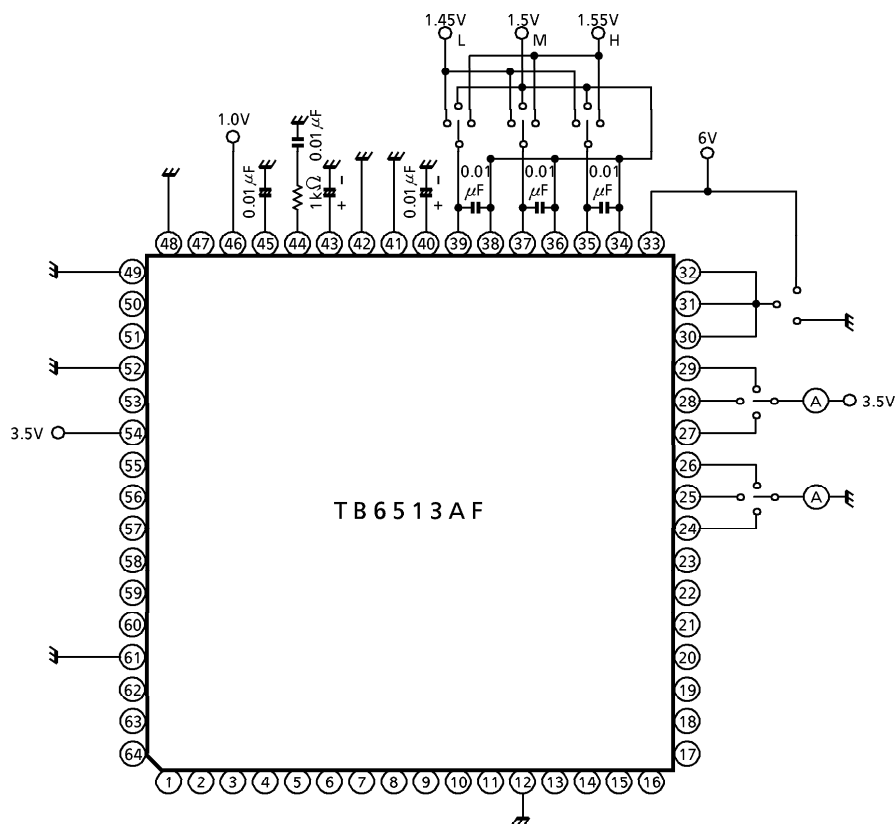
No.50 R

Adjust the CEC voltage so that CCS becomes 0.06V with H1+ = 1.525V and H2+ = 1.525V. Measure the CCS (CS_L) when H1+ = 1.525V and H2+ = 1.525V and measure the CCS (CS_H) when H1+ = 1.55V and H2+ = 1.5V.

Then determine

$$R = \frac{CS_H - CS_L}{CS_L}$$

TEST CIRCUIT 19. C_{IU} , C_{IL}

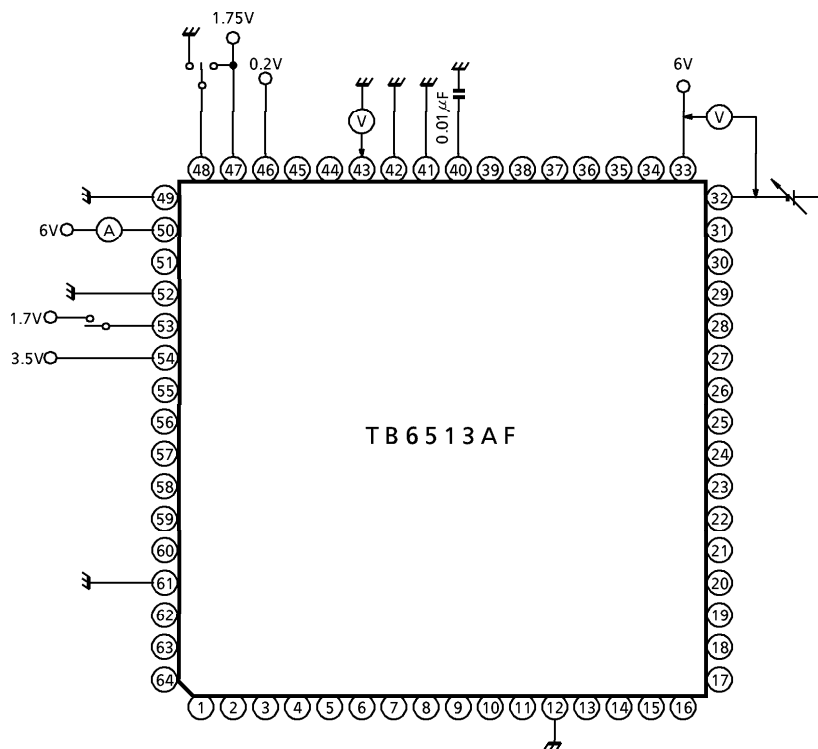


No.51 C_{IU} , No.52 C_{IL}

Make the settings in the following table, and measure the current to the CU1, CU2, and CU3 terminals, and to the CL1, CL2, and CL3 terminals.

	H1 +	H2 +	H3 +	M1, M2, M3	PIN
1	L	H	M	GND	CU1
2	M	L	H	GND	CU2
3	H	M	L	GND	CU3
4	H	L	M	V_M	CL1
5	M	H	L	V_M	CL2
6	L	M	H	V_M	CL3

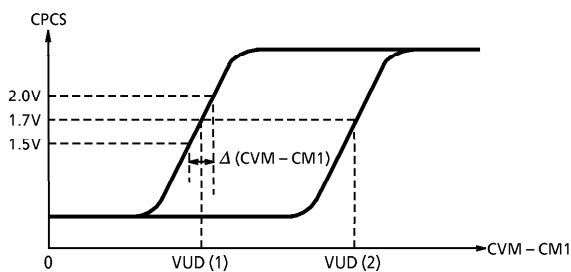
TEST CIRCUIT 20. CG_PCS, VUD (1), VUD (2), C_ISWB



No.54 CG_PCS, No.55 VUD (1), No.56 VUD (2)

Set CEC = 0V and change CM1 from 6V to 5V. Measure the potential differential (CVM - CM1) between the CVM terminal and the CM1 terminal when the potential of the CPCS terminal becomes 1.7V.

Set CEC = CECR = 1.75V, make the same measurements as above, and obtain the characteristics in the following diagram.

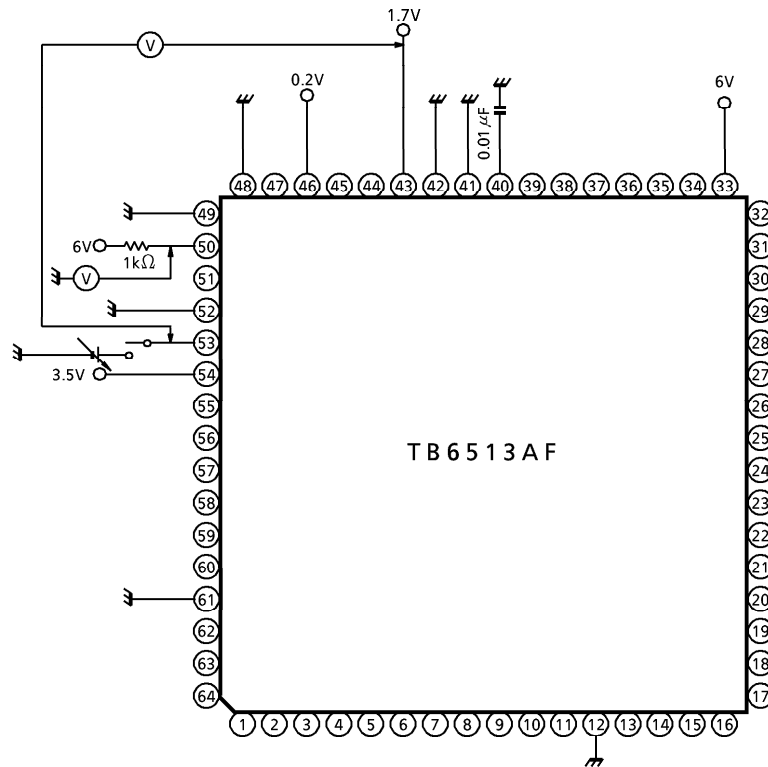


$$CG_{P}CS = \frac{2.0V - 1.5V}{\Delta (CVM - CM1)}$$

No.57 C_ISWB

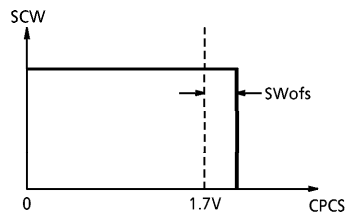
Set FC = 1.7V, CEC = 0V, and CM1 = 6V, measure the current to the SCW terminal.

TEST CIRCUIT 21. CSWofs

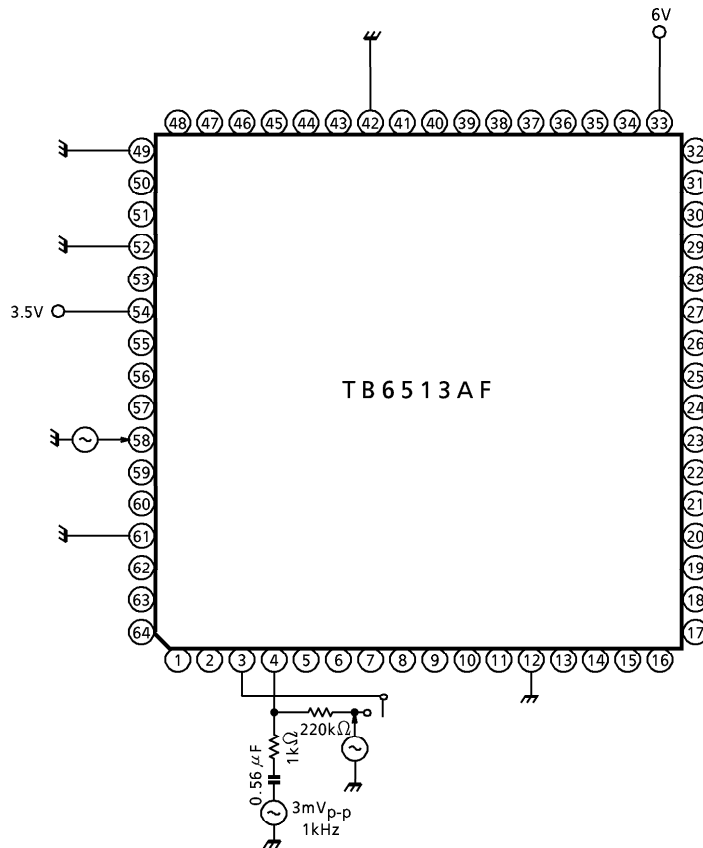


No.53 CSWofs

Set CPCS = 1.7V and change FC from 0V to 3.5V. Measure the potential differential (FC – CPCS) between the FC terminal and the CPCS terminal when SCW changes from high to low.



TEST CIRCUIT 22. CG_{FG} , CG_H , CG_L



No.59 CG_{FG} No.60 CG_H No.61 CG_L

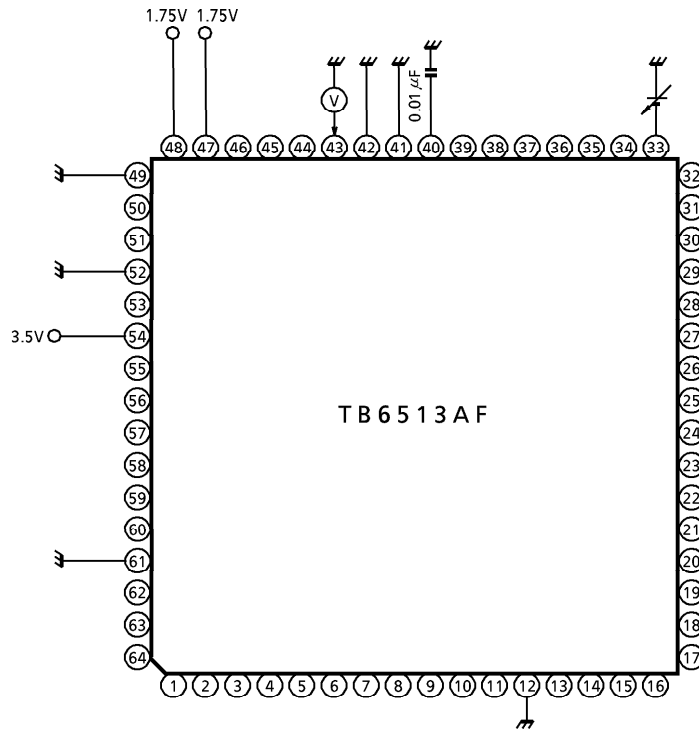
Set $CG_{out} = V_o$. When $V_{in} = 3mV_{p-p}$ at 1kHz, measure V_o and determine the following :

$$CG_{FG} = 20 \log \frac{V_o}{V_{in}}$$

Obtain the characteristics in the following diagram and measure the high-level and low-level potential of the CFG terminal output waveform.

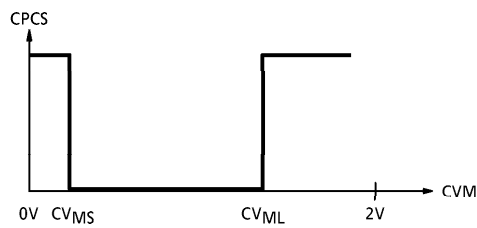


TEST CIRCUIT 23. CV_{ML} , CV_{MS}



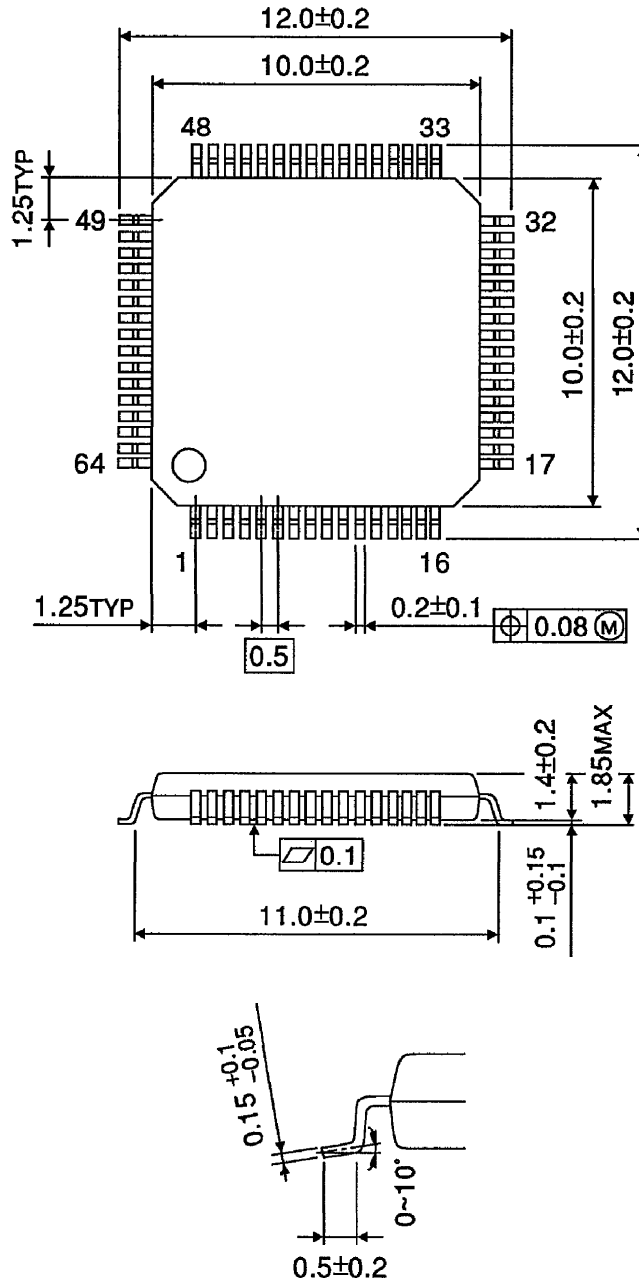
No.62 CV_{ML} No.63 CV_{MS}

Change the CVM from 2V to 0V, obtain the characteristics in the diagram below, and measure the threshold voltage.



OUTLINE DRAWING
LQFP64-P-1010-0.50A

Unit : mm



Weight : 0.34g (Typ.)