

TOSHIBA Bi-CMOS INTEGRATED CIRCUIT MULTICHIP

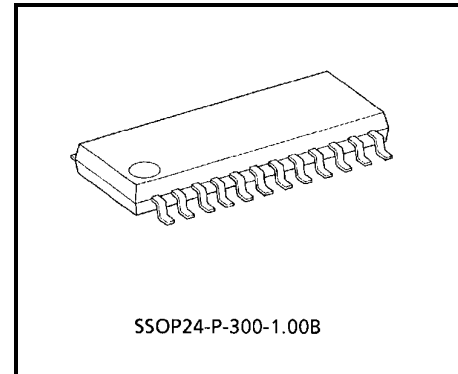
TB6512AF/AFG

PWM CHOPPER TYPE BIPOLAR STEPPING MOTOR DRIVER

The TB6512AF/AFG is PWM chopper type sinusoidal micro step bipolar stepping motor driver. Sinusoidal micro step operation is accomplished only a clock signal inputting by means of built-in hard ware.

FEATURES

- 1 chip bipolar sinusoidal micro step stepping motor driver.
- Output Current up to 150 mA
- PWM chopper type.
- Structured by high voltage Bi-CMOS process technology.
- Forward and reverse rotation are available.
- 1-2, 2W1-2 phase 1 or 2 clock drives are selectable.
- Package : SSOP24-P-300B
- Input Pull-Up Resistor equipped with RESET and ENABLE Terminal : R = 500 k Ω (Typ.)
- Output Monitor available with \overline{MO} . $I_{O(\overline{MO})} = \pm 2$ mA MAX.
- Reset and Enable are available with \overline{RESET} and \overline{ENABLE} .



SSOP24-P-300-1.00B

Weight: 0.27 g (Typ.)

TB6512AFG:

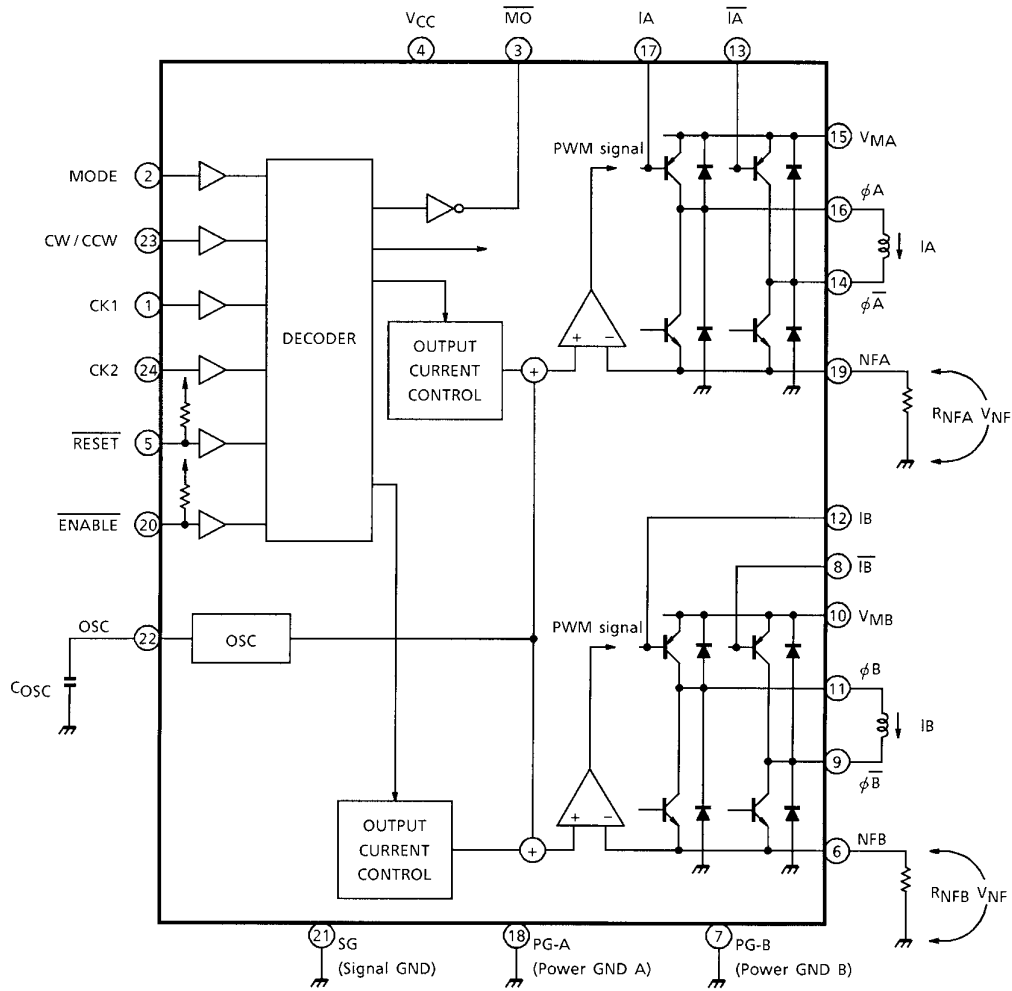
The TB6512AFG is a Pb-free product.

The following conditions apply to solderability:

*Solderability

1. Use of Sn-37Pb solder bath
 - *solder bath temperature = 230°C
 - *dipping time = 5 seconds
 - *number of times = once
 - *use of R-type flux
2. Use of Sn-3.0Ag-0.5Cu solder bath
 - *solder bath temperature = 245°C
 - *dipping time = 5 seconds
 - *the number of times = once
 - *use of R-type flux

BLOCK DIAGRAM

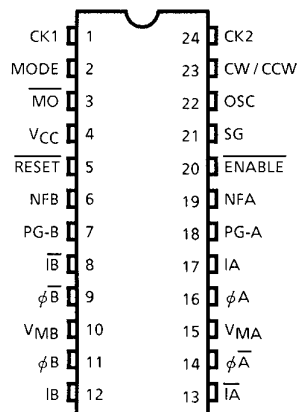


(5), (20) : Pull-up Resistor 500 kΩ (Typ.)

PIN FUNCTION

PIN No.	SYMBOL	FUNCTIONAL DESCRIPTION	
1	CK1	CLOCK Signal Input terminal	Truth table A
2	MODE	Excitation Mode Setting terminal	Truth table B
3	\overline{MO}	Monitor Output terminal	
4	V_{CC}	Power voltage supply terminal for Logic	
5	\overline{RESET}	Reset Signal Input terminal	Truth table A
6	NFB	B Channel current detective terminal	
7	PG-B	Power GND B terminal	
8	\overline{IB}	Upper PNP Transistor Base terminal	
9	$\phi \overline{B}$	Output \overline{B} terminal	
10	V_{MB}	Power voltage supply terminal for Motor B	
11	ϕB	Output B terminal	
12	IB	Upper PNP Transistor Base terminal	
13	\overline{IA}	Upper PNP Transistor Base terminal	
14	$\phi \overline{A}$	Output \overline{A} terminal	
15	V_{MA}	Power voltage supply terminal for Motor A	
16	ϕA	Output A terminal	
17	IA	Upper side PNP Transistor Base terminal	
18	PG-A	Power GND \overline{A} terminal	
19	NFA	A Channel current detective terminal	
20	\overline{ENABLE}	ENABLE Signal Input terminal	Truth table A
21	SG	Signal GND terminal	
22	OSC	Internal Oscillation frequency detective terminal	
23	CW / CCW	Forward rotation / Reverse rotation signal Input	Truth table A
24	CK2	Clock signal Input terminal	

PIN CONNECTION



TRUTH TABLE A

INPUT					MODE
CK1	CK2	CW / CCW	$\overline{\text{RESET}}$	$\overline{\text{ENABLE}}$	
	H	L	H	L	CW
	L	L	H	L	INHIBIT
H		L	H	L	CCW
L		L	H	L	INHIBIT
	H	H	H	L	CCW
	L	H	H	L	INHIBIT
H		H	H	L	CW
L		H	H	L	INHIBIT
X	X	X	L	L	INITIAL
X	X	X	X	H	Z

Z : High impedance
 X : Don't care
 Note: Do not use INHIBIT mode.

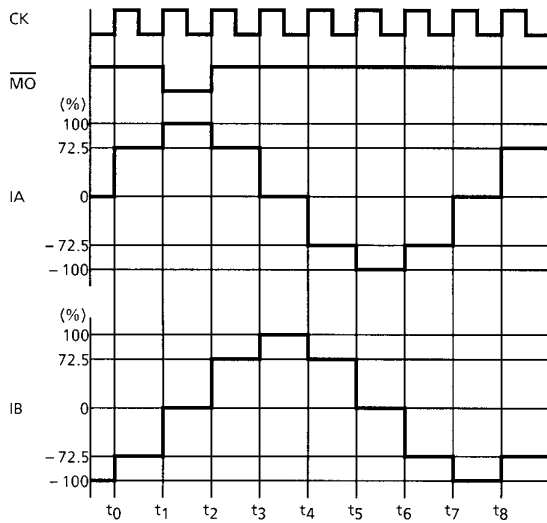
TRUTH TABLE B

INPUT	MODE (EXCITATION)
L	1-2 phase
H	2W1-2 phase

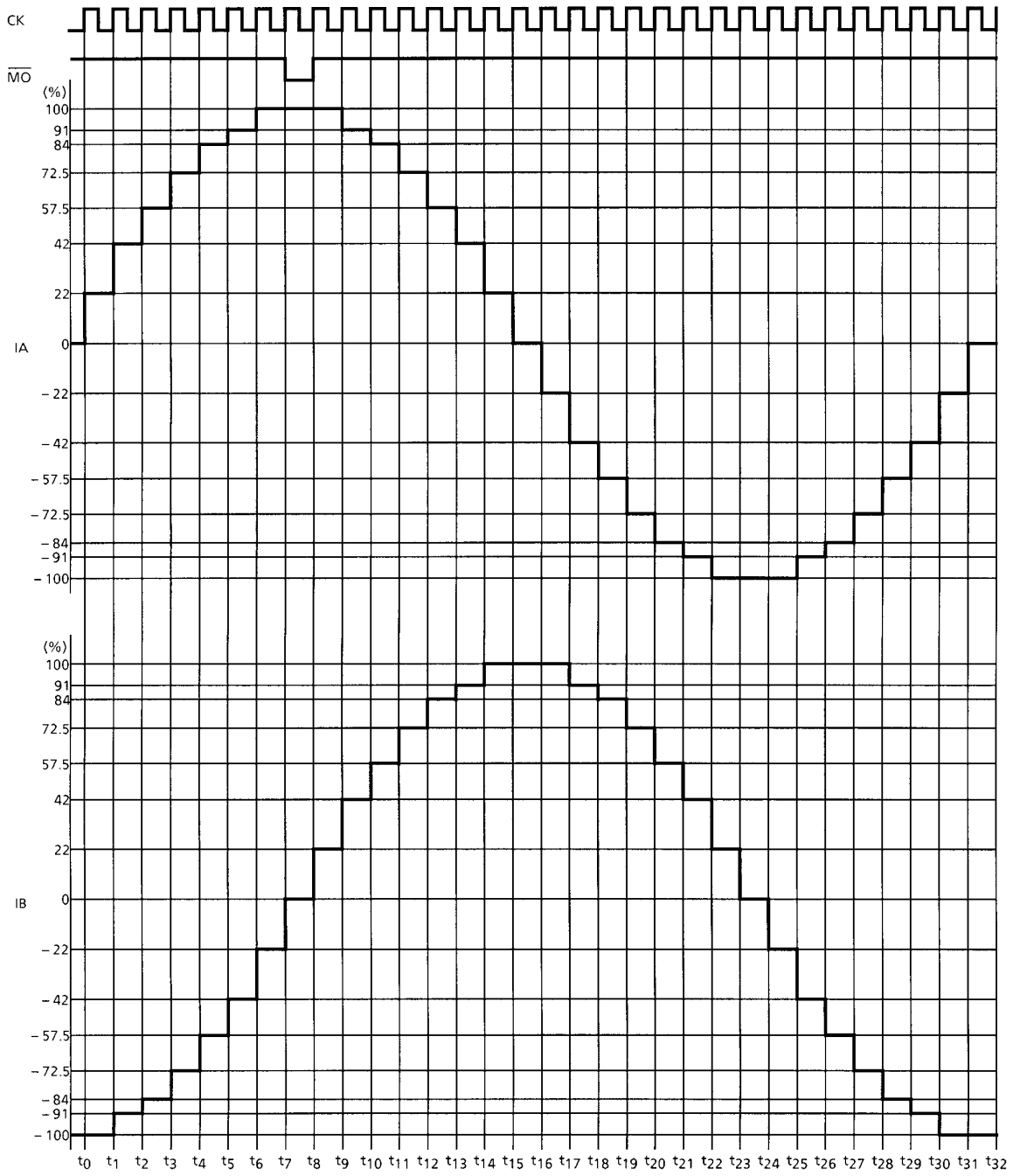
INITIAL MODE

EXCITATION MODE	$I_{OUT} (A)$	$I_{OUT} (B)$
1-2 phase	100%	0%
2W1-2 phase	100%	0%

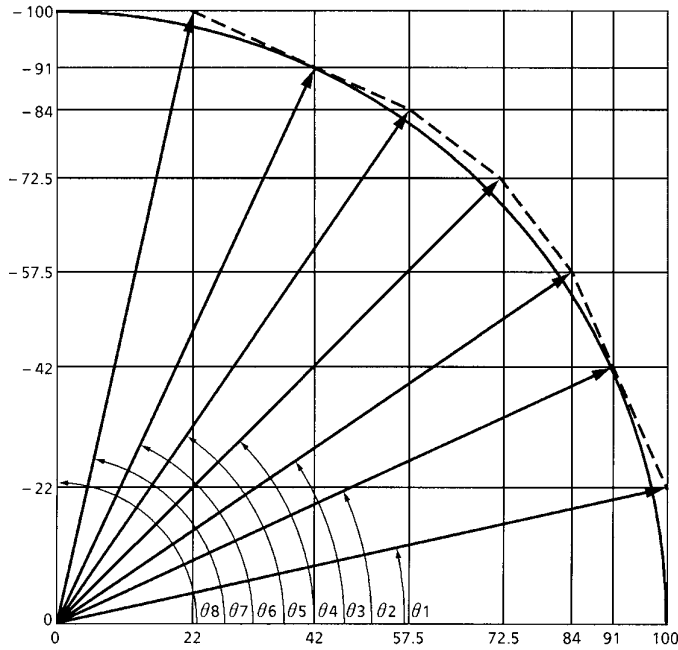
1-2 PHASE EXCITATION (MODE : L, CW mode)



2W1-2 PHASE EXCITATION (MODE : H, CW mode)



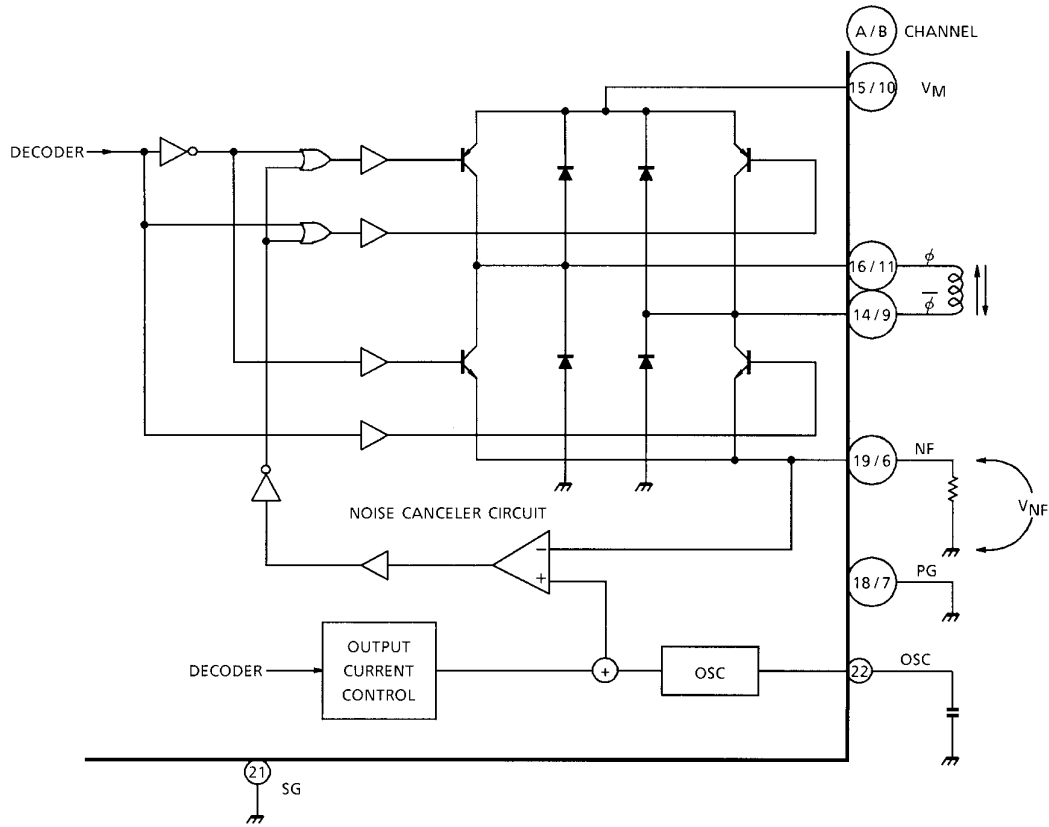
OUTPUT CURRENT VECTOR OR BIT (Normalize to 90 deg for each one step)



θ	ROTATION ANGLE		VECTOR LENGTH	
	IDEAL	TB6512AF/AFG	IDEAL	TB6512AF/AFG
θ_0	0°	0°	100	100.00
θ_1	11.25°	12.41°	100	102.39
θ_2	22.5°	27.78°	100	100.22
θ_3	33.75°	34.39°	100	101.80
θ_4	45°	45°	100	102.53
θ_5	56.25°	55.61°	100	101.81
θ_6	67.5°	65.22°	100	100.22
θ_7	78.75°	77.59°	100	102.39
θ_8	90°	90°	100	100.00

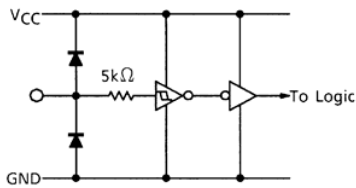
1-2 / 2W1-2 Phase

OUTPUT CIRCUIT

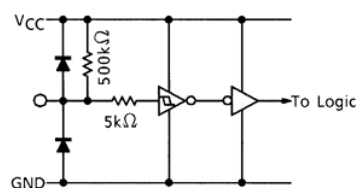


INPUT CIRCUIT

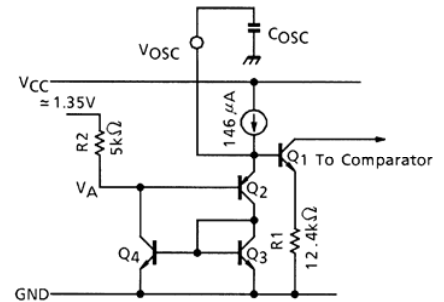
CK1, CK2, CW / CCW,
MODE Terminals



$\overline{\text{RESET}}$, $\overline{\text{ENABLE}}$ Terminals



OSC Terminals



- OSC frequency calculation

Sawtooth OSC circuit consists of Q₁ through Q₄ and R₁ through R₄.

Q₂ is turned "off" when V_{OSC} is less than the voltage of 2.5 V + V_{BE} Q₂ approximately equal to 2.05 V.

V_{OSC} is increased by C_{OSC} charging through R₁.

Q₃ and Q₄ are turned "on" when V_{OSC} becomes 2.05 V (Higher level.)

Lower level of V(22) pin is equal to V_{BE} Q₂ + V_{SAT} Q₄ approximately equal to 1.4 V.

V_{OSC} is calculated by following equation.

Assuming that V_{OSC} = 1.4 V (t = t₁) and = 2.05 (t = t₂)

C_{OSC} is external capacitance connected to pin(22) and R₁ is on-chip 10 kΩ resistor.

Therefore, OSC frequency is calculated as follows.

$$t_1 = \frac{1.0 \times C_{OSC}}{146 \times 10^{-6}}$$

$$t_2 = \frac{2.05 \times C_{OSC}}{146 \times 10^{-6}}$$

$$f_{OSC} = \frac{1}{t_2 - t_1} = \frac{146 \times 10^{-6}}{C_{OSC} (2.05 - 1.0)}$$

$$= \frac{0.139}{C_{OSC}} (\text{kHz}) \quad (C_{OSC} \text{ unit} = \mu\text{F})$$

ENABLE AND RESET FUNCTION AND MO SIGNAL

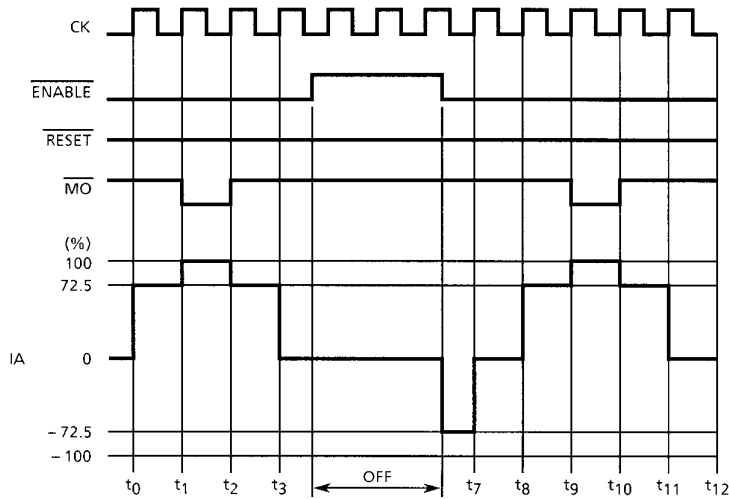


Fig.1. 1-2 phase drive mode (MODE : L)

$\overline{\text{ENABLE}}$ signal disables only Output signal. Internal logic functions are proceeded by CK signal without regard to $\overline{\text{ENABLE}}$ signal.

Therefore, Output Current is initiated from the proceeded timing point of internal logic circuit, after release of disable mode.

Fig.1 shows the $\overline{\text{ENABLE}}$ functions, when the system is selected in 1-2 phase drive mode.

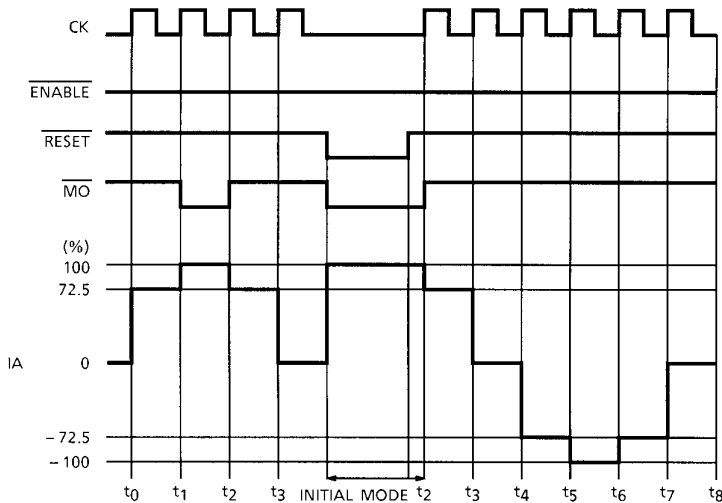


Fig.2. 1-2 phase drive mode (MODE : L)

As $\overline{\text{RESET}}$ is low, the decoder is initialized and $\overline{\text{MO}}$ is low.

After $\overline{\text{RESET}}$ is high, the motion is resumed from next clock as show in Fig.2.

$\overline{\text{MO}}$ (Monitor Output) signals is used as rotation and initial signal for stable rotation checking.

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{CC}	5.5	V
Output Voltage	V _M (opr.)	4.0~10.0	V
	V _M (MAX.)	12.0	
Output Current	I _O (MAX.)	120	mA
	AVE. I _O (\overline{MO})	±2	
Input Voltage	V _{IN}	~V _{CC}	V
Power Dissipation	P _D	0.83 (Note 1)	W
		1.04 (Note 2)	
Operating Temperature	T _{opr}	-30~85	°C
Storage Temperature	T _{stg}	-55~150	°C
Feed Back Voltage	V _I	1.0	V

Note 1: No heat sink

Note 2: With heat sink (50 × 50 × 1.6 mm Cu 10%)

RECOMMENDED OPERATING CONDITIONS (Ta = -30~85°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Supply Voltage	V _{CC} (opr.)		2.7	3.0	5.5	V
Output Voltage	V _M (opr.)		4.0	—	10.0	V
Output Current	I _{OUT}		—	—	100	mA
Input Voltage	V _{IN}		—	—	V _{CC}	V
Clock Frequency	f _{CLOCK}		—	—	5	kHz
OSC Frequency	f _{OSC}		15	—	80	kHz

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, ($T_a = 25^\circ\text{C}$, $V_{CC} = 3\text{ V}$, $V_M = 5\text{ V}$, $L = 20\text{ mH}$ / $R = 0.5\ \Omega$)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Input Voltage	High	$V_{IN(H)}$	1	MODE, CW / CCW, $\overline{\text{ENABLE}}$ CK1, CK2, $\overline{\text{RESET}}$	$V_{CC} \times 0.7$	—	$V_{CC} + 0.4$	V
	Low	$V_{IN(L)}$			GND - 0.4	—	GND + 0.3	
Input Hysteresis Voltage		V_H			—	600	—	mV
Input Current		$I_{IN-1(H)}$	1	M1, M2, REF IN, $V_{IN} = 5.0\text{ V}$	—	—	100	nA
		$I_{IN-1(L)}$		$\overline{\text{RESET}}$, $V_{IN} = 0\text{ V}$, ENABLE Internal pull-up resistor	3	6	12	μA
		$I_{IN-2(L)}$		$V_{IN} = 0\text{ V}$	—	—	100	nA
Quiescent Current V_{CC}		I_{CC1}	2	Output open, $\overline{\text{RESET}} : \text{H}$, $\overline{\text{ENABLE}} : \text{L}$, (1-2 phase excitation)	—	5	9	mA
		I_{CC2}		Output open, $\overline{\text{RESET}} : \text{H}$, $\overline{\text{ENABLE}} : \text{L}$ (2W1-2 phase excitation)	—	5	9	
		I_{CC3}		$\overline{\text{RESET}} : \text{L}$, $\overline{\text{ENABLE}} : \text{H}$	—	1.3	—	
		I_{CC4}		$\overline{\text{RESET}} : \text{H}$, $\overline{\text{ENABLE}} : \text{H}$	—	1.3	—	
Comparator Reference Voltage		V_{NF}	3	$R_{NF} = 2.5\ \Omega$, $C_{OSC} = 0.0033\ \mu\text{F}$	0.22	0.25	0.28	V
Output Diffirencial		ΔV_O	—	B / A, $C_{OSC} = 0.0033\ \mu\text{F}$ $R_{NF} = 2.5\ \Omega$	-10	—	10	%
Maximum OSC Frequency		$f_{OSC(MAX.)}$	—		100	—	—	kHz
Minimum OSC Frequency		$f_{OSC(MIN.)}$	—		—	—	10	kHz
OSC Frequency		f_{OSC}	—	$C_{OSC} = 0.0033\ \mu\text{F}$	31	44	70	kHz
Output Voltage		$V_{OH(MO)}$	—	$I_{OH} = -40\ \mu\text{A}$	2.5	—	V_{CC}	V
		$V_{OL(MO)}$	—	$I_{OL} = 40\ \mu\text{A}$	GND	0.1	0.5	

Output block

CHARACTERISTIC			SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT	
Output Saturation Voltage	Upper Side		$V_{SAT U1}$	4	$I_{OUT} = 0.12 A$	—	0.08	0.23	V	
	Lower Side		$V_{SAT L1}$			—	0.16	0.43		
	Upper Side		$V_{SAT U2}$		$I_{OUT} = 0.06 A$	—	0.06	—		
	Lower Side		$V_{SAT L2}$			—	0.10	—		
Diode Forward Voltage	Upper Side		$V_F U1$	5	$I_{OUT} = 0.12 A$	—	1.13	1.8	V	
	Lower Side		$V_F L1$			—	0.95	1.6		
Output Dark Current (A+B Channels)			I_{M1}	2	ENABLE : "H" Level RESET : "L" Level Output Open	—	—	50	μA	
			I_{M2}		ENABLE : "L" Level RESET : "H" Level Output Open,	—	17	28		mA
NF Terminal Current (1 Channels)			I_{NF}		ENABLE : "L" Level RESET : "H" Level Output Open	1	2.5	7		
A-B Chopping Current (Note)	2W1-2 ϕ	1-2 ϕ	VECTOR	3	$R_{NF} = 2.5 \Omega$ $C_{OSC} = 0.0033 \mu F$	$\theta = 0$	—	100	—	%
	2W1-2 ϕ	—				$\theta = 1 / 8$	—	100	—	
	2W1-2 ϕ	—				$\theta = 2 / 8$	86	91	96	
	2W1-2 ϕ	—				$\theta = 3 / 8$	79	84	89	
	2W1-2 ϕ	1-2 ϕ				$\theta = 4 / 8$	67.5	72.5	77.5	
	2W1-2 ϕ	—				$\theta = 5 / 8$	52.5	57.5	62.5	
	2W1-2 ϕ	—				$\theta = 6 / 8$	37	42	47	
	2W1-2 ϕ	—				$\theta = 7 / 8$	17	22	27	

Note: Maximum current ($\theta = 0$) : 100%
 2W1-2 ϕ : 2W1, 2 phase excitation mode
 W1-2 ϕ : W1, 2 phase excitation mode
 1-2 ϕ : 1, 2 phase excitation mode

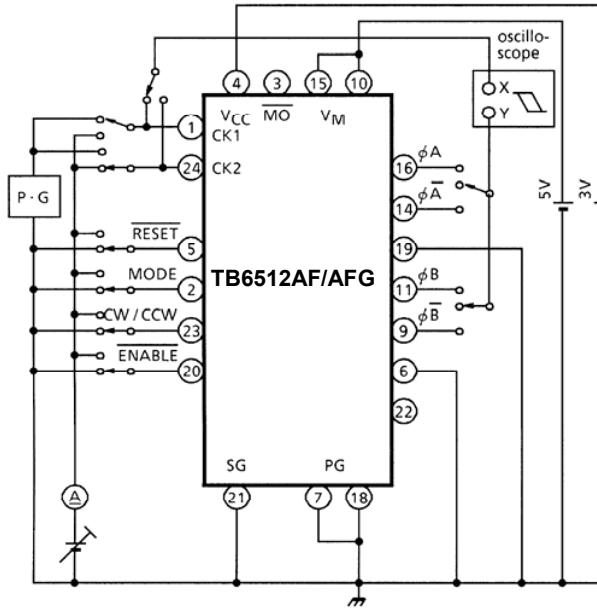
ELECTRICAL CHARACTERISTICS

Unless otherwise specified, ($T_a = 25^\circ\text{C}$, $V_{CC} = 3\text{ V}$, $V_M = 5\text{ V}$, $L = 20\text{mH}$ / $R = 0.5\ \Omega$)

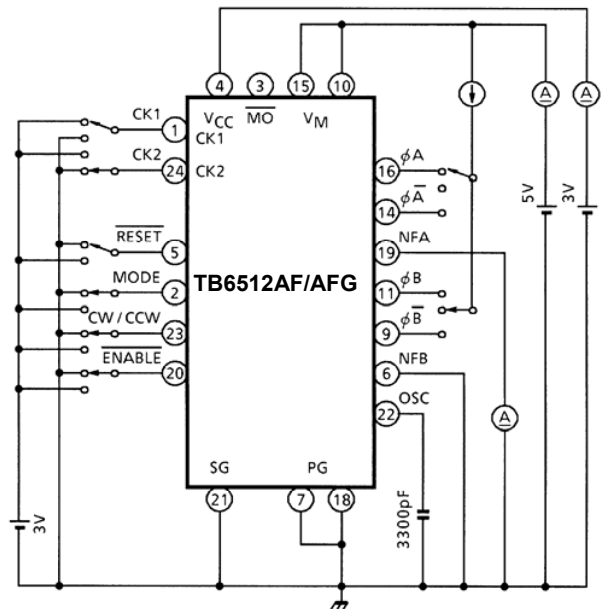
CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT				
A-B Chopping Current (Note)	2W1-2 ϕ	1-2 ϕ	VECTOR	3	$\theta = 0$ $\theta = 1/8$ $\theta = 2/8$ $\theta = 3/8$ $\theta = 4/8$ $\theta = 5/8$ $\theta = 6/8$ $\theta = 7/8$ $R_{NF} = 3.3\ \Omega$ $C_{OSC} = 0.0033\ \mu\text{F}$ $L = 5\text{mH} / R = 50\ \Omega$	—	100	—	%			
	2W1-2 ϕ	—				—	100	—				
	2W1-2 ϕ	—				—	91.1	—				
	2W1-2 ϕ	—				—	83.6	—				
	2W1-2 ϕ	1-2 ϕ				—	72.6	—				
	2W1-2 ϕ	—				—	60.0	—				
	2W1-2 ϕ	—				—	44.5	—				
	2W1-2 ϕ	—				—	24.3	—				
	Reference Voltage					ΔV_{NF}	7	$R_{NF} = 2.5\ \Omega$ $C_{OSC} = 0.0033\ \mu\text{F}$		—	0	—
$\Delta\theta = 0/8-1/8$				10	22.5				35			
$\Delta\theta = 1/8-2/8$				5	17.5				30			
$\Delta\theta = 2/8-3/8$				16.25	28.75				41.25			
$\Delta\theta = 3/8-4/8$				25	37.5				50			
$\Delta\theta = 4/8-5/8$				26.25	38.75				51.25			
$\Delta\theta = 5/8-6/8$				37.5	50				62.5			
Output Tr Switching Characteristics				7	$R_L = 2\ \Omega$, $V_{NF} = 0\text{ V}$, $C_L = 15\ \mu\text{F}$	—	0.3	—	μs			
						t_r	—	2.2		—		
						t_f	CK ~ Output			—	1.5	—
						t_{pLH}	OSC ~ Output			—	2.7	—
						t_{pHL}	OSC ~ Output			—	5.4	—
						t_{pLH}	OSC ~ Output			—	6.3	—
						t_{pHL}	RESET ~ Output			—	2.0	—
						t_{pLH}	RESET ~ Output			—	2.5	—
						t_{pHL}	ENABLE ~ Output			—	5.0	—
						t_{pHL}	ENABLE ~ Output			—	6.0	—
Output Leakage Current	Upper Side	I_{OH}	6	$V_M = 12\text{ V}$	—	—	50	μA				
	Upper Side	I_{OL}			—	—	50					

Note: Maximum current ($\theta = 0$) : 100%
 2W1-2 ϕ : 2W1, 2 phase excitation mode
 W1-2 ϕ : W1, 2 phase excitation mode
 1-2 ϕ : 1,2 phase excitation mode

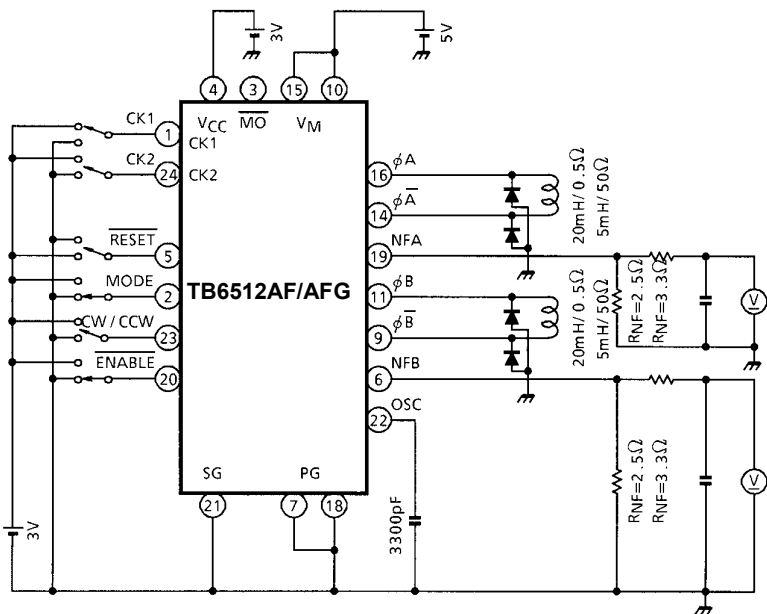
TEST CIRCUIT 1 : V_{IN} (H), (L), I_{IN} (H), (L)



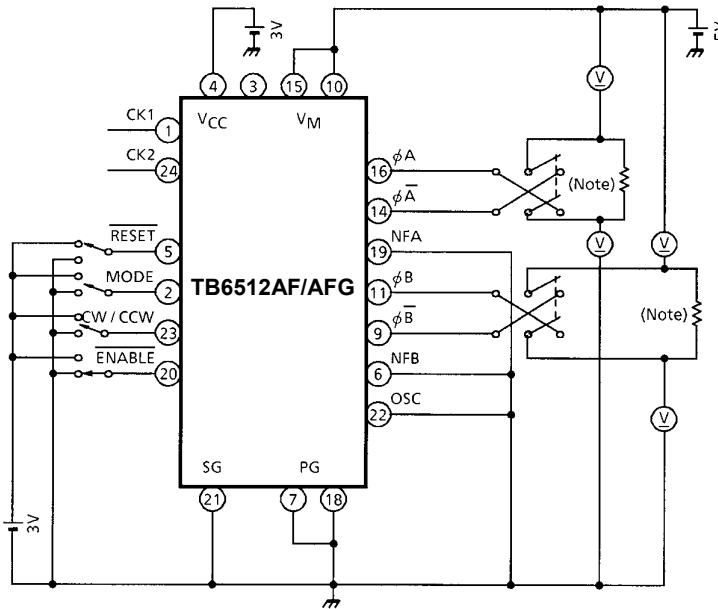
TEST CIRCUIT 2 : I_{CC} , I_M , I_{NF}



TEST CIRCUIT 3 : V_{NF}

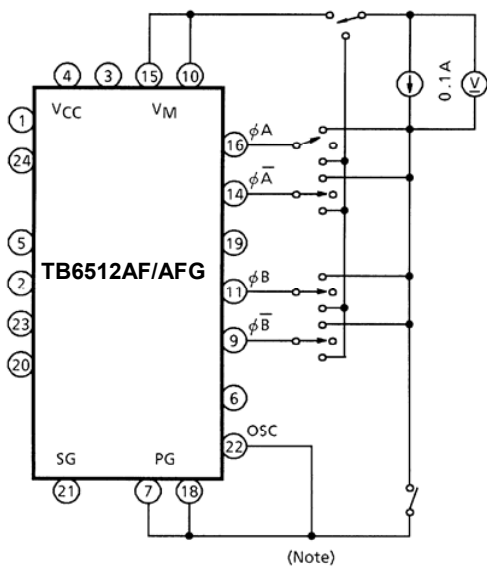


TEST CIRCUIT 4 : $V_{CE(SAT)}$ Upper, lower

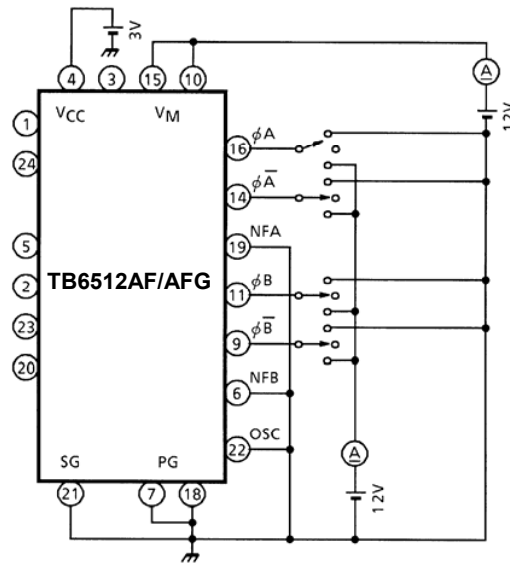


Note: Calibrate Output Current becomes 0.06 A (or 0.10 A) with this resistor.

TEST CIRCUIT 5 : V_{F-U} , V_{F-L}



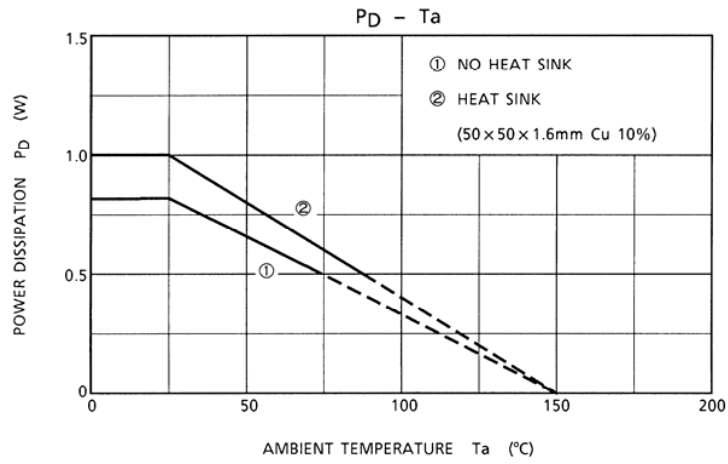
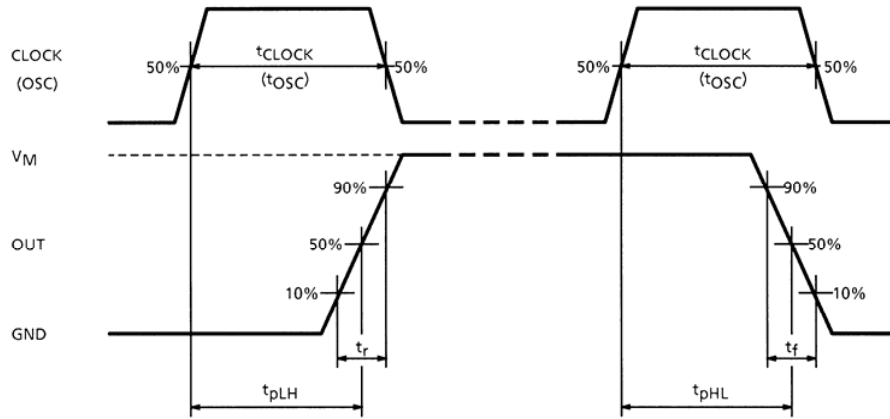
TEST CIRCUIT 6 : I_{OH} , I_{OL}



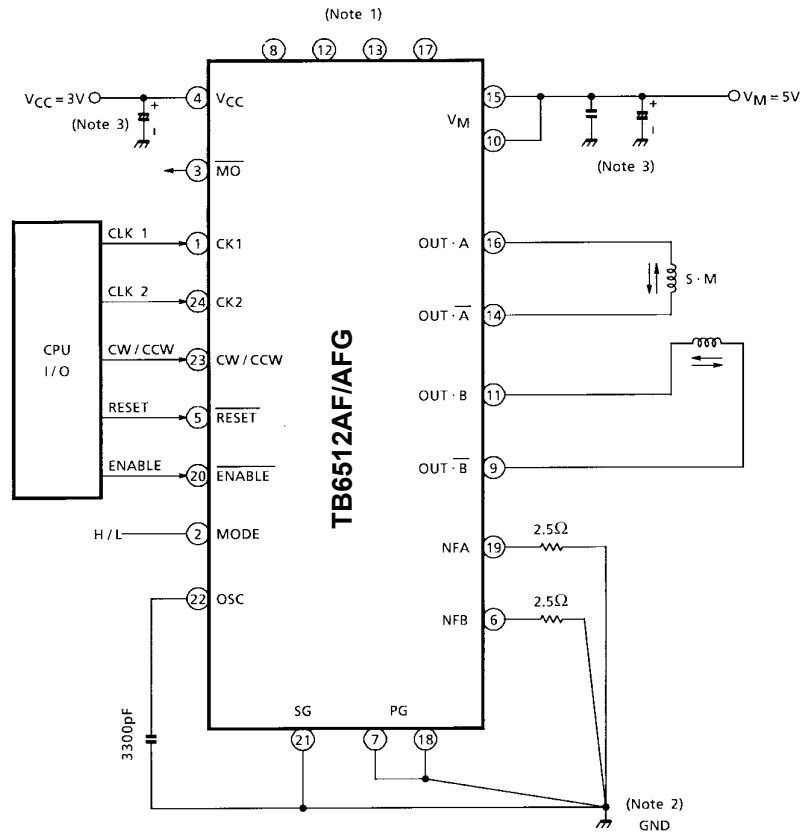
Note: Not to take a GND with any non-connecting Pins.

AC ELECTRICAL, CHARACTERICAL

CK (OSC) - OUT



APPLICATION CIRCUIT



Note 1: (8), (12), (13), (17) pin : open

Note 2: GND pattern to be laid out at one point in order to prevent common impedance.

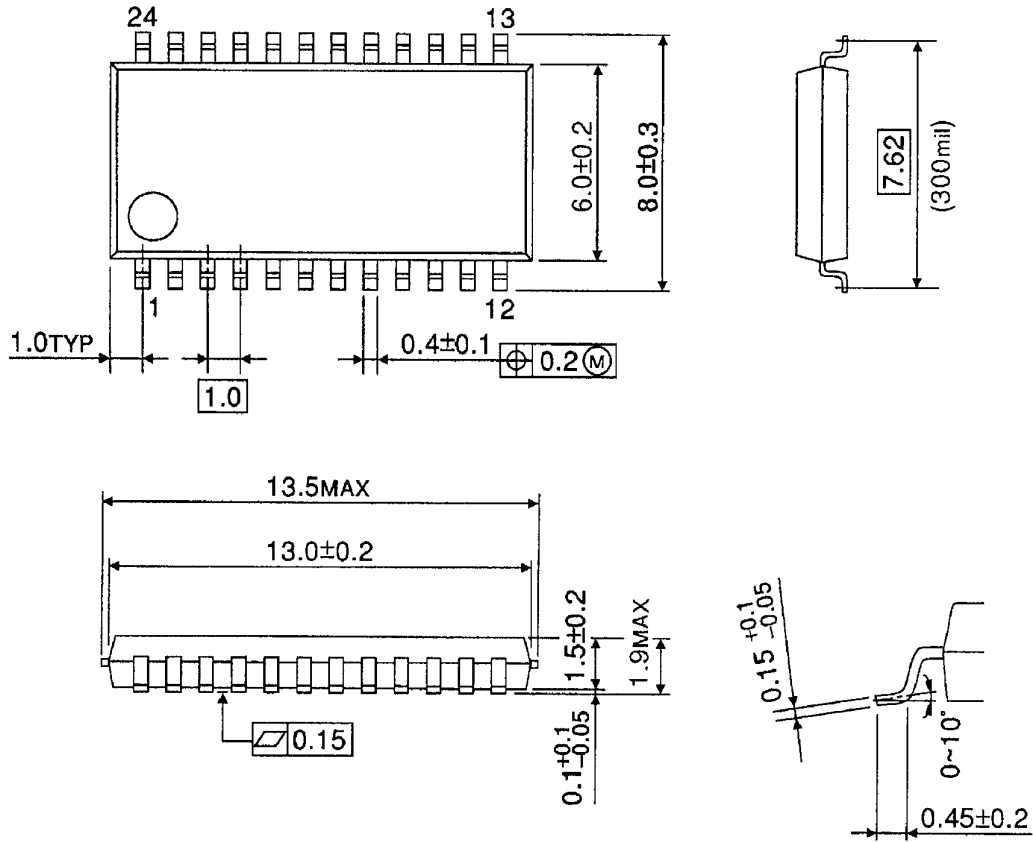
Note 3: Capacitor for noise suppression to be connected between the Power Supply (V_{CC} , V_M) and GND to stabilize the operation.

Note 4: Utmost care is necessary in the design of the output, V_{CC} , V_M , and GND lines since the IC may be destroyed by short-circuiting between outputs, air contamination faults, or faults due to improper grounding, or by short-circuiting between contiguous pins.

PACKAGE DIMENSIONS

SSOP24-P-300-1.00B

Unit: mm



Weight: 0.27 g (Typ.)

Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.

Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on handling of ICs

- [1] The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result in injury by explosion or combustion.
- [2] Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead to smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.
- [3] If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.
- [4] Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result in injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

Points to remember on handling of ICs**(1) Heat Radiation Design**

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_j) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into consideration the effect of IC heat radiation with peripheral components.

(2) Back-EMF

When a motor rotates in the reverse direction, stops or slows down abruptly, a current flows back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

RESTRICTIONS ON PRODUCT USE

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- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.
In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the "Handling Guide for Semiconductor Devices," or "TOSHIBA Semiconductor Reliability Handbook" etc. 021023_A
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