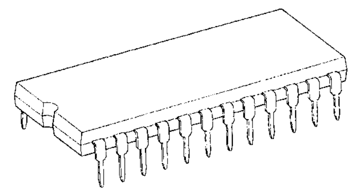
TOSHIBA Bi−CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

TB6528P

FIVE−PHASE STEPPING MOTOR DRIVE CONTROLLER

The TB6528P universal controller for stepping motor drives is a Bi−CMOS monolithic−type IC for controlling five−phase stepping motors.
This IC enables five−phase stepping motor drive units to be configured simply by preparing a pulse oscillator, a switching element and a direct current power source. This IC was developed in order to simplify the use of stepping motors.



DIP24-P-600-2.54

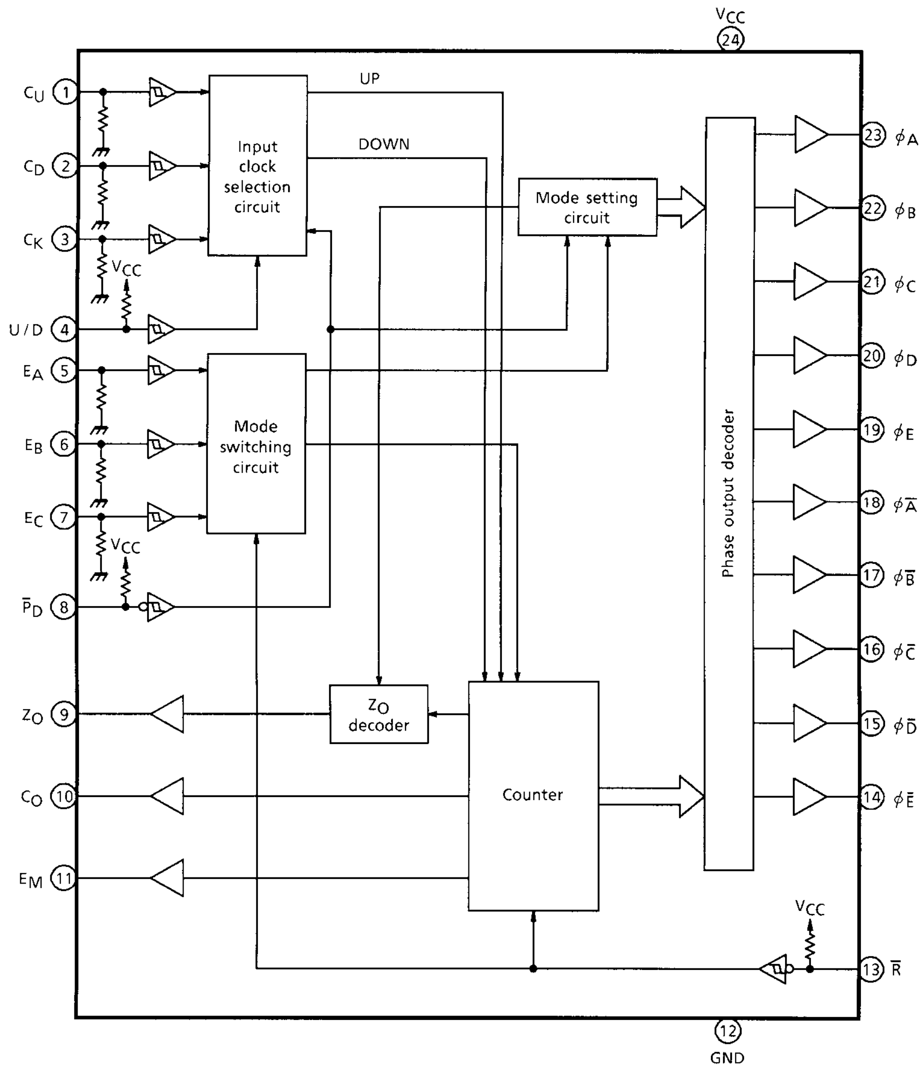
Weight: 3.38 g (Typ.)

FEATURES

- Universal controller : The excitation mode switching terminal enables the selection of the following eight modes.
  - Uni−polar type : 2 excitation, 2−3 excitation, 3 excitation
  - Bi−polar type : 2−3 excitation, 3 excitation, 4 excitation, 4−5 excitation, 5 excitation
- Operating suplly voltage range : V_{CC} = 4~16 V
- High−output current : 20 mA min (source)
- High noise margin : All input pin are equipped with a Schmidt circuit.
- Two types of pulse input : 2 input pin method (CW and CCW input modes). 1 input / 1 switching pin method (CK and U / D input modes).
- Power down function : All output is at the “L” level
- Excitation mode protection function : No fluctuations in output even when switching excitation modes such as 2Ex ↔ 2−3Ex ↔ 3Ex, 4Ex ↔ 4−5Ex ↔ 5Ex.
- Reset function : Moves the phase home position across to the excitation status.
- Phase home position monitor : “H” level is output when at the phase home position (output in the reset mode).
- Excitation status identification monitor : The controller’s operating status is output as a monitor signal.
- Input pulse monitor : The input is output as a monitor signal.

The TB6528P is a Pb-free product.
The following conditions apply to solderability:
*Solderability
1. Use of Sn-37Pb solder bath
   *solder bath temperature = 230°C
   *dipping time = 5 seconds
   *number of times = once
   *use of R-type flux
2. Use of Sn-3.0Ag-0.5Cu solder bath
   *solder bath temperature = 245°C
   *dipping time = 5 seconds
   *number of times = once
   *use of R-type flux

BLOCK DIAGRAM

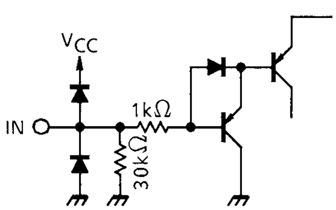


PIN FUNCTION

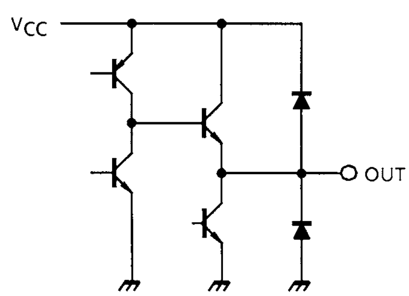
PIN No.	PIN SYMBOL	PIN FUNCTION	
1	C_U	Input pulse UP clock	Truth table A
2	C_D	Input pulse DOWN clock	
3	C_K	Input pulse clock	
4	U / D	Converts rotation directions “0” is DOWN, “1” is UP	
5	E_A	Excitation mode switching input	Truth table B
6	E_B		
7	E_C		
8	$\overline{P}_D$	All output becomes “L” when power down is “L”	
9	Z_O	Phase home position monitor	
10	C_O	Input pulse monitor	
11	E_M	Excitation monitor	
12	GND	GND	
13	$\overline{R}$	Reset when the reset input is “L”	
14	$\varphi_{\overline{E}}$	$\varphi_{\overline{E}}$ Output	
15	$\varphi_{\overline{D}}$	$\varphi_{\overline{D}}$ Output	
16	$\varphi_{\overline{C}}$	$\varphi_{\overline{C}}$ Output	
17	$\varphi_{\overline{B}}$	$\varphi_{\overline{B}}$ Output	
18	$\varphi_{\overline{A}}$	$\varphi_{\overline{A}}$ Output	
19	φ_E	φ_E Output	
20	φ_D	φ_D Output	
21	φ_C	φ_C Output	
22	φ_B	φ_B Output	
23	φ_A	φ_A Output	
24	V_{CC}	V_{CC}	

EQUIVALENT I / O CIRCUIT

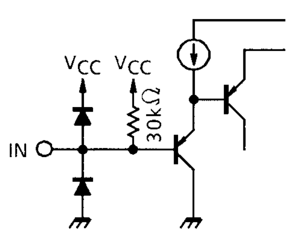
C_U, C_D, C_K



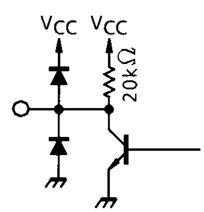
φ_A~φ_E and $\varphi_{\overline{A}}$~$\varphi_{\overline{E}}$



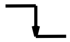
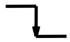
U / D, $\overline{P}_D$, $\overline{R}$



Z_O, C_O, E_M



TRUTH TABLE A

C_U	C_D	C_K	U / D	FUNCTION
	L	L	*	CW
L		L	*	CCW
L	L		H	CW
L	L		L	CCW

Note 1: * means Don't Care
Note 2: The C_U pin is an input pin when counting up, and the C_D pin is an input pin when counting down.
Note 3: The C_K pin is the count pulse input pin, and count−up and count−down is determined by the U / D pin.

TRUTH TABLE B

E_A	E_B	E_C	$\overline{R}$	$\overline{P}_D$	FUNCTION	EXCITATION TYPE
L	H	H	H	H	2 Excitation	Uni−polar type
L	L	H	H	H	2−3 Excitation	
H	L	H	H	H	3 Excitation	
H	H	L	H	H	2−3 Excitation	Bi−polar type
H	H	H	H	H	3 Excitation	
L	H	L	H	H	4 Excitation	
L	L	L	H	H	4−5 Excitation	
H	L	L	H	H	5 Excitation	

Note 4: The output enters the initial status when $\overline{R}$ is set at the LOW level, and the Z_O output indicates the High level.
Note 5: The input clock signal is prohibited and the phase output terminals (φA~φE and φ$\overline{A}$ ~φ$\overline{E}$) enter the LOW level when $\overline{P}_D$ is set at the LOW level.
Z_O, C_O and E_M output is not prohibited.

FUNCTION 1 (Uni−polar type)

2 EXCITATION

PULSE / PHASE	0 (RESET)	1	2	3	4	5
φA	H	L	L	L	H	H
φB	H	H	L	L	L	H
φC	L	H	H	L	L	L
φD	L	L	H	H	L	L
φE	L	L	L	H	H	L
φ$\overline{A}$	L	L	L	L	L	L
φ$\overline{B}$	L	L	L	L	L	L
φ$\overline{C}$	L	L	L	L	L	L
φ$\overline{D}$	L	L	L	L	L	L
φ$\overline{E}$	L	L	L	L	L	L
Z_O	H	L	L	L	L	H
E_M	L	L	L	L	L	L
UP	→					
DOWN	←					

2−3 EXCITATION

PULSE / PHASE	0 (RESET)	1	2	3	4	5	6	7	8	9	10
φA	H	H	L	L	L	L	L	H	H	H	H
φB	H	H	H	H	L	L	L	L	L	H	H
φC	L	H	H	H	H	H	L	L	L	L	L
φD	L	L	L	H	H	H	H	H	L	L	L
φE	L	L	L	L	L	H	H	H	H	H	L
φ$\overline{A}$	L	L	L	L	L	L	L	L	L	L	L
φ$\overline{B}$	L	L	L	L	L	L	L	L	L	L	L
φ$\overline{C}$	L	L	L	L	L	L	L	L	L	L	L
φ$\overline{D}$	L	L	L	L	L	L	L	L	L	L	L
φ$\overline{E}$	L	L	L	L	L	L	L	L	L	L	L
Z_O	H	L	L	L	L	L	L	L	L	L	H
E_M	L	H	L	H	L	H	L	H	L	H	L
UP	→										
DOWN	←										

3 EXCITATION

PHASE \ PULSE	0 (RESET)	1	2	3	4	5
φ_A	H	H	L	L	H	H
φ_B	H	H	H	L	L	L
φ_C	L	H	H	H	L	L
φ_D	L	L	H	H	H	L
φ_E	H	L	L	H	H	H
$\varphi_{\overline{A}}$	L	L	L	L	L	L
$\varphi_{\overline{B}}$	L	L	L	L	L	L
$\varphi_{\overline{C}}$	L	L	L	L	L	L
$\varphi_{\overline{D}}$	L	L	L	L	L	L
$\varphi_{\overline{E}}$	L	L	L	L	L	L
Z_O	H	L	L	L	L	H
E_M	H	H	H	H	H	H
UP	→					
DOWN	←					

FUNCTION 2 (Bi−polar type)

2−3 EXCITATION

PHASE \ PULSE	0 (RESET)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
$\varphi_{A'}$	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	L	L	L	L	L
$\varphi_{B'}$	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H
$\varphi_{C'}$	L	L	L	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L
$\varphi_{D'}$	L	L	L	L	L	L	L	L	L	H	H	H	H	H	L	L	L	L	L	L	L
$\varphi_{E'}$	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	L
$\varphi_{\overline{A}'}$	L	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
$\varphi_{\overline{B}'}$	L	L	L	L	L	L	L	H	H	H	H	H	L	L	L	L	L	L	L	L	L
$\varphi_{\overline{C}'}$	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	L	L	L
$\varphi_{\overline{D}'}$	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H
$\varphi_{\overline{E}'}$	L	L	L	L	L	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L
Z_O	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H
E_M	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L
UP	→																				
DOWN	←																				

3 EXCITATION

PHASE \ PULSE	0 (RESET)	1	2	3	4	5	6	7	8	9	10
$\phi_{A'}$	L	L	L	L	L	L	H	H	H	L	L
$\phi_{B'}$	H	H	L	L	L	L	L	L	L	H	H
$\phi_{C'}$	L	L	H	H	H	L	L	L	L	L	L
$\phi_{D'}$	L	L	L	L	L	H	H	H	L	L	L
$\phi_{E'}$	H	L	L	L	L	L	L	L	H	H	H
$\phi_{\overline{A}'}$	L	H	H	H	L	L	L	L	L	L	L
$\phi_{\overline{B}'}$	L	L	L	L	H	H	H	L	L	L	L
$\phi_{\overline{C}'}$	L	L	L	L	L	L	L	H	H	H	L
$\phi_{\overline{D}'}$	H	H	H	L	L	L	L	L	L	L	H
$\phi_{\overline{E}'}$	L	L	L	H	H	H	L	L	L	L	L
Z_O	H	L	L	L	L	L	L	L	L	L	H
E_M	H	H	H	H	H	H	H	H	H	H	H
UP	→										
DOWN	←										

4 EXCITATION

PHASE \ PULSE	0 (RESET)	1	2	3	4	5	6	7	8	9	10
ϕ_A	H	L	L	L	L	L	L	H	H	H	H
ϕ_B	H	H	L	L	L	L	L	L	H	H	H
ϕ_C	H	H	H	L	L	L	L	L	L	H	H
ϕ_D	H	H	H	H	L	L	L	L	L	L	H
ϕ_E	L	H	H	H	H	L	L	L	L	L	L
$\phi_{\overline{A}}$	L	L	H	H	H	H	L	L	L	L	L
$\phi_{\overline{B}}$	L	L	L	H	H	H	H	L	L	L	L
$\phi_{\overline{C}}$	L	L	L	L	H	H	H	H	L	L	L
$\phi_{\overline{D}}$	L	L	L	L	L	H	H	H	H	L	L
$\phi_{\overline{E}}$	L	L	L	L	L	L	H	H	H	H	L
Z_O	H	L	L	L	L	L	L	L	L	L	H
E_M	L	L	L	L	L	L	L	L	L	L	L
UP	→										
DOWN	←										

4−5 EXCITATION

PHASE \ PULSE	0 (RESET)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
ϕ_A	H	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H
ϕ_B	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H
ϕ_C	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H
ϕ_D	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	H	H
ϕ_E	L	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L
$\phi_{\bar{A}}$	L	L	L	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L
$\phi_{\bar{B}}$	L	L	L	L	L	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L
$\phi_{\bar{C}}$	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	L	L	L	L	L
$\phi_{\bar{D}}$	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	L	L	L
$\phi_{\bar{E}}$	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	L
Z_O	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H
E_M	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L
UP	→																				
DOWN	←																				

5 EXCITATION

PHASE \ PULSE	0 (RESET)	1	2	3	4	5	6	7	8	9	10
ϕ_A	H	H	L	L	L	L	L	H	H	H	H
ϕ_B	H	H	H	L	L	L	L	L	H	H	H
ϕ_C	H	H	H	H	L	L	L	L	L	H	H
ϕ_D	H	H	H	H	H	L	L	L	L	L	H
ϕ_E	L	H	H	H	H	H	L	L	L	L	L
$\phi_{\bar{A}}$	L	L	H	H	H	H	H	L	L	L	L
$\phi_{\bar{B}}$	L	L	L	H	H	H	H	H	L	L	L
$\phi_{\bar{C}}$	L	L	L	L	H	H	H	H	H	L	L
$\phi_{\bar{D}}$	L	L	L	L	L	H	H	H	H	H	L
$\phi_{\bar{E}}$	H	L	L	L	L	L	H	H	H	H	H
Z_O	H	L	L	L	L	L	L	L	L	L	H
E_M	H	H	H	H	H	H	H	H	H	H	H
UP	→										
DOWN	←										

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Power Suplly Voltage		V_{CC}	−0.5~20	V
Output Current φn	“H” LEVEL	I_{OH} φ	−30	mA
	“L” LEVEL	I_{OL} φ	2	
Output Current (C_O, E_M, Z_O)	“H” LEVEL	I_{OH}	−50	μA
	“L” LEVEL	I_{OL}	2	mA
Input Voltage		V_{IN}	−0.5~V_{CC}	V
Input Current		I_{IN}	±1	mA
Power Dissipation		P_D	1000	mW
Operating Temperature		T_{opr}	−20~85	°C
Storage Temperature		T_{stg}	−55~150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = −30~85°C)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Power Suplly Voltage		V_{CC}	—	4	—	13	V
Output Current φn	“H” LEVEL	I_{OH} φ	—	—	—	−10	mA
	“L” LEVEL	I_{OL} φ	—	—	—	1.6	
Output Current (C_O, E_M, Z_O)	“H” LEVEL	I_{OH}	—	—	—	−40	μA
	“L” LEVEL	I_{OL}	—	—	—	1.6	mA
Input Voltage		V_{IN}	—	0	—	V_{CC}	V
Clock Frequency		—	—	0	—	250	kHz

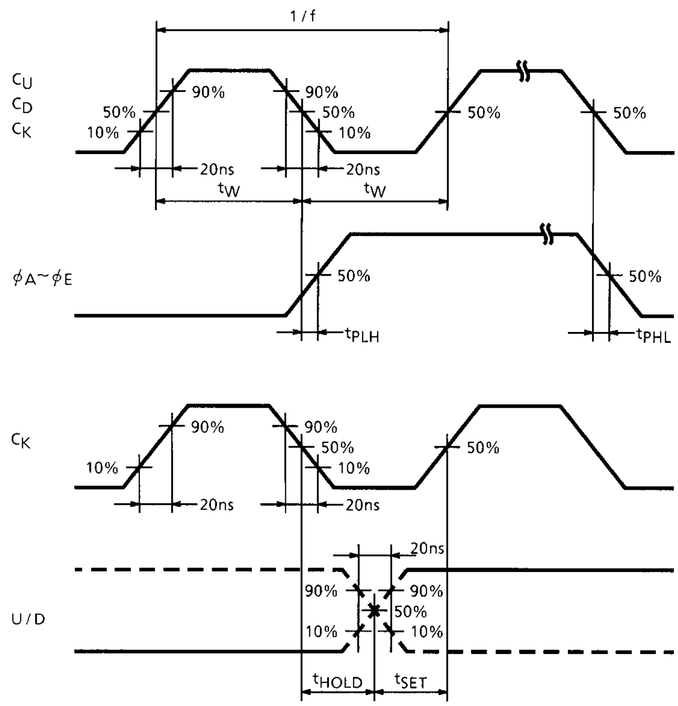
ELECTRICAL CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CIR– CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Output Current $φ_A$~φ E	"H" level	I_{OH}	—	V_{CC} = 5 V, V_O = V_{CC}−2.0	−20	—	—	mA
			—	V_{CC} = 10 V, V_O = V_{CC}−2.0	−20	—	—	
	"L" level	I_{OL}	—	V_{CC} = 5 V, V_O = 0.3 V	1.6	—	—	mA
			—	V_{CC} = 10 V, V_O = 0.3 V	1.6	—	—	
Output Current C_O, E_M, Z_O	"H" level	V_{OH}	—	V_{CC} = 5 V, I_O = −40 μA	3.6	—	—	V
			—	V_{CC} = 10 V, I_O = −40 μA	8.6	—	—	
	"L" level	V_{OL}	—	V_{CC} = 5 V, I_O = 1.6 mA	—	—	0.4	V
			—	V_{CC} = 10 V, I_O = 1.6 mA	—	—	0.6	
Input Voltage	"H" level	V_{IH}	—	V_{CC} = 5 V	3.0	2.5	—	V
			—	V_{CC} = 10 V	6.0	5.0	—	
	"L" level	V_{IL}	—	V_{CC} = 5 V	—	2.0	1.5	V
			—	V_{CC} = 10 V	—	4.0	3.0	
Input Current C_U, C_D, C_K E_A, E_B, E E_C	"H" level	I_{IH}	—	V_{CC} = 5 V, V_{IN} = V_{CC}−0.5 V	—	—	0.4	mA
			—	V_{CC} = 10 V, V_{IN} = V_{CC}−0.5 V	—	—	0.7	
	"L" level	I_{IL}	—	V_{CC} = 5 V, V_{IN} = 0 V	—	—	±10	μA
			—	V_{CC} = 10 V, V_{IN} = 0 V	—	—	±10	
Input Current U / D, $\overline{P}_D$, $\overline{R}$	"H" level	I_{IH}	—	V_{CC} = 5 V, V_{IN} = V_{CC}−0.5 V	—	—	−100	μA
			—	V_{CC} = 10 V, V_{IN} = V_{CC}−0.5 V	—	—	−100	
	"L" level	I_{IL}	—	V_{CC} = 5 V, V_{IN} = 0 V	—	—	−0.4	mA
			—	V_{CC} = 10 V, V_{IN} = 0 V	—	—	−0.7	
Static Current Consumption		I_{CC}	—	V_{CC} = 5 V, all pins open	—	—	25	mA
			—	V_{CC} = 10 V, all pins open	—	—	35	

SWITCHING CHARACTERISTICS (Ta = 25°C)

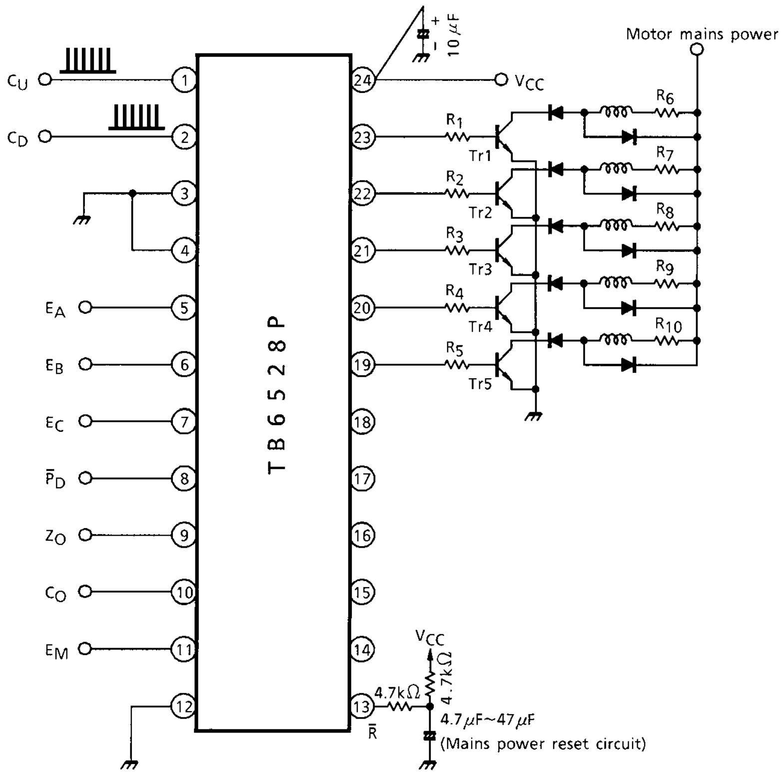
CHARACTERISTIC	SYMBOL	TEST CIR−CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Maximum Clock Frequency	f_{MAX}	—	V_{CC} = 5 V	250	300	—	kHz
		—	V_{CC} = 10 V	270	350	—	
Minimum Clock Pulse Width	t_W	—	V_{CC} = 5 V	—	300	500	ns
		—	V_{CC} = 10 V	—	300	500	
Minimum Reset Pulse Width	t_{WR}	—	V_{CC} = 5 V	—	200	500	ns
		—	V_{CC} = 10 V	—	200	500	
Delay Time (φ output from clock input)	t_{PLH}	—	V_{CC} = 5 V	—	2500	3500	ns
	t_{PHL}	—	V_{CC} = 10 V	—	2500	3500	
Delay Time (each monitor from clock input)	t_{PLH}	—	V_{CC} = 5 V	—	3000	4000	ns
	t_{PHL}	—	V_{CC} = 10 V	—	3000	4000	
Setting Time	t_{SET}	—	V_{CC} = 5 V	4000	3000	—	ns
		—	V_{CC} = 10 V	4000	3000	—	
Storage Time	t_{HOLD}	—	V_{CC} = 5 V	500	0	—	ns
		—	V_{CC} = 10 V	500	0	—	

MEASURED WAVE−FORM FOR SWITCHING TIME



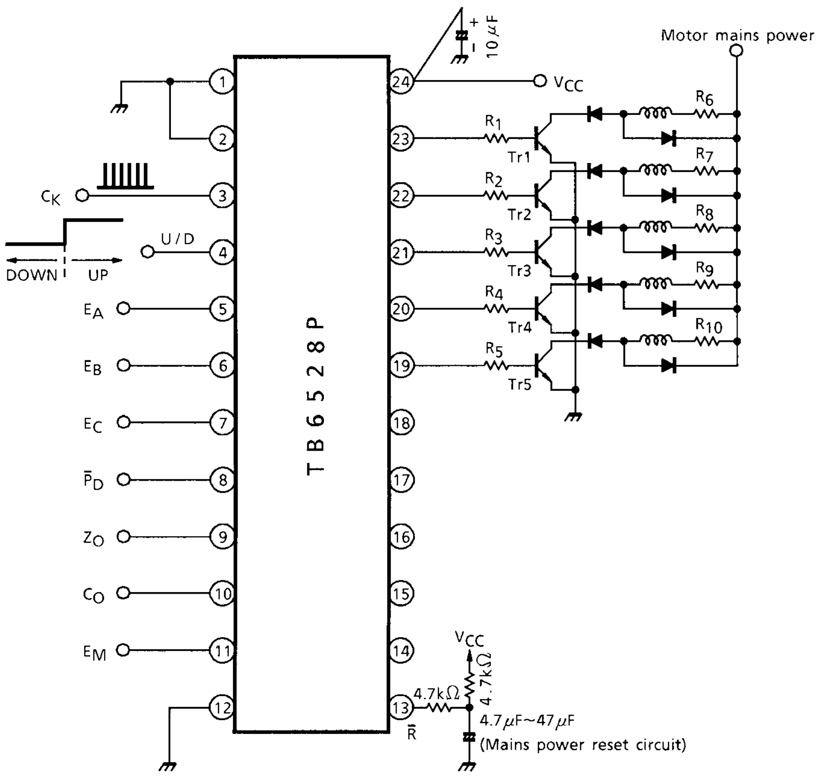
APPLICATION CIRCUIT 1

2 input pin method



APPLICATION CIRCUIT 2

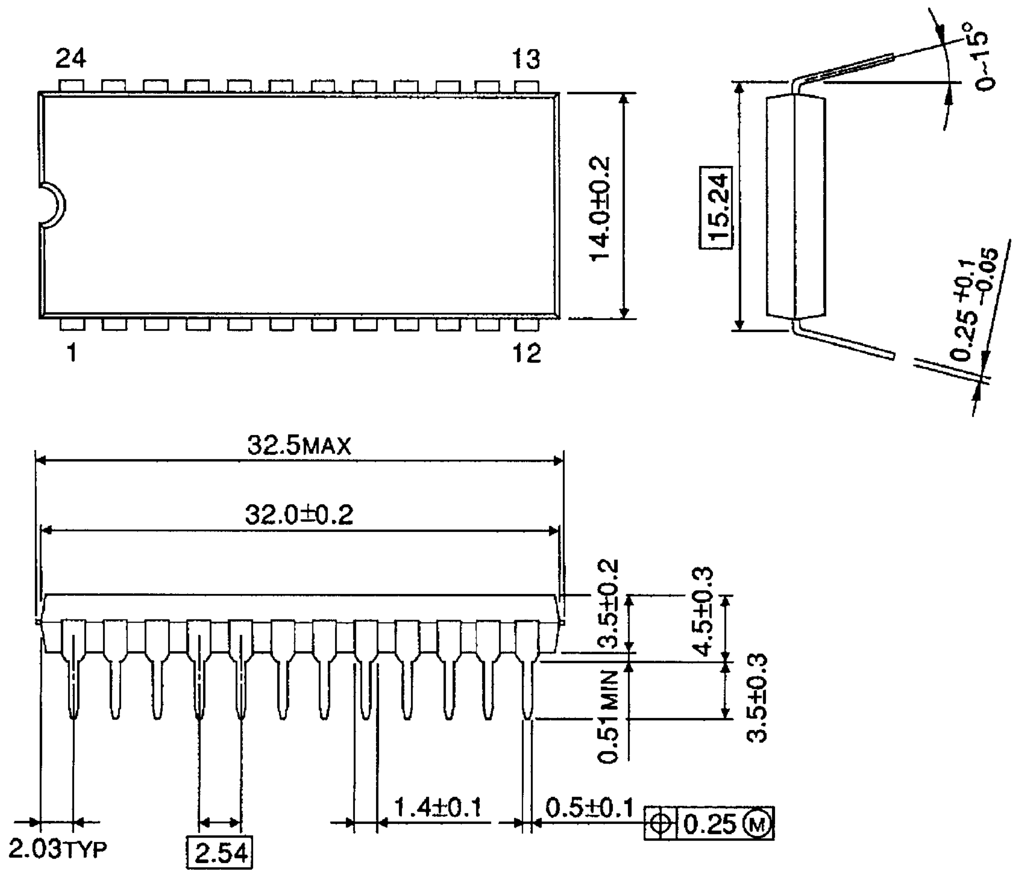
1 input / switting pin method



(Note)
Utmost care is necessary in the design of the output, VCC, VM, and GND lines since the IC may be destroyed by short-circuiting between outputs, air contamination faults, or faults due to improper grounding, or by short-circuiting between contiguous pins.

PACKAGE DIMENSIONS

DIP24−P−600−2.54 Unit: mm



Weight: 3.38 g (Typ.)

Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.
Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on handling of ICs

[1] The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

[2] Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

Points to remember on handling of ICs

(1) Back-EMF
When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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