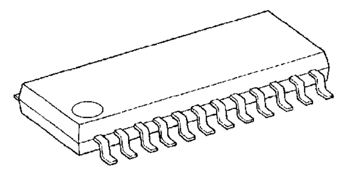
TOSHIBA Bi−CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

TB6526AF/AFG

CHOPPER−TYPE BIPOLAR STEPPING MOTOR CONTROL DRIVER IC

The TB6526AF/AFG is a PWM chopper−type sinusoidal micro−step bipolar stepping motor driver IC.
It is capable of 1−2 and 2W1−2 phase excitation modes and forward and reverse rotation modes, low−vibration, low−torque ripple, and high−efficiency driving.



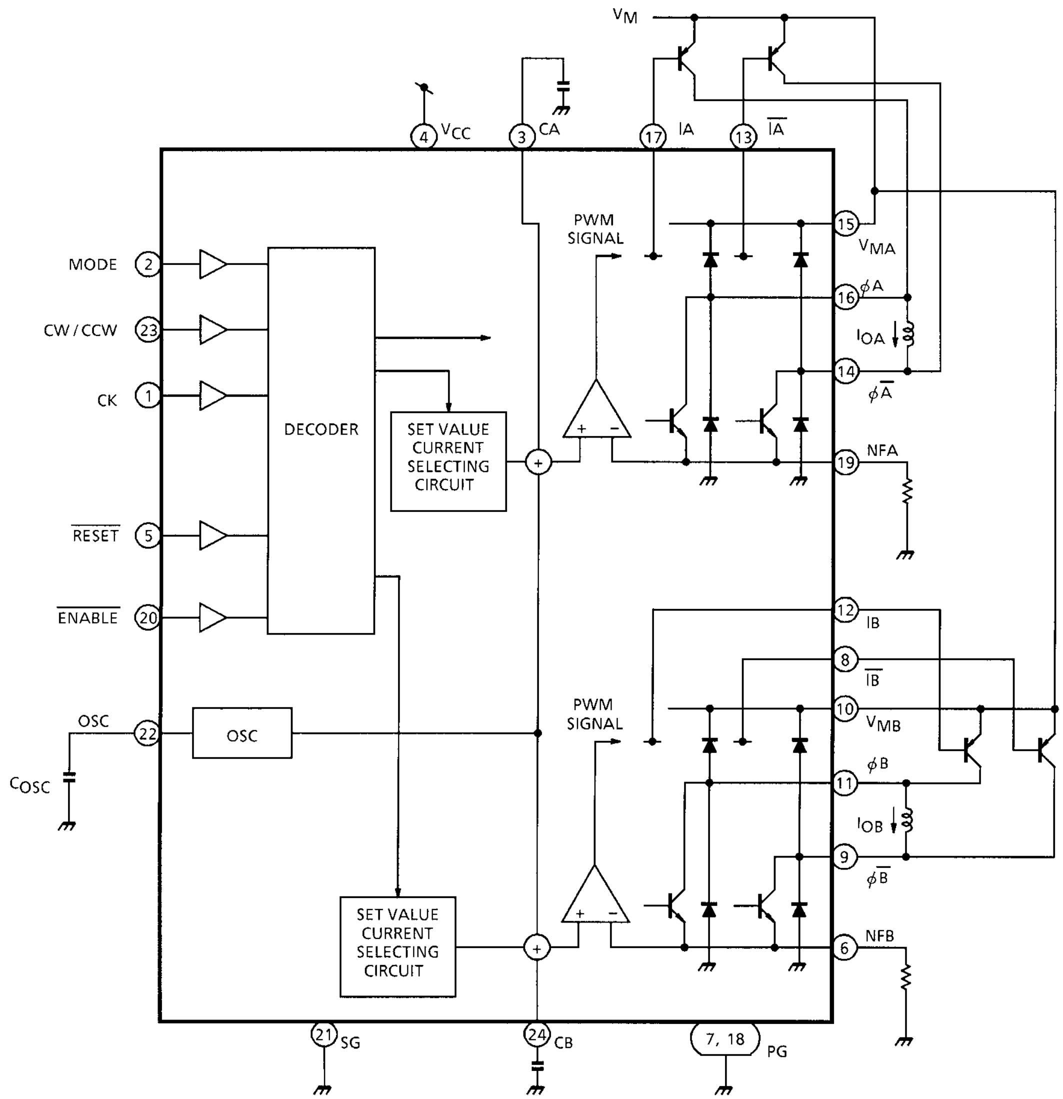
Weight: 0.27 g (Typ.)

FEATURES

- Forward and reverse rotations are available.
- 1−2, 2W1−2 phase driving is available.
- Structured by Bi−CMOS process.
- Package: SSOP24−P−300−1.00B
- Externally equipped with PNP output transistor.
- Reset and enable pins are attached.

TB6526AFG:
The TB6526AFG is a Pb-free product.
The following conditions apply to solderability:
*Solderability
1. Use of Sn-37Pb solder bath
   *solder bath temperature = 230°C
   *dipping time = 5 seconds
   *number of times = once
   *use of R-type flux
2. Use of Sn-3.0Ag-0.5Cu solder bath
   *solder bath temperature = 245°C
   *dipping time = 5 seconds
   *the number of times = once
   *use of R-type flux

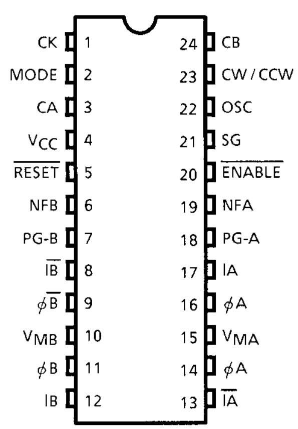
BLOCK DIAGRAM



PIN FUNCTION

PIN No.	SYMBOL	FUNCTIONAL DESCRIPTION
1	CK	CLOCK Signal Input Truth table A
2	MODE	Excitation Mode Setting terminal Truth table B
3	CA	Noise reduction condenser outer terminal
4	V_{CC}	Power voltage supply terminal for Logic
5	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ Signal Input terminal Truth table A
6	NFB	B Channel current detective terminal
7	PG−B	Power GND B terminal
8	$I\overline{B}$	Upper PNP Transistor Base terminal ($\overline{B}$ phase)
9	$\varphi\overline{B}$	$\overline{B}$ output
10	V_{MB}	Power voltage supply terminal for Motor B
11	φB	Output B terminal
12	IB	Upper PNP Transistor Base terminal (B phase)
13	$I\overline{A}$	Upper PNP Transistor Base terminal ($\overline{A}$ phase)
14	$\varphi\overline{A}$	Output $\overline{A}$ terminal
15	V_{MA}	Power voltage supply terminal for Motor A
16	φA	Output A terminal
17	IA	Upper side PNP transistor Base terminal (A phase)
18	PG−A	Power GND A terminal
19	NFA	A Channel current detection terminal
20	$\overline{\text{ENABLE}}$	$\overline{\text{ENABLE}}$ Signal input terminal Truth table A
21	SG	Signal GND terminal
22	OSC	Internal Oscillation frequency detective terminal with external condenser
23	CW / CCW	Forward rotation / Reverse rotation signal input Truth table A
24	CB	Noise reduction condenser outside terminal

PIN CONNECTION



TRUTH TABLE A

INPUT				MODE
CK1	CW / CCW	$\overline{\text{RESET}}$	$\overline{\text{ENABLE}}$	
↑	L	H	L	CW
↑	H	H	L	CCW
X	X	L	L	INITIAL MODE
X	X	X	H	Z

Z : High impedance
X : Don't care
Note: Do not use INHIBIT mode.

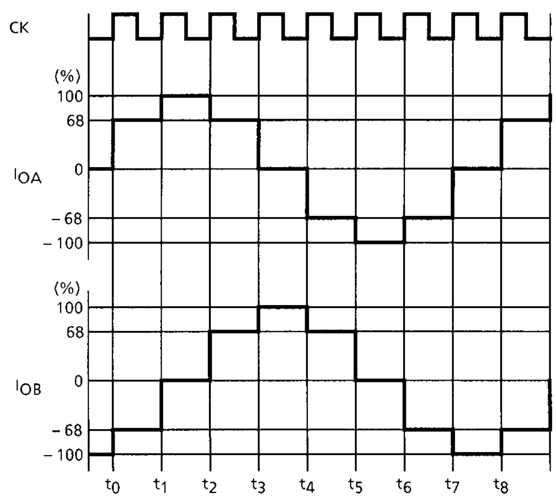
TRUTH TABLE B

INPUT MODE	MODE (EXCITATION)
L	1−2 phase
H	2W1−2 phase

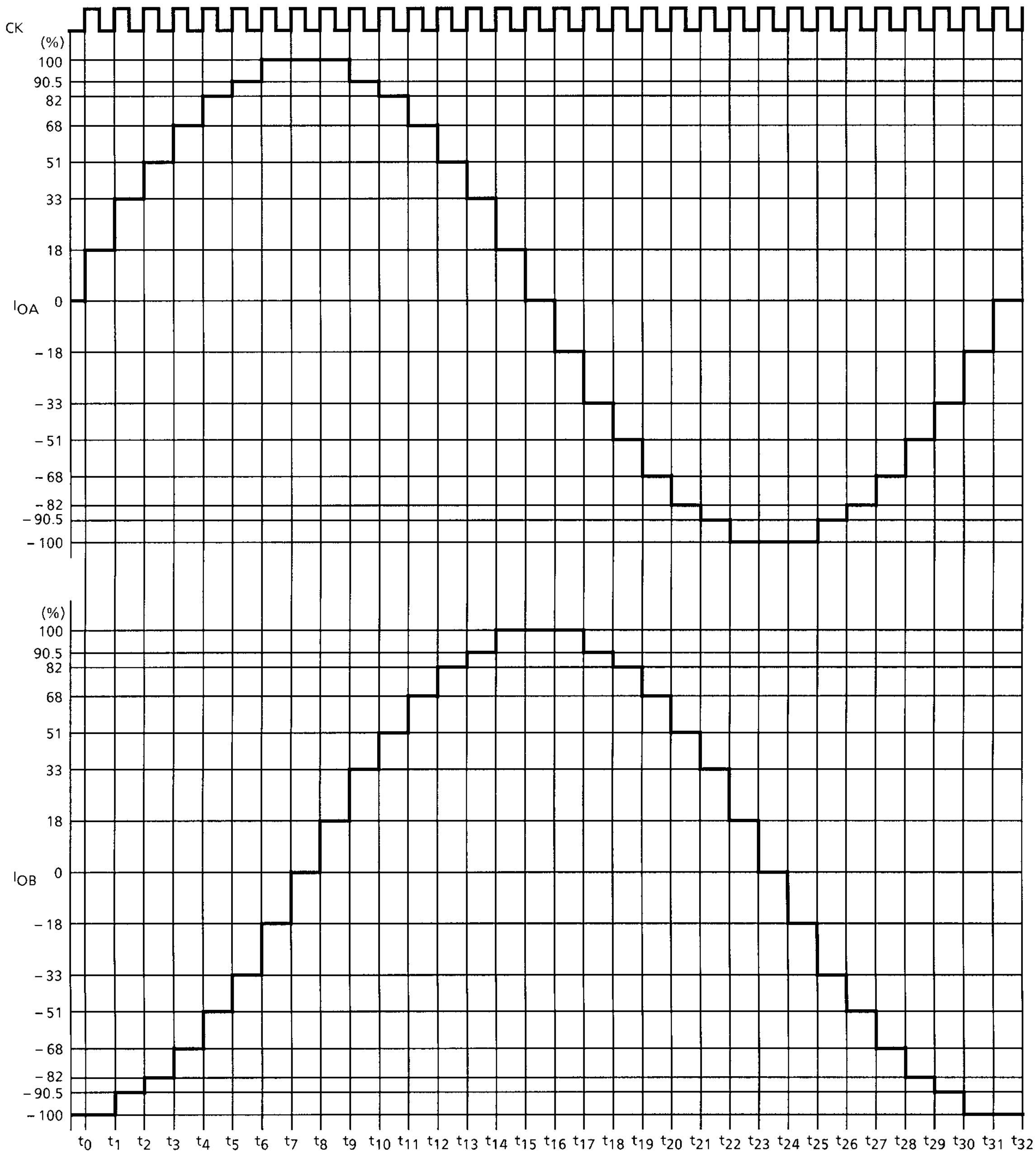
INITIAL MODE

MODE EXCITATION	A−PHASE CURRENT	B−PHASE CURRENT
1−2 phase	100%	0%
2W1−2 phase	100%	0%

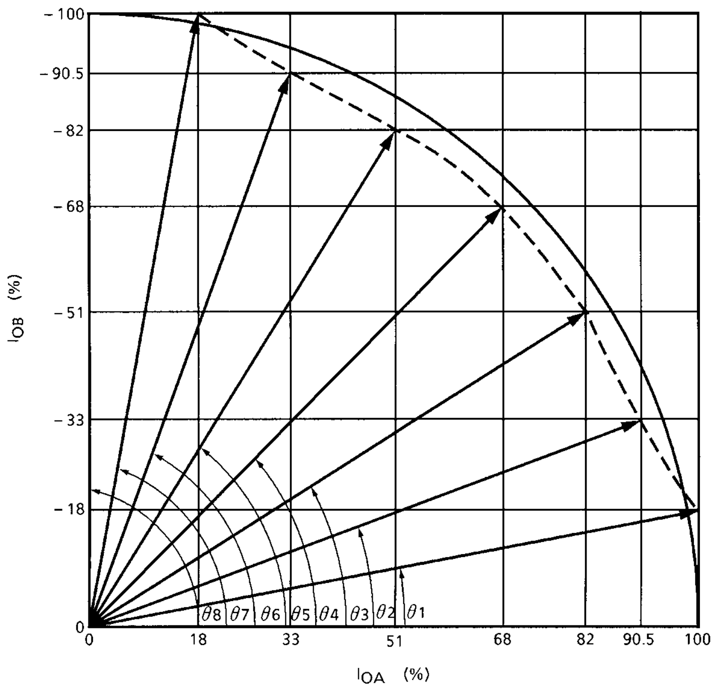
1−2 PHASE EXCITATION (MODE : L, CW mode)



2W1−2 EXCITATION (MODE : H, CW mode)

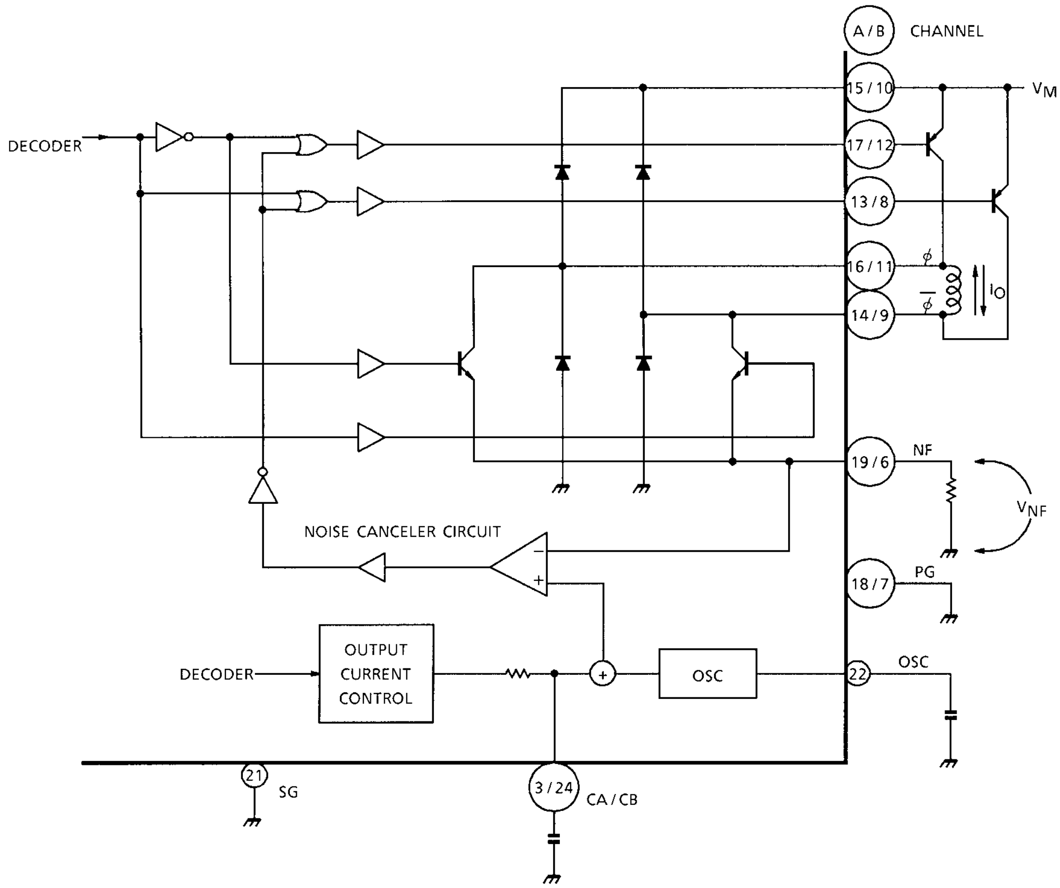


OUTPUT CURRENT VECTOR OR BIT (Normalize to 90 deg for each one step)



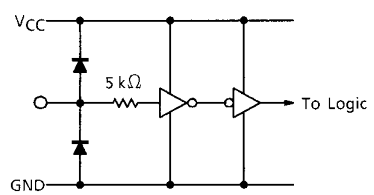
θ	ROTATION ANGLE		VECTOR LENGTH	
	IDEAL	TB6526AF/AFG	IDEAL	TB6526AF/AFG
θ0	0°	0°	100	100.00
θ1	11.25°	10.20°	100	101.65
θ2	22.5°	20.03°	100	96.35
θ3	33.75°	31.88°	100	96.56
θ4	45°	45°	100	96.17
θ5	56.25°	58.12°	100	96.57
θ6	67.5°	69.97°	100	96.33
θ7	78.75°	79.80°	100	101.61
θ8	90°	90°	100	100.00
			1−2 / 2W1−2, Phase	

OUTPUT CIRCUIT

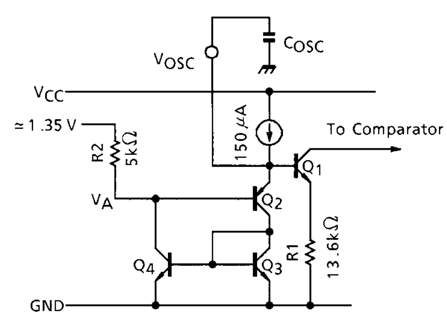


INPUT CIRCUIT

CK,CW / CCW, $\overline{\text{RESET}}$, $\overline{\text{ENABLE}}$, MODE Terminals



OSC : Terminals



- OSC frequency calculation

  V_{OSC} is increased by C_{OSC} charging through the constant current source (150 μA).
  V_{OSC} is calculated by following equation.

$$V_{OSC} = \frac{150 \times 10^{-6} \times t}{C_{OSC}}$$

Q_2 is turned "off" when V_{OSC} is less than the voltage of 1.35 V + V_{BE} (Q_2) approximately equal to 2.05 V.
Q3 and Q4 are turned "on" when V_{OSC} becomes 2.05 V.

$$V_{OSC\,(H)} = V_{BE\,(Q2)} + 1.35 \approx 2.05\ \text{V}$$

Lower level of V (22) pin is equal to V_{BE} (Q_2) + $V_{CE\,(SAT)}$ (Q_4) approximately equal to 1.0 V.

$$V_{OSC\,(L)} = V_{BE\,(Q2)} + V_{CE\,(SAT)}\,(Q_4) \approx 1.0\ \text{V}$$

Assuming that V_{OSC} = 1.0 V (t = t_1) and = 2.05 V (t = t_2), OSC frequency is calculated as follows.

$$t_1 = \frac{1.0 \times C_{OSC}}{150 \times 10^{-6}}$$

$$t_2 = \frac{2.05 \times C_{OSC}}{150 \times 10^{-6}}$$

$$f_{OSC} = \frac{1}{t_2 - t_1} = \frac{150 \times 10^{-6}}{C_{OSC}\ (2.05 - 1.0)}$$

$$= \frac{0.143}{C_{OSC}}\ (\text{kHz})\ \ (C_{OSC}\ \text{unit} = \mu\text{F})$$

$\overline{\text{ENABLE}}$ AND $\overline{\text{RESET}}$ FUNCTION AND $\overline{\text{MO}}$ SIGNAL

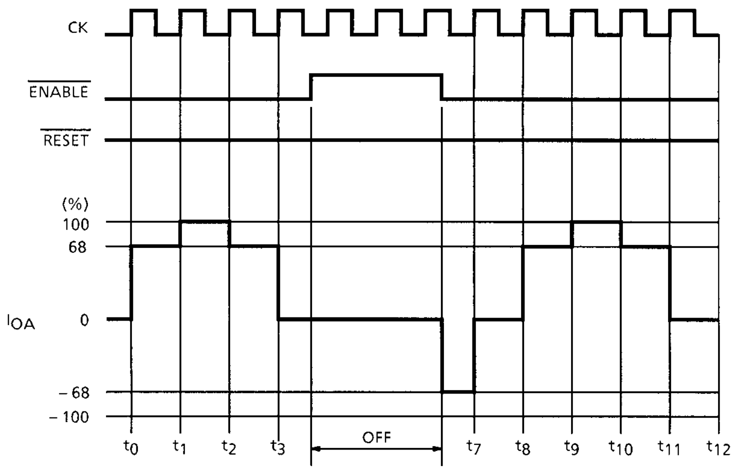


Fig.1. 1−2 phase drive mode (MODE : L)

$\overline{\text{ENABLE}}$ signal disables only Output signal. Internal logic functions are proceeded by CK signal without regard to $\overline{\text{ENABLE}}$ signal.
Therefore, Output Current is initiated from the proceeded timing point of internal logic circuit, after release of disable mode.
Fig.1 shows the $\overline{\text{ENABLE}}$ functions, when the system is selected in 1−2 phase drive mode.

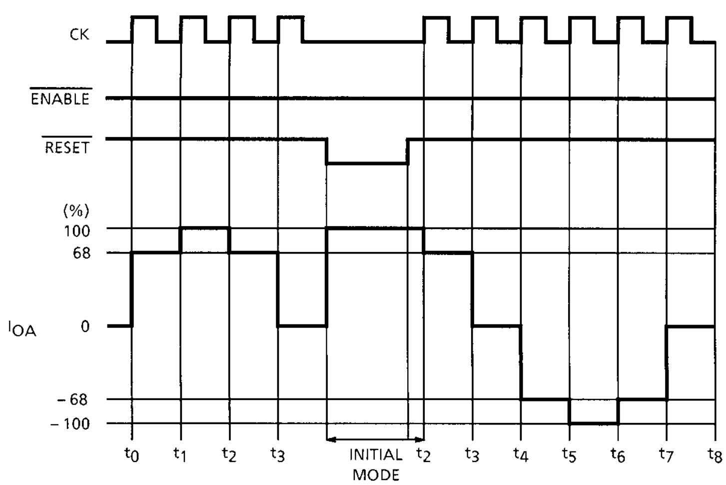


Fig.2. 1−2 phase drive mode (MODE : L)

As $\overline{\text{RESET}}$ is low, the decoder is initialized. (Output Current : A−Phase 100%, B−Phase 0%)
After $\overline{\text{RESET}}$ is high, the motion is resumed from next clock as show in Fig.2.
$\overline{\text{MO}}$ (Monitor Output) signals is used as rotation and initial signal for stable.
rotation checking.

ABSOLUTE MAXIMUM RATING (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	5.5	V
Output Voltage	$V_{M\ (opr.)}$	3.5~8.0	V
	$V_{M\ (MAX.)}$	10.0	
Output Current	$I_{O\ (MAX.)}$	120	mA
Input Voltage	V_{IN}	~V_{CC} + 0.5	V
Power Dissipation	P_D	0.83 (Note 1)	W
		1.04 (Note 2)	
Operating Temperature	T_{opr}	−30~85	°C
Storage Temperature	T_{stg}	−55~150	°C
Feed Back Voltage	V_I	1.0	V

Note 1: No heat sink
Note 2: When mounted on substrate (50 × 50 × 1.6 mm Cu 10%)

RECOMMENDED OPERATING CONDITIONS (Ta = −30~85°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Control Power Supply Voltage	$V_{CC\ (opr.)}$		2.7	3.0	5.5	V
Motor Power Supply Voltage	$V_{M\ (opr.)}$		3.5	—	8.0	V
Output Current	I_{OUT}		—	—	100	mA
Input Voltage	V_{IN}		−0.4	—	V_{CC} + 0.4	V
Clock Frequency	f_{CLOCK}		—	—	5	kHz
OSC Frequency	f_{OSC}		15	—	80	kHz

ELECTRICAL CHARACTERISTICS

Unless otherwise specified (Ta = 25°C, V_{CC} = 3 V, V_M = 5 V, load inductance : L = 8 mH / R = 50 Ω, with outer PNP)

CHARACTERISTIC		SYMBOL	TEST CIR−CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Input Voltage	High	$V_{IN (H)}$	1	MODE, CW / CCW, $\overline{ENABLE}$ CK, $\overline{RESET}$	V_{CC} × 0.7	—	V_{CC} + 0.4	V
	Low	$V_{IN (L)}$			GND − 0.4	—	V_{CC} × 0.3	
Input Current		$I_{IN (H)}$	2	V_{IN} = 3.0 V	—	—	100	nA
		$I_{IN (L)}$		V_{IN} = 0 V	—	—	100	
Current Consumption V_{CC} Pin		I_{CC1}	3	Output open, $\overline{RESET}$: H, $\overline{ENABLE}$: L, (1−2 phase excitation)	—	7	9	mA
		I_{CC2}		Output open, $\overline{RESET}$: H, $\overline{ENABLE}$: L, (2W1−2 phase excitation)	—	7	9	
		I_{CC3}		$\overline{RESET}$: L, $\overline{ENABLE}$: H	—	1.3	—	
		I_{CC4}		$\overline{RESET}$: H, $\overline{ENABLE}$: H	—	1.3	—	
Comparator Reference Voltage Level		V_{NF1}	9	C_A, C_B	0.245	0.275	0.305	V
		V_{NF2}	4	R_{NF} = 3.3 Ω, C_{OSC} = 3300 pF	175	195	220	mV
		V_{NF3}	4	R_{NF} = 2.2 Ω, C_{OSC} = 3300 pF	150	172	190	mV
Output Inter−channel Differential		ΔV_O	4	$(V_{NFA}-V_{NFB}) / V_{NFA}$, C_{OSC} = 3300 pF, R_{NF} = 3.3 Ω	−10	—	10	%
Maximum OSC Frequency		$f_{OSC (MAX.)}$	—		100	—	—	kHz
Minimum OSC Frequency		$f_{OSC (MIN.)}$	—		—	—	10	kHz
OSC Frequency		f_{OSC}	5	C_{OSC} = 3300 pF	31	44	70	kHz

ELECTRICAL CHARACTERISTICS

Unless otherwise specified (Ta = 25°C, V_{CC} = 3 V, V_M = 5 V, load inductance : L = 8 mH / R = 50 Ω, with outer PNP)

OUTPUT SECTION

CHARACTERISTIC			SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN	TYP.	MAX	UNIT
Upper Side Driving Current			I_U	6	V_C = 3 V		—	1.5	1.6	mA
Lower Side Saturation Voltage			$V_{SAT\ L1}$	7	I_{OUT} = 0.06 A		—	0.10	—	V
			$V_{SAT\ L2}$		I_{OUT} = 0.12 A		—	0.16	0.43	
Diode Forward Voltage	Upper Side		$V_{F\ U}$	8	I_{OUT} = 0.12 A		—	1.24	1.8	V
	Lower Side		$V_{F\ L}$				—	0.95	1.6	
Output Dark Current (A + B channel)			I_{M1}	3	$\overline{\text{ENABLE}}$: "H" level RESET : "L" level Output open		—	—	50	μA
			I_{M2}		$\overline{\text{ENABLE}}$: "L" level RESET : "H" level Output open		—	17	28	mA
NF Dark Current (1 channel)			I_{NF}		$\overline{\text{ENABLE}}$: "L" level RESET : "H" level Output open		1	2.5	7	
A−B Chop− per Current (Note)	2W1−2 phase excitation	1−2 phase excitation	Vector	4	θ = 0	R_{NF} = 3.3 Ω C_{OSC} = 3300 pF V_{NF}	—	100	—	
	2W1−2 phase excitation	—			θ = 1 / 8		—	100	—	
	2W1−2 phase excitation	—			θ = 2 / 8		85.5	90.5	95.5	
	2W1−2 phase excitation	—			θ = 3 / 8		77	82	87	
	2W1−2 phase excitation	1−2 phase excitation			θ = 4 / 8		64	69	74	
	2W1−2 phase excitation	—			θ = 5 / 8		48	53	58	
	2W1−2 phase excitation	—			θ = 6 / 8		31	36	41	
	2W1−2 phase excitation	—			θ = 7 / 8		16	21	26	

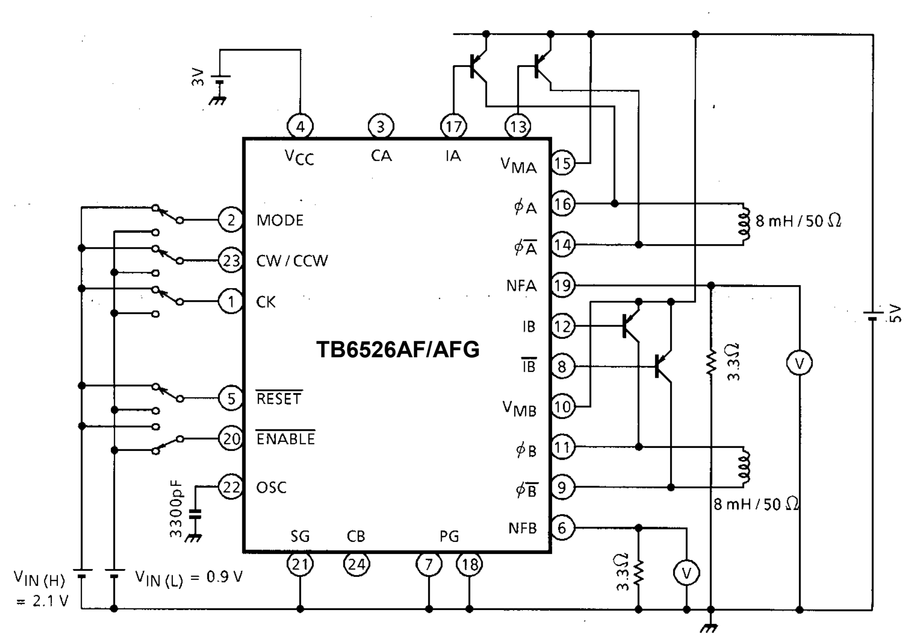
Note: Maximum current θ = 0 is set at 100.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified (Ta = 25°C, V_{CC} = 3 V, V_M = 5 V, load inductance : L = 8 mH / R = 50 Ω, with outer PNP)

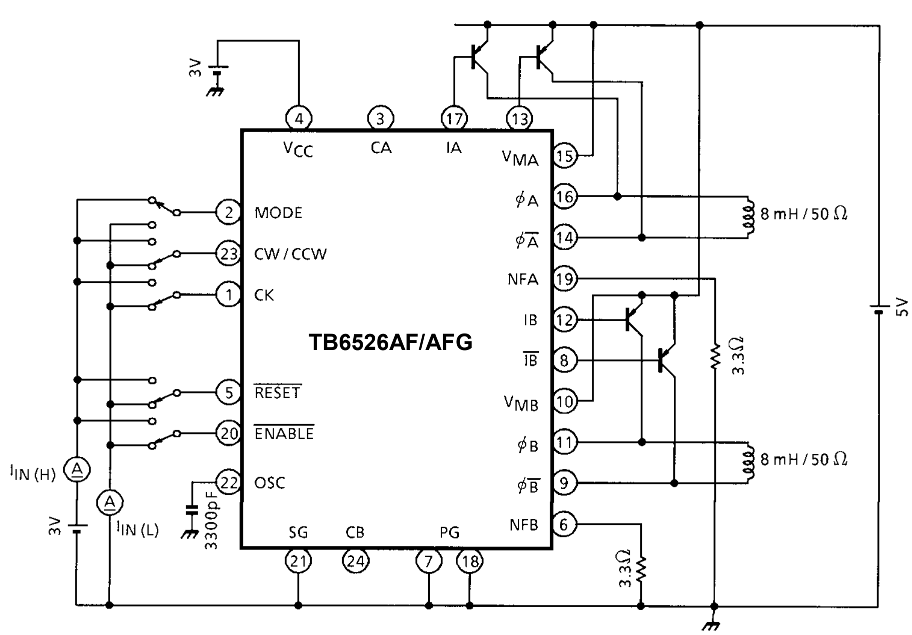
CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN	TYP.	MAX	UNIT
Reference Voltage	ΔV_{NF}	9	Δθ = 0 / 8−1 / 8	Measured by CA and CB	—	0	—	mV
			Δθ = 1 / 8−2 / 8		10	17	35	
			Δθ = 2 / 8−3 / 8		5	16	30	
			Δθ = 3 / 8−4 / 8		16.25	21	41.25	
			Δθ = 4 / 8−5 / 8		25	32	50	
			Δθ = 5 / 8−6 / 8		26.25	31	51.25	
			Δθ = 6 / 8−7 / 8		15	28	45	
Output Tr Switching	t_r	12	R_L = 2 Ω, V_{NF} = 0 V, C_L = 15 pF		—	0.3	—	μs
	t_f				—	2.2	—	
	t_{pLH}		CK~output		—	1.5	—	
	t_{pHL}				—	2.7	—	
	t_{pLH}		OSC~output		—	5.4	—	
	t_{pHL}				—	6.3	—	
	t_{pLH}		$\overline{\text{RESET}}$ ~ output		—	2.0	—	
	t_{pHL}				—	2.5	—	
	t_{pLH}		$\overline{\text{ENABLE}}$ ~ output		—	5.0	—	
	t_{pHL}				—	6.0	—	
Output Leakage Current	I_{OL}	10	V_M = 10 V		—	—	50	μA
V_{MA} / V_{MB} Off Current	I_{off}	11	V_{CC} = 0, V_M = 5 V		—	—	1	μA

TEST CIRCUIT 1 : $V_{IN\ (H)}$, $V_{IN\ (L)}$

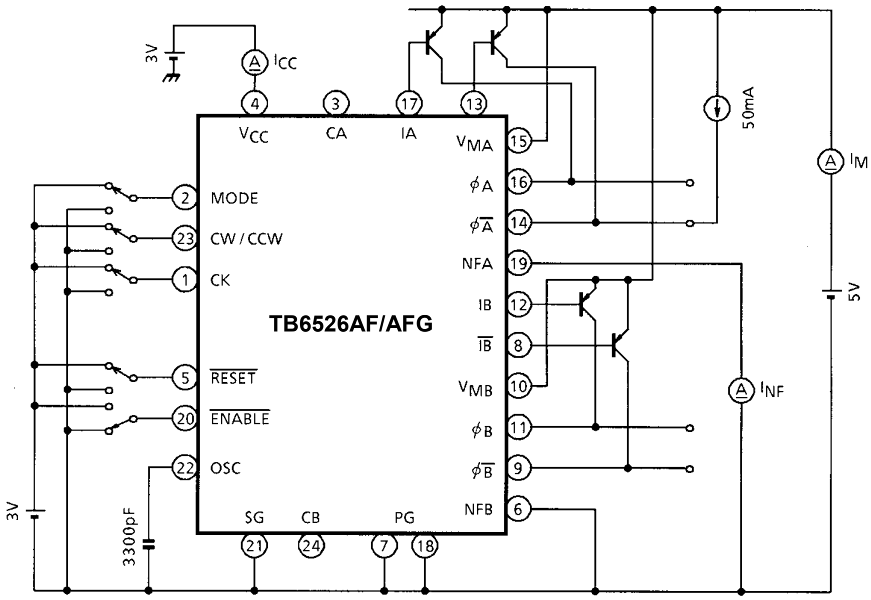


Note: When input voltage $V_{IN\ (H)}$, $V_{IN\ (L)}$ is applied, verify the output function (NF voltage measurement).

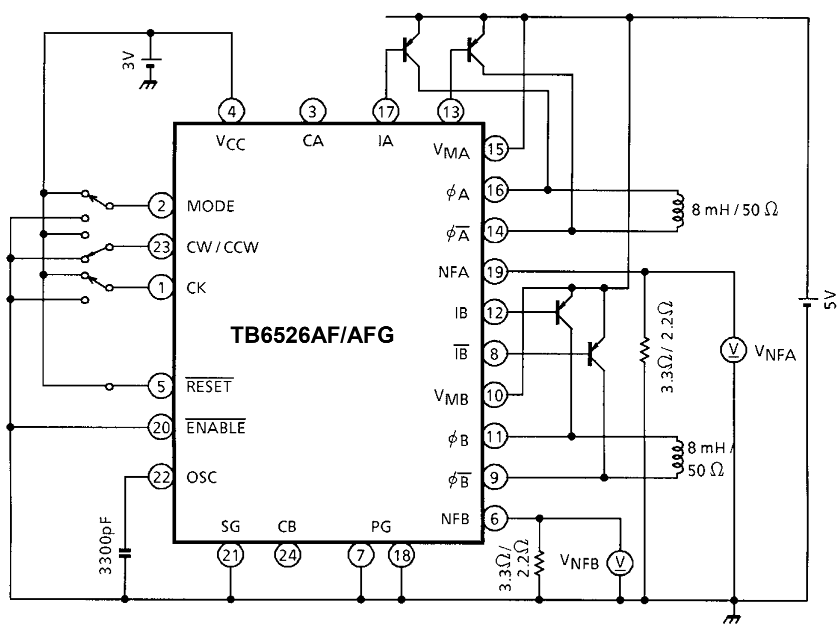
TEST CIRCUIT 2 : $I_{IN\ (H)}$, $I_{IN\ (L)}$



TEST CIRCUIT 3 : I_{CC}, I_M, I_{NF}

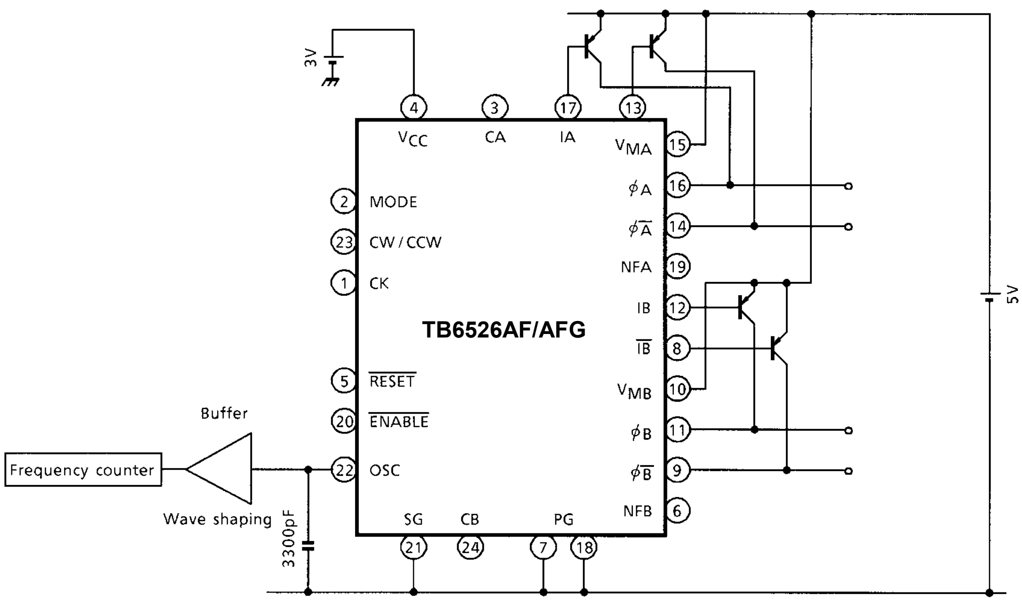


TEST CIRCUIT 4 : V_{NF2}, V_{NF3}, ΔV_O

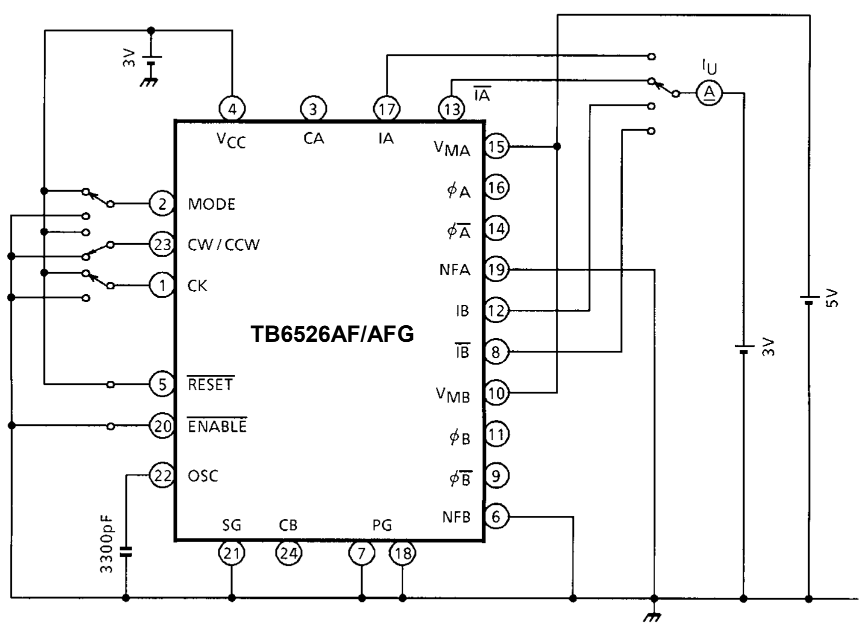


Note: V_{NF2} : V_{NFA} (100%), V_{NFB} (100%) when R_{NF} = 3.3 Ω
V_{NF3} : V_{NFA} (100%), V_{NFB} (100%) when R_{NF} = 2.2 Ω

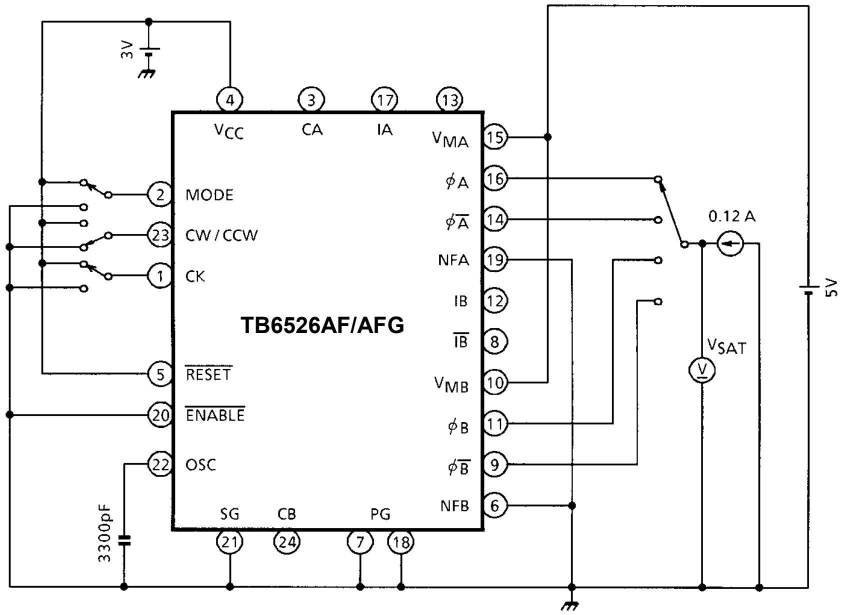
TEST CIRCUIT 5 : f_{OSC}



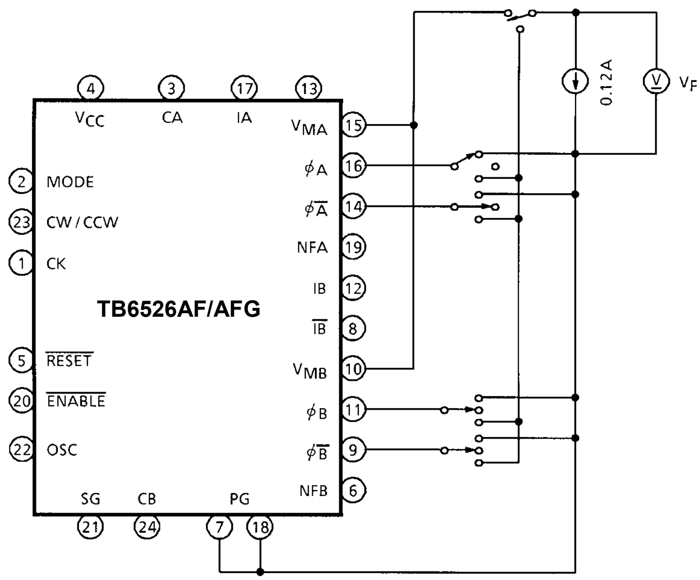
TEST CIRCUIT 6 : I_U



TEST CIRCUIT 7 : V_{SAT}

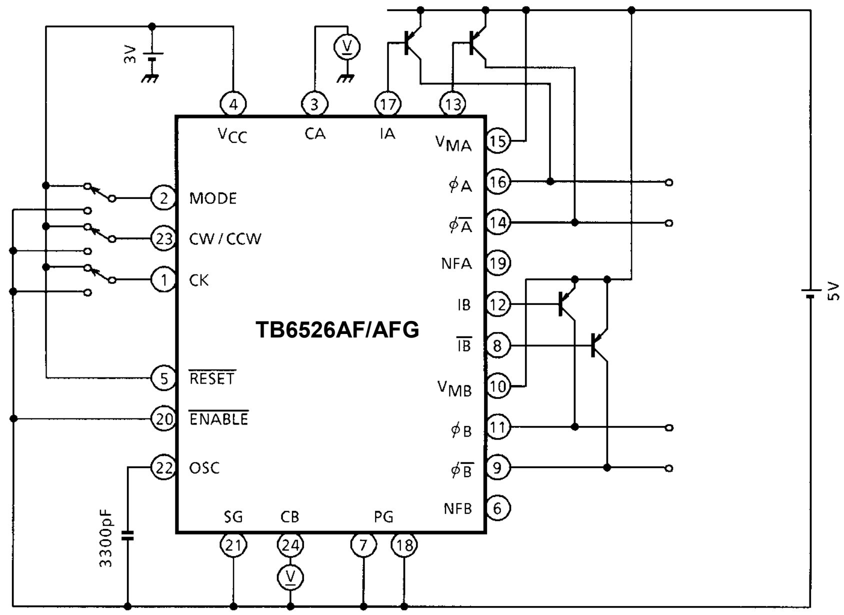


TEST CIRCUIT 8 : V_{F-U}, V_{F-L}

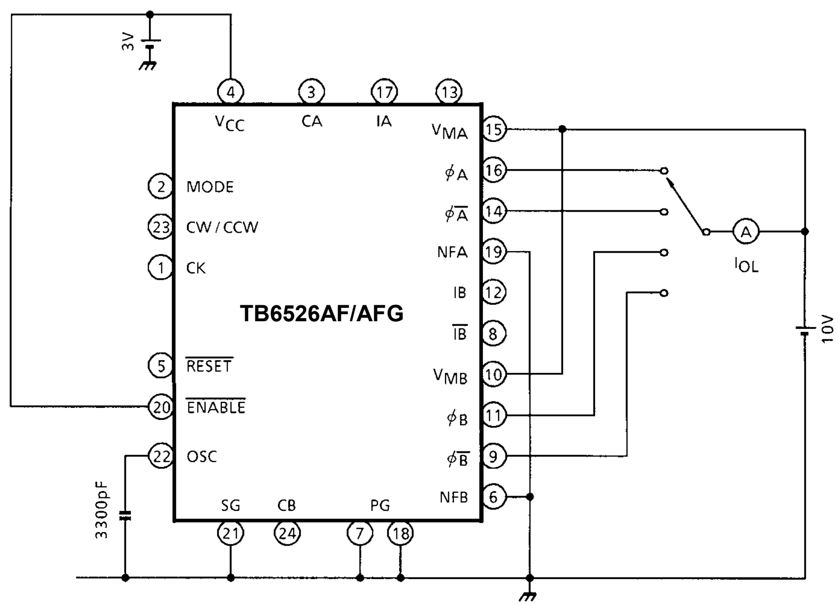


Note: Not to take GND with any non−connecting pins.

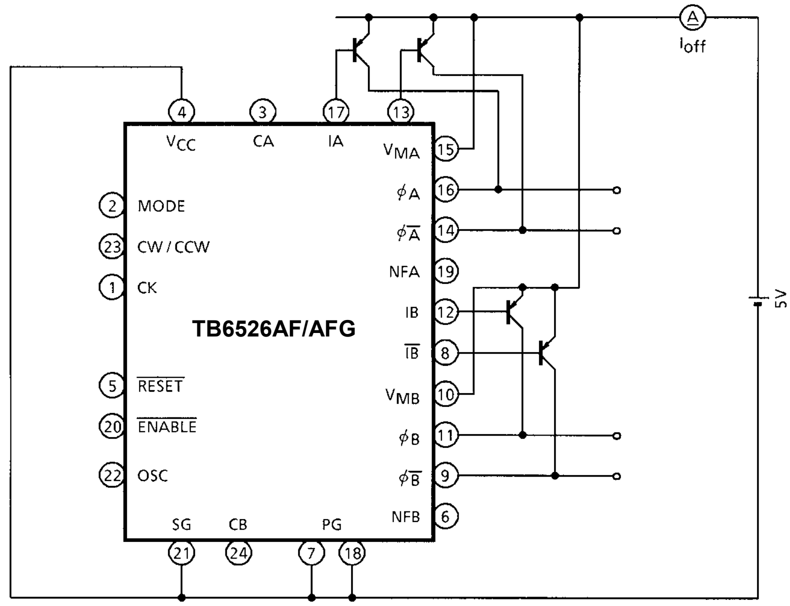
TEST CIRCUIT 9 : V_{NF1}, ΔV_{NF}



TEST CIRCUIT 10 : I_{OL}

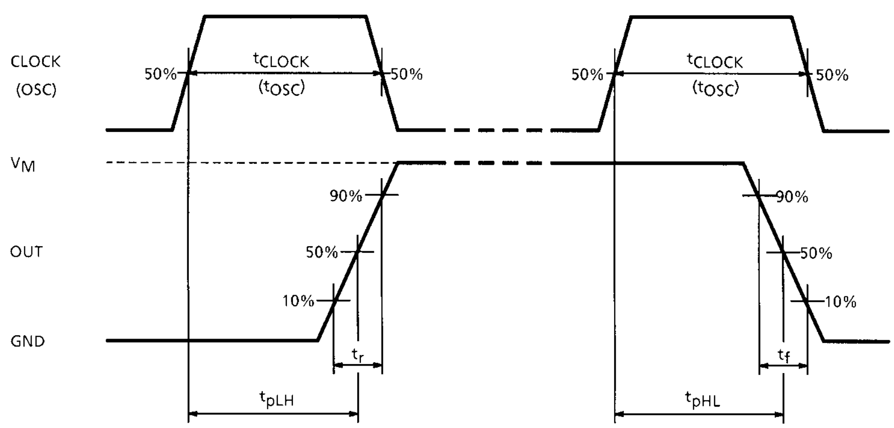


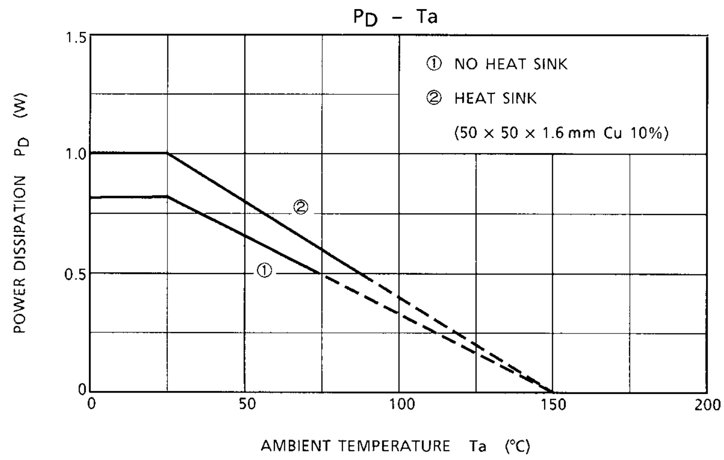
TEST CIRCUIT 11



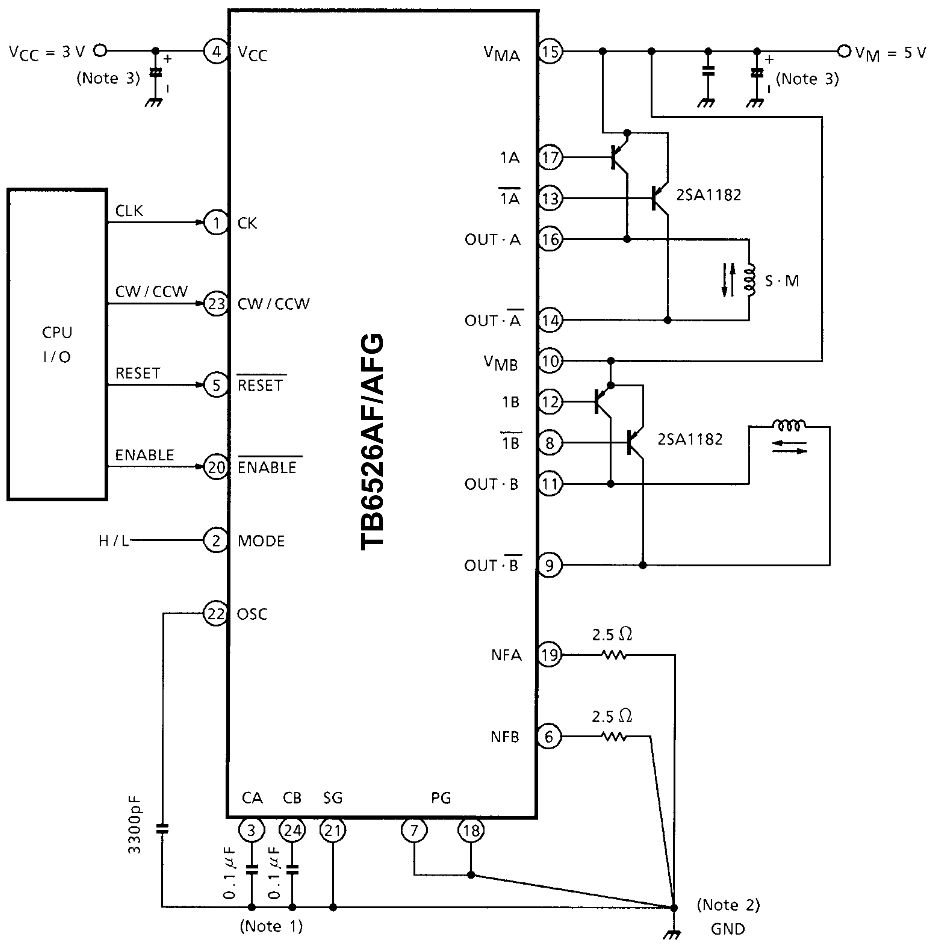
AC ELECTRICAL CHARACTERISTICS, TEST CIRCUIT 12 CK (OSC) − OUT

CK (OSC) − OUT




PD – Ta
① NO HEAT SINK
② HEAT SINK
(50 × 50 × 1.6 mm Cu 10%)
POWER DISSIPATION PD (W)
AMBIENT TEMPERATURE Ta (°C)
1.5
1.0
0.5
0
0
50
100
150
200
②
①

APPLICATION CIRCUIT



Note 1: A change in a step at the time of the micro−step can be improved smoothly with the capacitor of CA, CB.

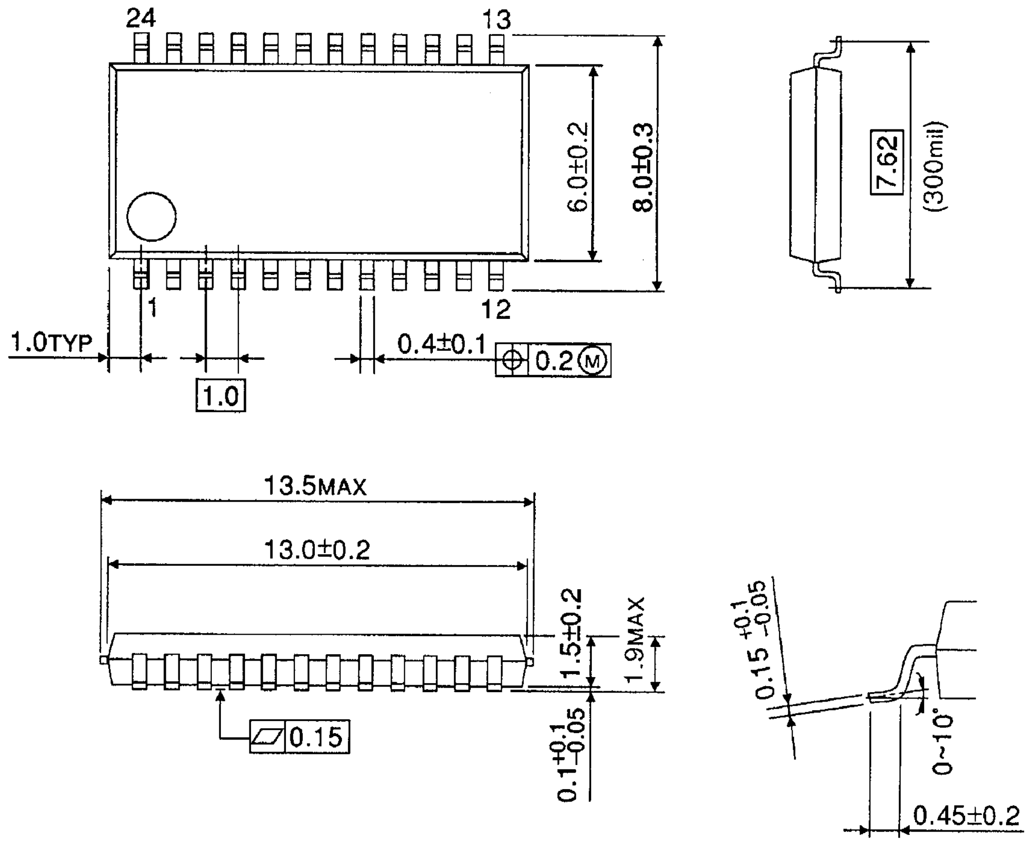
Note 2: GND pattern to be laid out at one point in order to prevent common impedance.

Note 3: Capacitor for noise suppression to be connected between the Power Supply (V_{CC}, V_M) and GND to stabilize the operation.

Note 4: Utmost care is necessary in the design of the output, V_{CC}, V_M, and GND lines since the IC may be destroyed by short-circuiting between outputs, air contamination faults, or faults due to improper grounding, or by short-circuiting between contiguous pins.

PACKAGE DIMENSIONS

SSOP24−P−300−1.00B Unit: mm



Weight: 0.27 g (Typ.)

Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.
Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on handling of ICs

[1] The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

[2] Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

[3] If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

[4] Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

Points to remember on handling of ICs

(1) Heat Radiation Design

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_J) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(2) Back-EMF

When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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