# rohm

STRUCTURE	Silicon Monolithic Integrated Circuit			
PRODUCT SERIES	Three-Phase Full-Wave Driver for Fan Motor			
TYPE	BD6331FM			
FEATURES	PWM operating Output DMOS driving system DC and PWM speed control Lock detection, Automatic restart circuit			

# ○ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

Parameter	Symbol	Limit	Unit	
Supply voltage	VCC, VM	20	٧	
Output current	I oMAX	*2500	mA	
Power dissipation	Pd	**2200	mW	
Junction temperature	TJMAX	150	°C	
Operating temperature	Topr	-20~+75	°C	
Storage temperature	Tstg	-55~+150	°C	
SOUT voltage	VSOUT	20	٧	
SOUT current	I SOUT	10	mA	
VREG output current	I VREG	10	mA	

\*This value is not to exceed Pd, ASO and Tj=150°C.

\*\*On 70mmX70mmX1.6mmglass epoxy board.

\*\*Reduce by 17.6mW/°C over Ta=25°C.

# OPERATING CONDITIONS (Ta=25°C)

Parameter	Symbo I	Limit	Unit
Operating supply voltage range	VCC, VM	8.0~18.0	V
Hall input voltage range	VHAR	1.4~VREG	V
VTH input voltage range	VTH	0~VREG	V
VMIN input voltage range	VMIN	0~VREG	V

 $\ast \mbox{This product is not designed for production against radioactive rays.}$ 

 $\ast {\rm This}$  document may be strategic data subject to COCOM regulations.

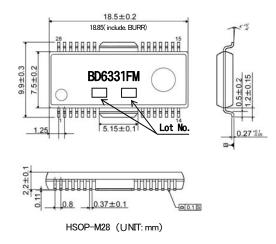
# ROHM

OELECTRICAL CHARACTERISTICS (Unless otherwise specified Ta=25°C, VCC=VM=12V)

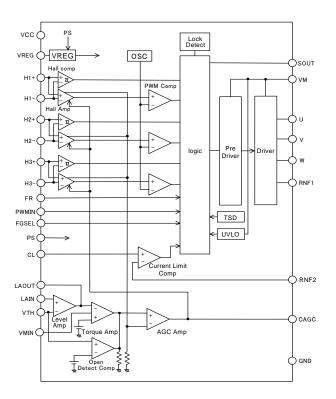
OELECTRICAL CHARACTERISTICS		erwise spec			20)	
Parameter	Symbol			Unit	Conditions	
	1001	Min.	Тур.	Max.		
Circuit current 1	1001	0	-	10	μA	VCC+VM, PS=0V
Circuit current 2	1CC2	4	6	10	mA	VCC+VM
【HALL Amp.】						
Input bias current	IB	-10	-	10	μA	
Input level	VINH	50	-	100	mVpp	
[VREG]						
VREG voltage	VREG	2.7	2.8	2.9	V	lo=-5mA
(FR)						
[L] level voltage range	VFRL	0	-	0.7	V	
[H] level voltage range	VFRH	2.1	-	2.8	V	
Input current	IFRI	22	28	35	μA	FR=2.8V
Output current	IFR0	0	-	10	μA	FR=0V
[FGSEL]						
[L] level voltage range	VSELL	0	-	0.7	V	
[H] level voltage range	VSELH	2.1	—	2.8	V	
Input current	ISELI	22	28	35	μA	FGSEL=2.8V
Output current	I SELO	0	_	10	μA	FGSEL=0V
(VTH)						
Input bias current	IVTH	-1	-	1	μA	VTH=0V, LAIN=2.8V
Open detect voltage	VDET	90	93	96	%	VTH/VREG
[PS]						
[L] level voltage range	PSL	0	_	1.3	V	
[H] level voltage range	PSH	2.3	_	12	v	
Input current	IPSI	18	24	30	μA	PS=12V
Output current	IPS0	0	_	10	μA	PS=0V
[Level Amp.]	11 00	Ū		10	μn	
Input bias current	ILA	-1	_	1	μA	LAIN=0V, VTH=2.8V
Output voltage L	VLAOL	0	_	0.3	μr V	VTH=0V
Output voltage H	VLAOH	2.79	2.8	2.81	v	VTH=2.8V
Output Tr. ON voltage range	VLAL	0	-	51.6	%	VTH/VREG
Output Tr. OFF voltage range	VLAL	57.4	_	89	%	VTH/VREG
PWM DUTY1	DPWM1	64	79	94	%	VTH=0.464×VREG
PWM DUTY2	DPWM2	42	57	72	%	VTH=0.5×VREG
PWM FREQUENCY	FPWM	30	50	80	∕₀ KHz	
	I I WIWI	50	50	00	IN 12	
Input bias current	IMIN	-1	_	1		VMIN=0V
	I IVI I IN	-1	_	I	μA	VMIIN-OV
		0		0.7	N	
[L] level voltage range	VPWML	0	_	0.7	V V	
[H] level voltage range	VPWMH	2.1		2.8		
Input current		-1		1	μΑ	PWMIN=2.8V
Output current		22	28	35		PWMIN =0V
Input frequency	FPWMIN	25	50	75	KHz	1
[Current limit]		1		1		
Input bias current	ICL	-1	-	1	μA	CL=0V, RNF2=2.8V
Current limit gain	VCL	0.98	1.0	1.02	V	RNF2=0.2V
[Output]	-	• -			-	
ON resistance	RON	0.7	1	1.3	Ω	lo=±600mA (Upper+Lower)
[SOUT]	ļ		ļ		ļ	
Leak current	IFG	0		10	μA	
Output voltage L	VFGL	0	-	0.3	V	lo=5mA
[Lock detection]						
ON time	TON	0.65	1.3	2.6	sec	
OFF time	TOFF	5.25	10.5	21	sec	



# OPACKAGE OUTLINES



# OBLOCK DIAGRAM



# $\bigcirc \mathsf{TERMINAL}$ NAME

PIN No.	Terminal name			
1	V			
2	W			
3	RNF2			
4	FR			
5	FGSEL			
6	VM			
7	GND			
8	VCC			
9	VREG			
10	CL			
11	CAGC			
12	H1+			
13	H1-			
14	H2+			
15	H2-			
16	H3+			
17	H3-			
18	VMIN			
19	VTH			
20	LAOUT			
21	LAIN			
22	PWMIN			
23	SOUT			
24	PS			
25	RNF			
26	N.C.			
27	N.C.			
28	U			



# CAUTION ON USE

## 1) Absolute maximum ratings

There is possibility of destruction in using beyond the absolute maximum rating. In case of destruction, a failure mode can not be defined (short mode or open mode). Therefore when special mode is envisaged where absolute maximum rating may be exceeded, please take a physical safety measure such as fuse.

## 2) Reverse connection of power supply connector

Reverse connection of power supply connector may break IC. Take a measure against reverse connection destruction such as inserting a diode between power supply and Vcc terminal.

## 3) Power supply line

Back electromotive force causes regenerated current to power supply line, therefore take a measure such as placing a capacitor between power supply and GND for routing regenerated current, and fully ensure that the capacitor characteristics have no problem before determine a capacitor value.

#### 4) GND potential

Ensure that the potential of GND terminal is the minimum potential in any operating condition. Also ensure that all terminals except GND terminal do not fall below GND voltage including transient characteristics. However, it is possible that the motor output terminal may deflect below GND because of influence by back electromotive force of motor. Malfunction may possibly occur depending on use condition, environment, and property of individual motor. Please make fully confirmation that no problem is found on operation of IC.

# 5) Thermal design

Consider the power dissipation under actual use condition and apply thermal design with sufficient margin.

# 6) Mounting failures

In attaching IC to printed board, pay enough attention to the direction and dislocation of IC. Mounting failures may break IC. In addition, destruction is also possible when circuit is shorted by foreign substance brought between outputs or between output and power supply - GND.

#### 7) Operation in strong electromagnetic field

Use in strong electromagnetic field may cause malfunction, please be careful.

#### 8) ASO

Please consider that the output Tr does not exceed the absolute maximum rating and ASO.

#### 9) Thermal shut down circuit

This IC has thermal shut down (TSD) circuit. Operation temperature is 175°C(typ.) and has a hysteresis width of 25°C(typ.). When IC chip temperature rises and TSD circuit works, the output terminal becomes an open state. TSD circuit is simply for the purpose of intercepting IC from overheating, and not for protecting and assuring IC. Therefore do not continue to use IC thereafter with this circuit operating and do not use IC assuming the operation of this circuit.

## 10) Inspection with a set board

When connecting a capacitor to a pin with low impedance in inspection on a set board, stress may possibly be applied to IC, therefore be sure to apply discharging in each process. In attaching to and detaching from jigs in inspection process, be sure to turn off power before connecting, and turn off power before removing IC. In addition, apply grounding to assembling process as a measure of anti-static electricity, and use full caution in transporting and storing.

#### 11) GND wiring pattern

When there are small signal GND and large current GND, separate the large current GND pattern from small signal GND pattern. It is recommended to apply one-point grounding at the reference point of the set in order that resistance of wiring pattern and large current do not cause change of voltage of small signal GND. Please be cautious not to fluctuate the wiring pattern of GND of external mounted parts.

## 12) IC terminal input

When Vcc voltage is not applied to IC, do not apply voltage to each input terminal. When voltage above Vcc or below GND is applied to the input terminal, parasitic element is actuated due to the structure of IC. Operation of parasitic element causes mutual interference between circuits, resulting in malfunction as well as destruction in the last. Do not use in a manner where parasitic element is actuated.

#### 13) Measure against VM voltage rise by back electromotive force

The re-circulate current might flow into the VM power supply for the PWM operation. Especially, please note it when rapidly changing it into a low torque at a high torque. In such case, please connect a zenner diode between VM and GND terminal, not to exceed the absolute maximum rating voltage.

14) FG output signal

Hall element may be affected by noise or the like depending on the wiring pattern of board. Especially, please note it when rapidly changing it into a low torque at a high torque. In this case, place a capacitor between the hall input terminals to decrease the noise of the hall signal, and increase the hall input level.

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Appendix1-Rev3.0