100mA CHARGE PUMP DC-TO-DC VOLTAGE CONVERTER

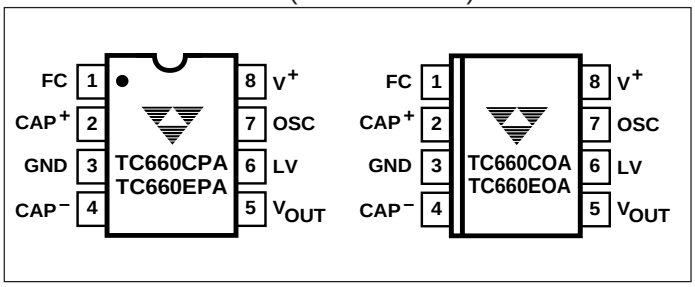
FEATURES

- **Pin Compatible with TC7660**
- **High Output Current 100mA**
- **Converts (+1.5V to 5.5V) to (– 1.5V to – 5.5V)**
- **Power Efficiency @100mA ..... 88% typ**
- **Low Power Consumption .....200μA @ 5 V_{IN}**
- **Low Cost and Easy to Use**
  — Only Two External Capacitors Required
- **Selectable Oscillator Frequency 10kHz/90kHz**
- **ESD Protection 4kV**

APPLICATIONS

- **Laptop Computers**
- **μP Based Controllers**
- **Process Instrumentation**
- **Automotive Instruments**

PIN CONFIGURATION (DIP and SOIC)



GENERAL DESCRIPTION

The TC660 DC-to-DC voltage converter generates a negative voltage supply, that can support a 100mA maximum load, from a positive voltage input of 1.5V to 5.5V. Only two external capacitors are required.

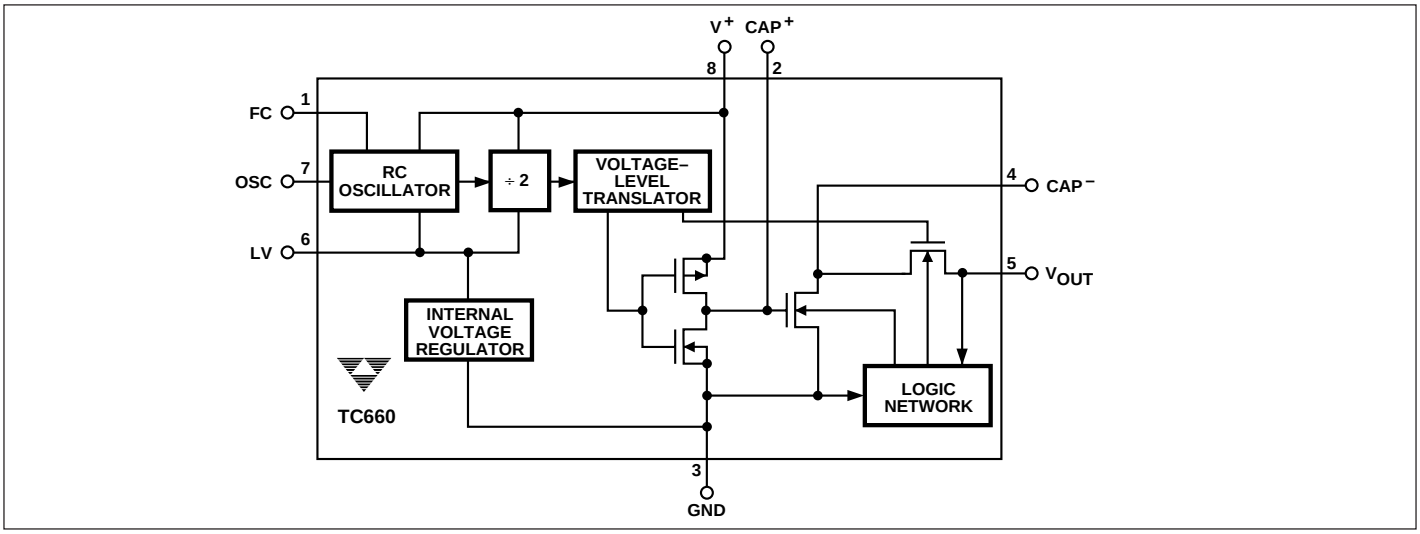
Power supply voltage is stored on an undedicated capacitor then inverted and transferred to an output reservoir capacitor. The on-board oscillator normally runs at a frequency of 10kHz with V^+ at 5V. This frequency can be lowered by the addition of an external capacitor from OSC (pin 7) to ground, or raised to 90kHz by connecting the frequency control pin (FC) to V^+, in order to optimize capacitor size, quiescent current, and output voltage ripple frequency. Operation using input voltage between 1.5V and 3.0V is accommodated by grounding the LV input (pin 6). Operation at higher input voltages (3.0V to 5.5V) is accomplished by leaving LV open.

The TC660 open circuit output voltage is within 0.1% of the input voltage with the output open-circuited. Power conversion efficiency is 98% when output load is between 2mA and 5mA.

ORDERING INFORMATION

Part No.	Package	Temp. Range
TC660COA	8-Pin SOIC	0°C to +70°C
TC660CPA	8-Pin Plastic DIP	0°C to +70°C
TC660EOA	8-Pin SOIC	– 40°C to +85°C
TC660EPA	8-Pin Plastic DIP	– 40°C to +85°C
TC7660EV	***Evaluation Kit for Charge Pump Family***	

FUNCTIONAL BLOCK DIAGRAM



TC660

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage ..... +6V
LV, FC, OSC Input
Voltage (Note 1) ..... V_{OUT} – 0.3V to (V^+ +0.3V)
Current Into LV (Note 1) ..... 20 µA for V^+ >3.5V
Output Short Duration ($V_{SUPPLY} \leq 5.5V$) (Note 3) .. 10 Sec
Power Dissipation (Note 2) ($T_A \leq 70°C$)
SOIC 470mW
Plastic DIP 730mW
Operating Temperature Range
C Suffix ..... 0°C to +70°C
E Suffix ..... – 40°C to +85°C
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: Specifications Measured Over Operating Temperature Range With, V^+ = 5V, C_{OSC} = Open, C1, C2 = 150µF, FC = Open, Test Circuit (Figure 1), unless otherwise indicated.

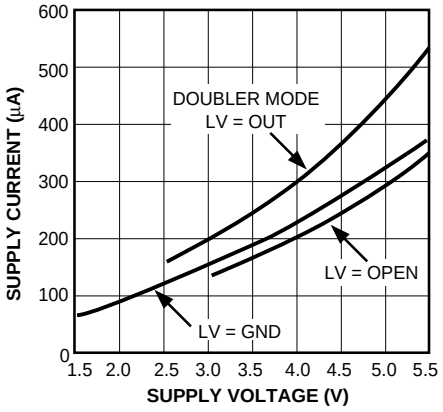
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I^+	Supply Current	$R_L = \infty$				
		FC pin = OPEN or GND	—	200	500	µA
		FC pin = V^+	—	1	3	mA
V^+	Supply Voltage Range	LV = HIGH, R_L = 1 kΩ	3	—	5.5	V
		LV = GND, R_L = 1 kΩ	1.5	—	5.5	
		LV = OUT, R_L = 1 kΩ (Figure 9)	2.5	—	5.5	
R_{OUT}	Output Source Resistance	I_{OUT} = 100mA	—	6.5	10	Ω
I_{OUT}	Output Current	$V_{OUT} < -4V$	100	—	—	mA
F_{OSC}	Oscillator Frequency	Pin 7 open; Pin 1 open or GND	—	10	—	kHz
		Pin 1 = V^+	—	90	—	
I_{OSC}	Input Current	Pin 1 open	—	±1.1	—	µA
		Pin 1 = V^+	—	±5	—	
P_{EFF}	Power Efficiency (Note 4)	R_L = 1 kΩ connected between V^+ & V_{OUT}	96	98	—	%
		R_L = 500Ω connected between V_{OUT} & GND	92	96	—	
		I_L = 100mA to GND	—	88	—	
V_{OUT} E_{FF}	Voltage Conversion Efficiency	$R_L = \infty$	99	99.9	—	%

NOTES: 1. Connecting any input terminal to voltages greater than V^+ or less than GND may cause destructive latch-up. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of the TC660.
2. Derate linearly above 50°C by 5.5 mW/°C.
3. To prevent damaging the device, do not short V_{OUT} to V^+.
4. To maximize output voltage and efficiency performance, use low ESR capacitors for C_1 and C_2.

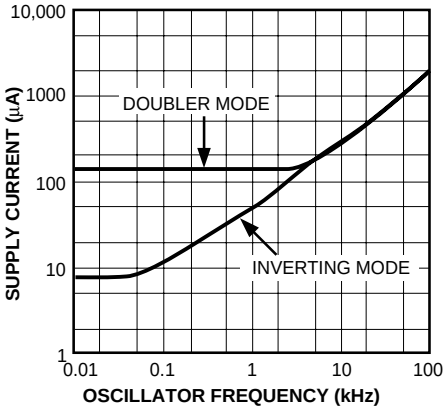
TYPICAL CHARACTERISTICS

All curves are generated using the test circuit of Figure 1 with V^+ = 5V, LV = GND, FC = open, and T_A = +25°C, unless otherwise noted.

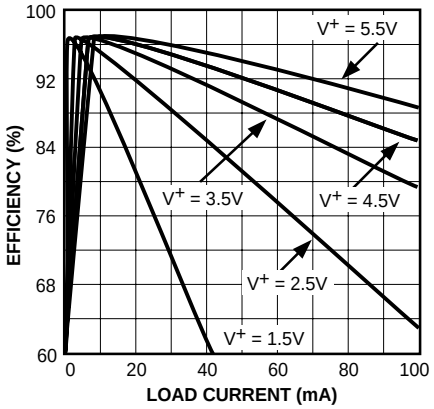
1) Supply Current vs. Supply Voltage



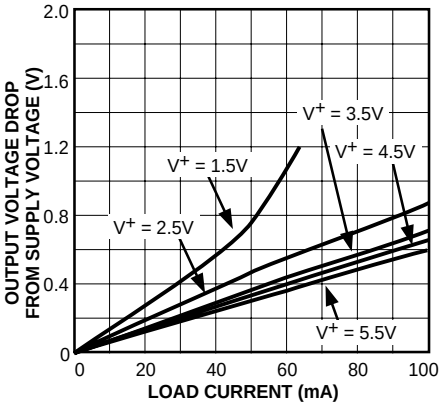
2) Supply Current vs. Oscillator Frequency



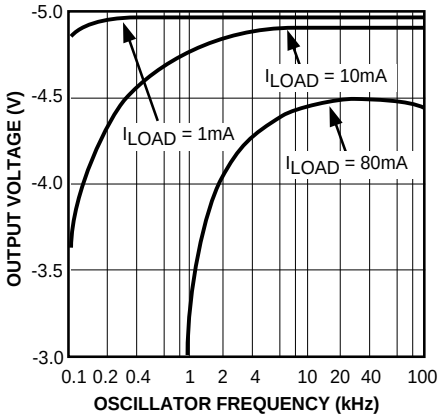
3) Efficiency vs. Load Current



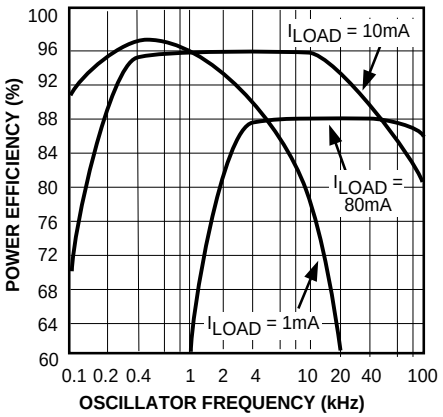
4) Output Voltage Drop vs. Load Current



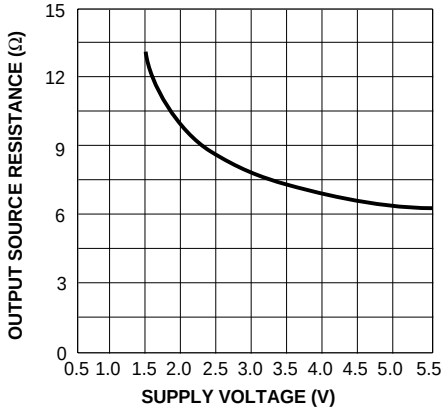
5) Output Voltage vs. Oscillator Frequency



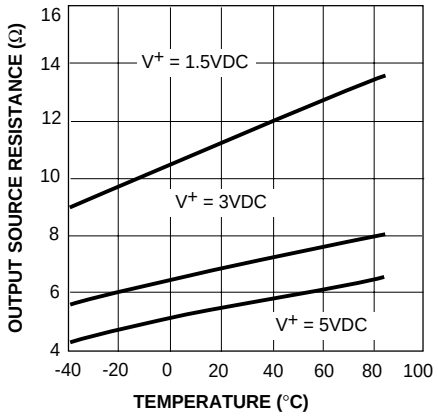
6) Efficiency vs. Oscillator Frequency



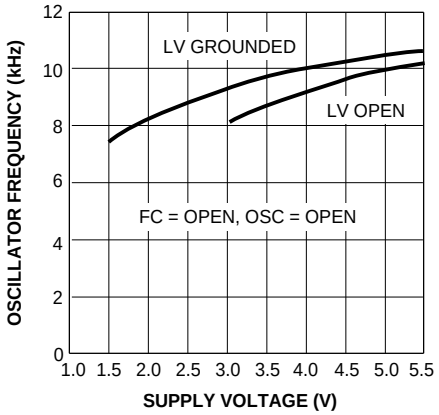
7) Output Source Resistance vs. Supply Voltage



8) Output Source Resistance vs. Temperature



9) Oscillator Frequency vs. Supply Voltage



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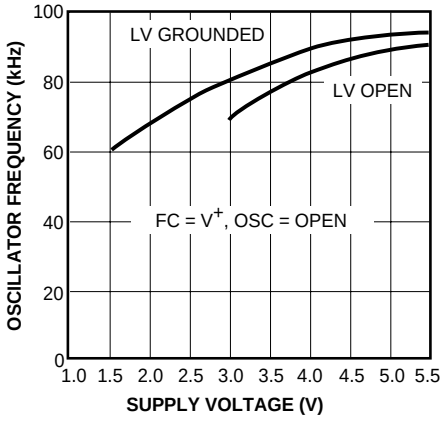
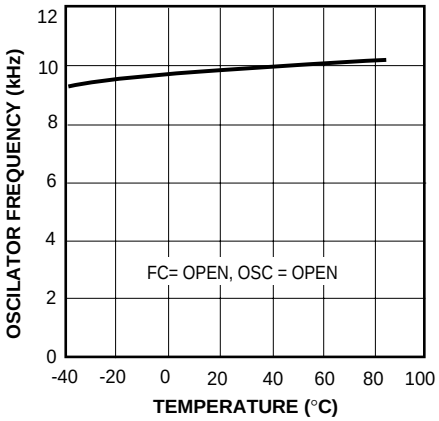
TC660

TYPICAL CHARACTERISTICS (Cont.)

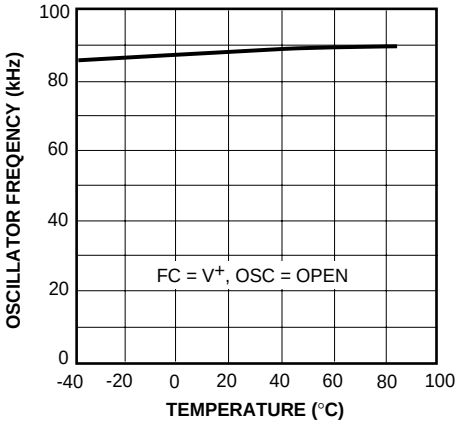
10) Oscillator Frequency vs. Supply Voltage



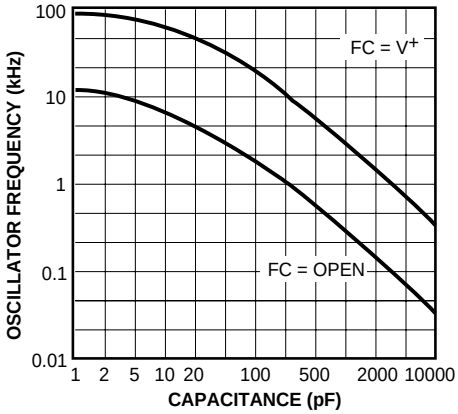
11) Oscillator Frequency vs. Temperature



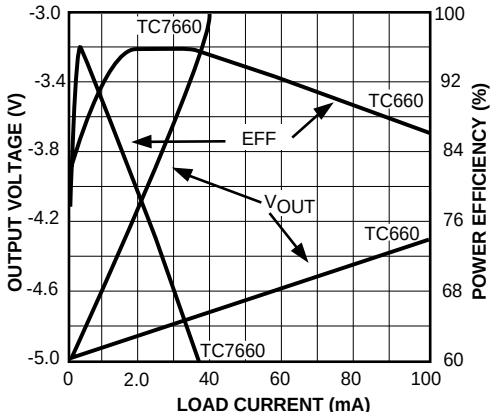
12) Oscillator Frequency vs. Temperature



13) Oscillator Frequency vs. External Capacitance



14) TC7660 and TC660 Output Voltage and Power Efficiency vs. Load Current, V+ = 5V



PIN DESCRIPTION

Pin No.	Symbol	Description
1	FC	Internal Oscillator frequency control. f ≈ 10 kHz when FC ≈ OPEN; ≈ 90 kHz when FC = V^+. FC has no effect if OSC is overdriven.
2	CAP^+	External capacitor, + terminal
3	GND	Power-Supply Ground (Inverter) or Positive Input (Doubler)
4	CAP^-	External capacitor, – terminal
5	V_{OUT}	Negative Voltage output (Inverter) or Ground (Doubler)
6	LV	"Low-Voltage" pin. Connect to GND Pin for inverter operation when V_{IN} < 3V; leave open or GND above 3V. When overdriving OSC, connect to GND.
7	OSC	For external control of internal OSC. Connect ext. C from OSC to GND (close to pkg.) to reduce frequency of oscillator
8	V^+	Positive Voltage Input (Inverter) or Output (Doubler)

Circuit Description

The TC660 contains all the necessary circuitry to complete a voltage inverter (Figure 1), with the exception of two external capacitors, which may be inexpensive 150µF polarized electrolytic capacitors. Operation is best understood by considering Figure 2, which shows an idealized voltage inverter. Capacitor C_1 is charged to a voltage V^+ for the half cycle when switches S_1 and S_3 are closed. (**Note:** Switches S_2 and S_4 are open during this half cycle.) During the second half cycle of operation, switches S_2 and S_4 are closed, with S_1 and S_3 open, thereby shifting capacitor C_1 negatively by V^+ volts. Charge is then transferred from C_1 to C_2, such that the voltage on C_2 is exactly V^+, assuming ideal switches and no load on C_2.

The four switches in Figure 2 are MOS power switches; S_1 is a P-channel device, and S_2, S_3 and S_4 are N-channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of S_3 and S_4 must always remain reverse-biased with respect to their sources, but not so much as to degrade their ON resistances. In addition, at circuit start-up, and under output short circuit conditions ($V_{OUT} = V^+$), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this would result in high power losses and possible device latch-up. This problem is eliminated in the TC660 by a logic network which senses the output voltage (V_{OUT}) together with the level translators, and switches the substrates of S_3 and S_4 to the correct level to maintain necessary reverse bias.

To improve low-voltage operation, the “LV” pin should be connected to GND, disabling the internal regulator. For supply voltages greater than 3.0V, the LV terminal should be left open to ensure latch-up-proof operation and prevent device damage.

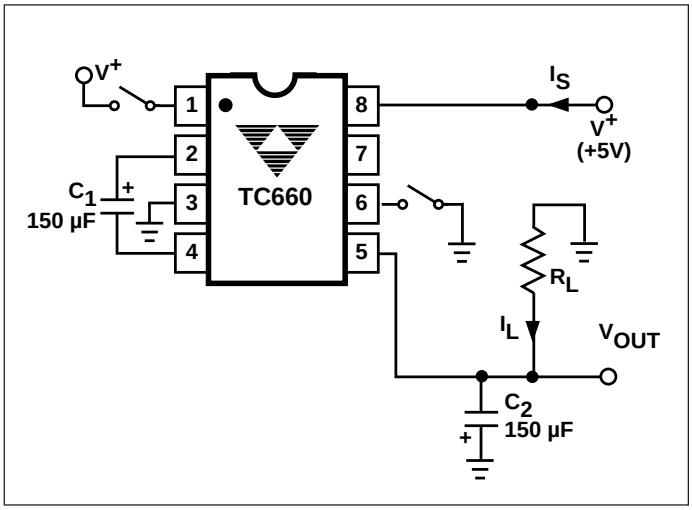


Figure 1. TC660 Test Circuit (Inverter)

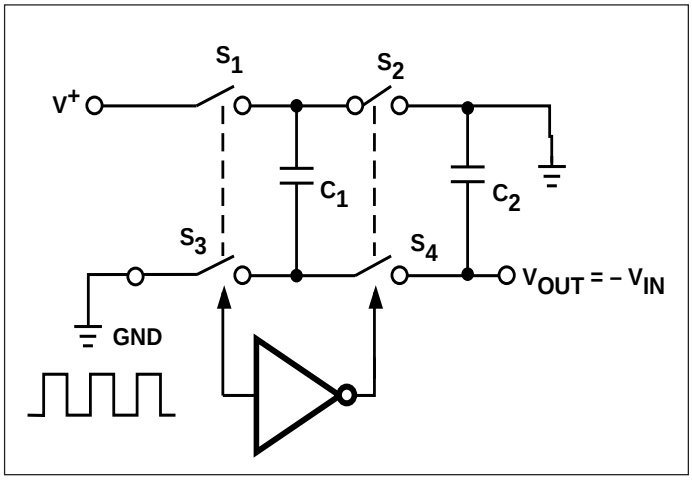


Figure 2. Idealized Switched Capacitor

Theoretical Power Efficiency Considerations

In theory, a voltage multiplier can approach 100% efficiency if certain conditions are met:

(1) The drive circuitry consumes minimal power.

(2) The output switches have extremely low ON resistance and virtually no offset.

(3) The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The TC660 approaches these conditions for negative voltage multiplication if large values of C_1 and C_2 are used. **Energy is lost only in the transfer of charge between capacitors if a change in voltage occurs.** The energy lost is defined by:

$$E = 1/2\ C_1\ (V_1^2 - V_2^2)$$

V_1 and V_2 are the voltages on C_1 during the pump and transfer cycles. If the impedances of C_1 and C_2 are relatively high at the pump frequency (refer to Figure 2) compared to the value of R_L, there will be a substantial difference in voltages V_1 and V_2. Therefore, it is desirable not only to make C_2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_1 in order to achieve maximum efficiency of operation.

Dos and Don'ts

- Do not exceed maximum supply voltages.
- Do not connect the LV terminal to GND for supply voltages greater than 3.0V.
- Do not short circuit the output to V^+ in inverting mode and for more than 10 sec (a very slow startup!) in doubler mode.
- When using polarized capacitors in the inverting mode, the + terminal of C_1 must be connected to pin 2 of the TC660 and the + terminal of C_2 must be connected to GND.

Simple Negative Voltage Converter

Figure 3 shows typical connections to provide a negative supply where a positive supply is available. A similar scheme may be employed for supply voltages anywhere in the operating range of +1.5V to +5.5V, keeping in mind that pin 6 (LV) is tied to the supply negative (GND) only for supply voltages below 3.0V.

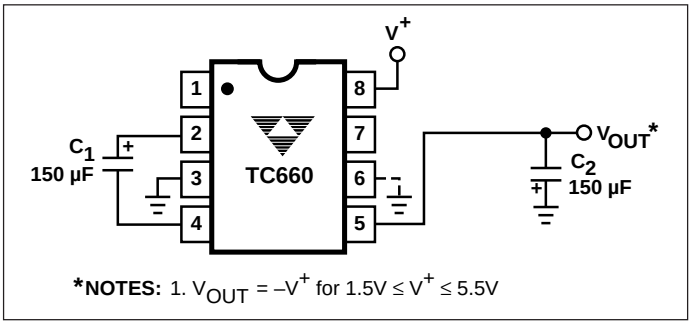


Figure 3. Simple Negative Converter

The output characteristics of the circuit in Figure 3 are those of a nearly ideal voltage source in series with 6.5Ω. Thus, for a load current of –100mA and a supply voltage of +5V, the output voltage would be – 4.35V.

The dynamic output impedance of the TC660 is due, primarily, to capacitive reactance of the charge transfer capacitor (C_1). Since this capacitor is connected to the output for only 1/2 of the cycle, the equation is:

$$X_C = \frac{2}{2\pi f\, C_1} = 0.21\Omega,$$

where f = 10 kHz and C_1 = 150 µF.

Paralleling Devices

Any number of TC660 voltage converters may be paralleled to reduce output resistance (Figure 4). The reservoir capacitor, C_2, serves all devices, while each device requires its own pump capacitor, C_1. The resultant output resistance would be approximately:

$$R_{OUT} = \frac{R_{OUT}\ (\text{of TC660})}{n\ (\text{number of devices})}$$

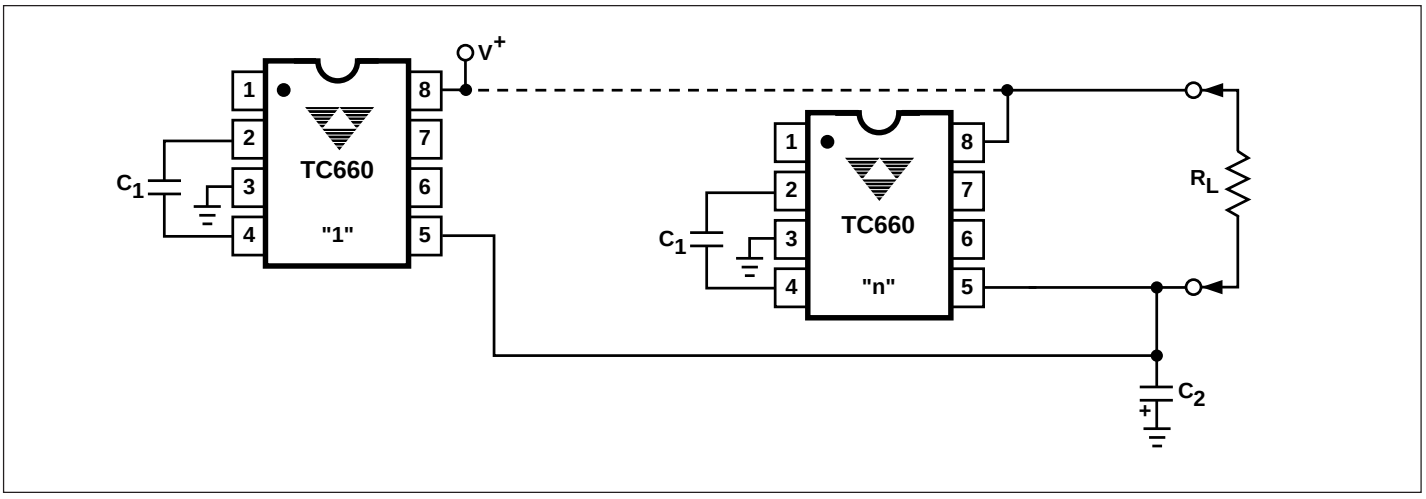


Figure 4. Paralleling Devices Lowers Output Impedance

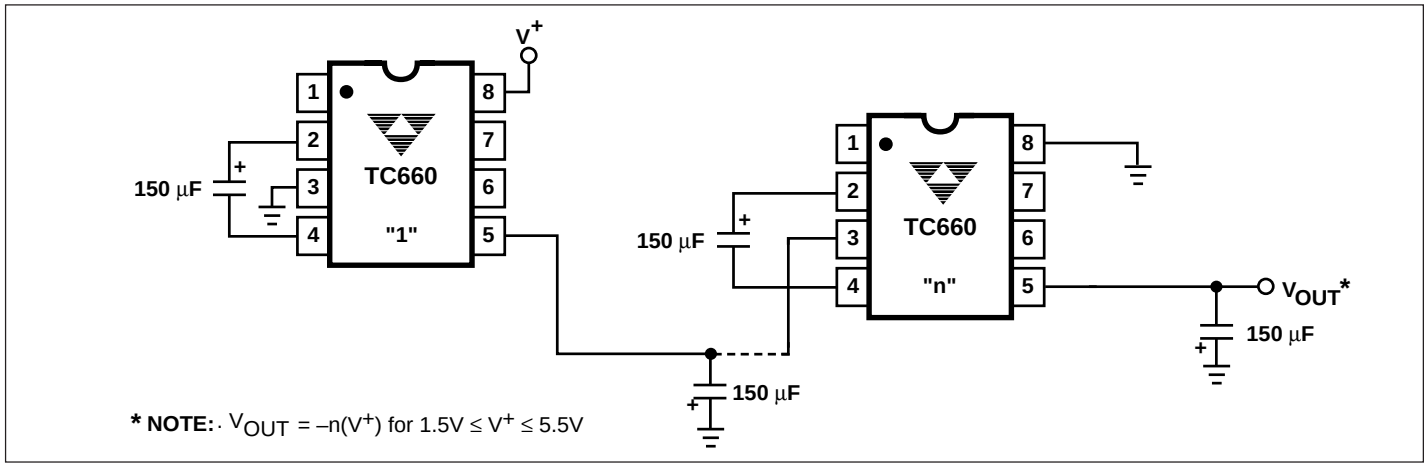


Figure 5. Increased Output Voltage by Cascading Devices

Cascading Devices

The TC660 may be cascaded as shown (Figure 5) to produce larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -n\ (V_{IN})$$

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual TC660 R_{OUT} values.

Changing the TC660 Oscillator Frequency

It may be desirable in some applications (due to noise or other considerations) to increase the oscillator frequency. Pin 1, the FC pin, may be connected to V^+ to increase oscillator frequency to 90kHz from a nominal of 10 kHz for an input supply voltage of 5.0 volts. The oscillator may also be synchronized to an external clock as shown in Figure 6 and LV must be grounded when overdriving OSC. In a situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10kΩ pull-up resistor to V^+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be 1/2 of the clock frequency. Output transitions occur on the positive-going edge of the clock.

It is also possible to increase the conversion efficiency of the TC660 at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is achieved by connecting an additional capacitor, C_{OSC}, as shown in Figure 7. Lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C_1) and the reservoir (C_2) capacitors. To overcome this, increase the values of C_1 and C_2 by the same factor that the frequency has been reduced. For example, the addition of a 100pF capacitor between pin 7 (OSC) and GND will lower the oscillator frequency to 1kHz from its nominal frequency of 10kHz (a multiple of 10), and necessitate a corresponding increase in the values of C_1 and C_2.

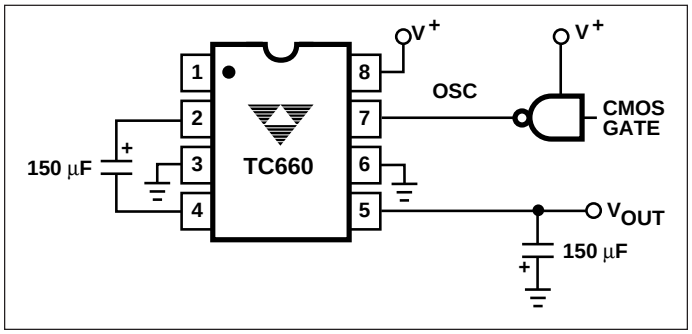


Figure 6. External Clocking

Positive Voltage Doubler

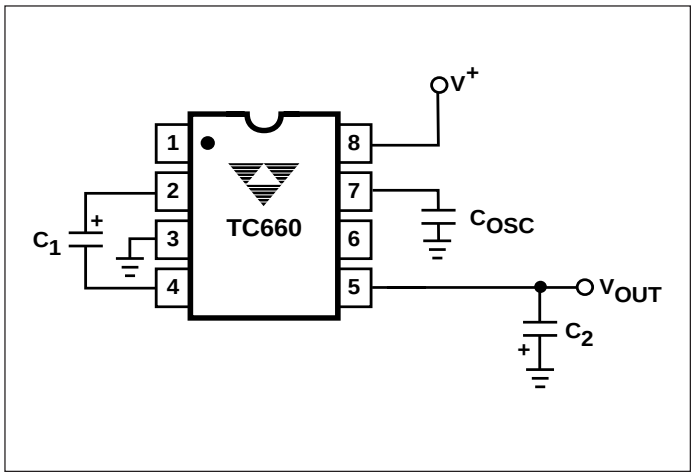


Figure 7. Lowering Oscillator Frequency

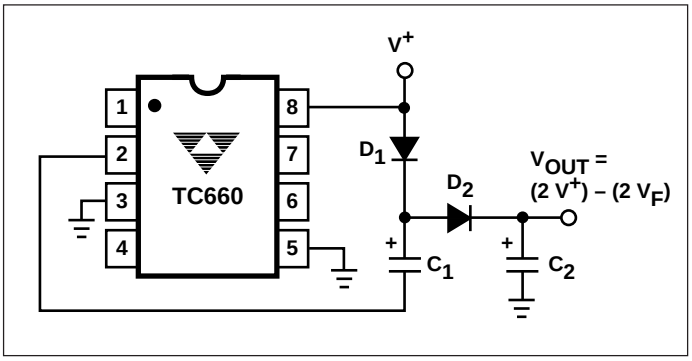


Figure 8. Positive Voltage Doubler

Figure 9 shows an improved way of using the TC660 as a voltage doubler.

In this circuit, C1 is first charged to V_{IN} and C2 is quickly brought to within a diode drop of V_{IN} (to prevent substrate reversal) through D. The optional 200 Ω resistor is only to limit the brief latchup current.

On the next half-cycle, V_{IN} is in series with C1; C2 is then charged to 2 V_{IN}. D is now reverse-biased and plays no further part. For V_{IN} < 3V, R may be necessary to ensure startup.

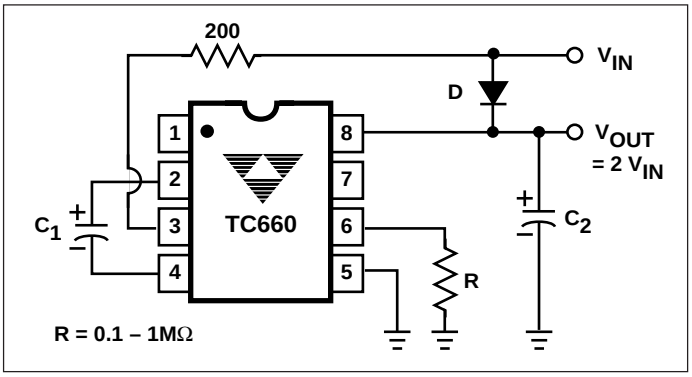


Figure 9. Improved Voltage Doubler

Combined Negative Voltage Conversion and Positive Supply Multiplication

Figure 10 combines the functions shown in Figures 3 and 8 to provide negative voltage conversion and positive voltage multiplication simultaneously. In this instance, capacitors C_1 and C_3 perform the pump and reservoir functions, respectively, for the generation of the negative voltage, while capacitors C_2 and C_4 are pump and reservoir, respectively, for the multiplied positive voltage. There is a penalty in this configuration in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

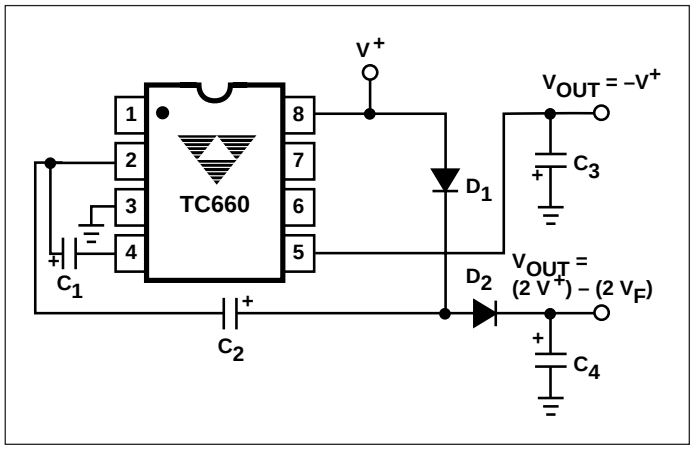


Figure 10. Combined Negative Converter and Positive Multiplier

Efficient Positive Voltage Multiplication/Conversion

Since the switches that allow the charge pumping operation are bidirectional, the charge transfer can be performed backward as easily as forward. Figure 11 shows a TC660 transforming –5V to +5V. The only problem here is that the internal clock and switch-drive section will not operate until some positive voltage has been generated. A diode and resistor shown dotted in Figure 11 can be used to "force" the internal regulator on.

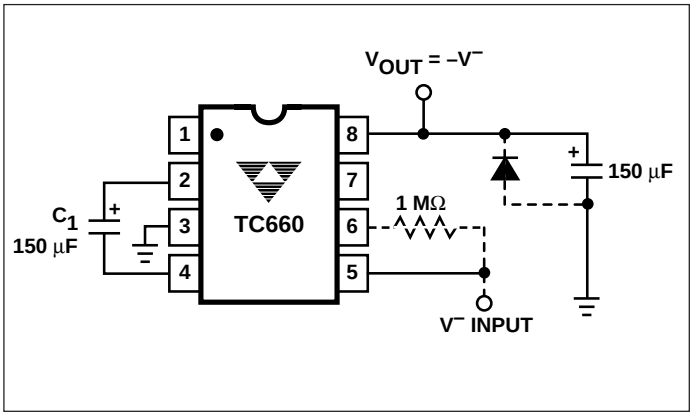


Figure 11. Positive Voltage Multiplier