

# DATA SHEET

Part No.	AN44069A
Package Code No.	HSOP042-P-0400D

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# AN44069A

## Driver IC for Stepping Motor

### ■ Overview

AN44069A is a two channels H-bridge driver IC. Bipolar stepping motor can be controlled by a single driver IC. 2-phase, half-step, 1-2 (type2) phase, W1-2 phase can be selected.

### ■ Features

- 4-phase input control (W1-2 phase excitation enabled)
- Built-in CR chopping (with frequency selected)
- Built-in thermal protection and low voltage detection circuit
- Built-in 5 V power supply

### ■ Applications

- IC for stepping motor drives

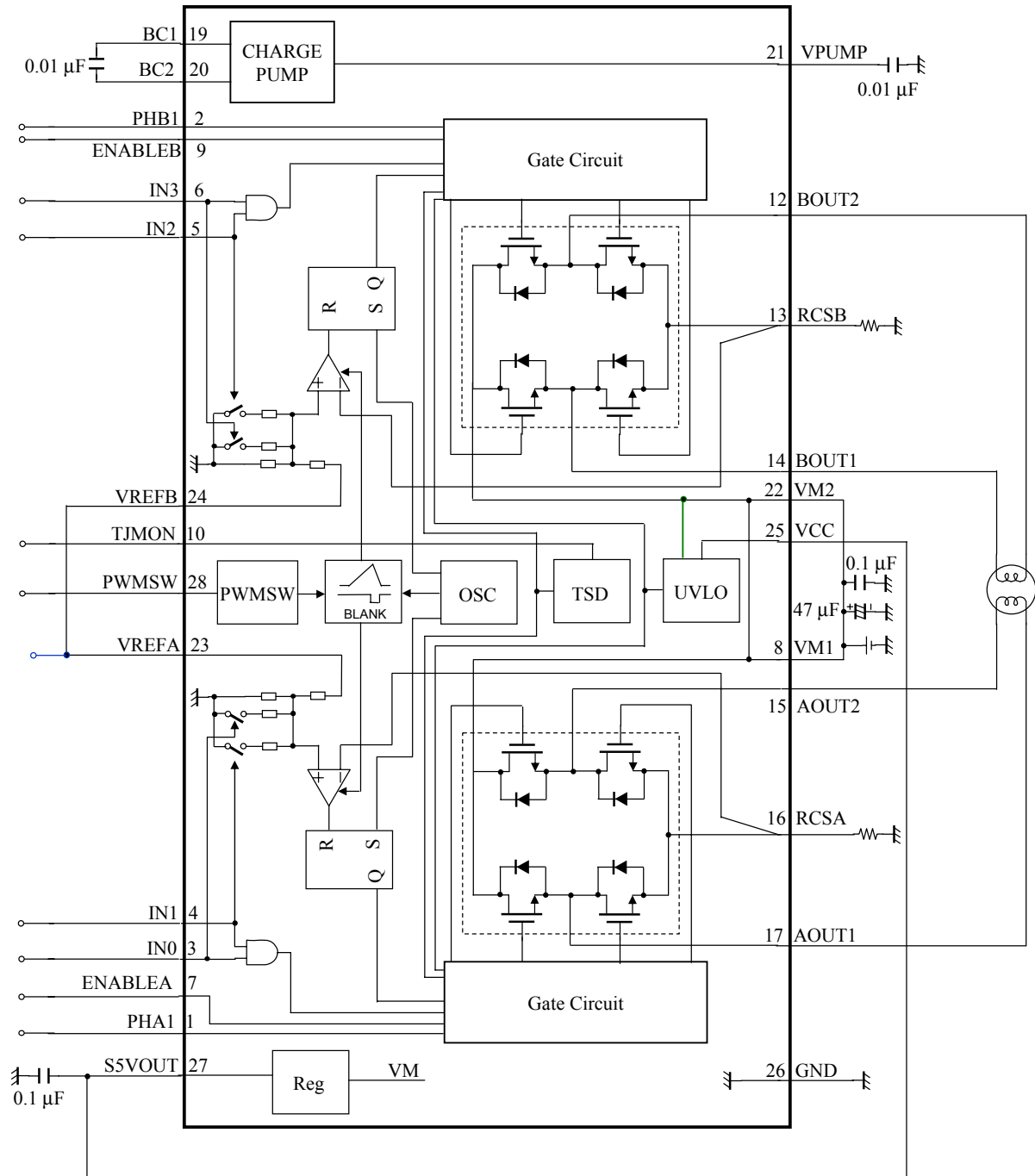
### ■ Package

- 28 pin Plastic Small Outline Package With Heat Sink (SOP Type)

### ■ Type

- Bi-CDMOS IC

## ■ Application Circuit Example



Notes) This application circuit is shown as an example but does not guarantee the design for mass production set.

## ■ Pin Descriptions

Pin No.	Pin name	Type	Description
1	PHA1	Input	Phase A phase selection input
2	PHB1	Input	Phase B phase selection input
3	IN0	Input	Phase A output torque control 1
4	IN1	Input	Phase A output torque control 2
5	IN2	Input	Phase B output torque control 1
6	IN3	Input	Phase B output torque control 2
7	ENABLEA	Input	Phase A Enable/Disable CTL
8	VM1	Power supply	Motor power supply 1
9	ENABLEB	Input	Phase B Enable/Disable CTL
10	TJMON	Output	VBE monitor use
11	N.C.	—	N.C.
12	BOUT2	Output	Phase B motor drive output 2
13	RCSB	Input / Output	Phase B current detection
14	BOUT1	Output	Phase B motor drive output 1
15	AOUT2	Output	Phase A motor drive output 2
16	RCSA	Input / Output	Phase A current detection
17	AOUT1	Output	Phase A motor drive output 1
18	N.C.	—	N.C.
19	BC1	Output	Charge pump capacitor connection 1
20	BC2	Output	Charge pump capacitor connection 2
21	VPUMP	Output	Charge pump circuit output
22	VM2	Power supply	Motor power supply 2
23	VREFA	Input	Phase A torque reference voltage input
24	VREFB	Input	Phase B torque reference voltage input
25	VCC	Power supply	Signal power supply
26	GND	Ground	Signal ground
27	S5VOUT	Output	Internal reference voltage (5 V output)
28	PWMSW	Input	PWM frequency selection input
FIN	FIN	—	Die pad ground (N.C.)

## ■ Absolute Maximum Ratings

Note) Absolute maximum ratings are limit values which are not destructed, and are not the values to which operation is guaranteed.

A No.	Parameter	Symbol	Rating	Unit	Notes
1	Supply voltage 1 (Pin 8, 22)	$V_M$	37	V	*1
2	Supply voltage 2 (Pin 25)	$V_{CC}$	-0.3 to +6	V	*1
3	Power dissipation	$P_D$	0.717	W	*2
4	Operating ambient temperature	$T_{opr}$	-20 to +70	°C	*3
5	Storage temperature	$T_{stg}$	-55 to +150	°C	*3
6	Output pin voltage (Pin 12, 14, 15, 17)	$V_{OUT}$	37	V	*4
7	Motor drive current (Pin 12, 14, 15, 17)	$I_{OUT}$	$\pm 1.5$	A	*4
8	Flywheel diode current (Pin 12, 14, 15, 17)	$I_f$	1.5	A	*4

Notes) \*1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

\*2 : The power dissipation shown is the value at  $T_a = 70^\circ\text{C}$  for the independent (unmounted) IC package without a heat sink.

When using this IC, refer to the  $P_D$ - $T_a$  diagram of the package standard and design the heat radiation with sufficient margin so that the allowable value might not be exceeded based on the conditions of power supply voltage, load, and ambient temperature.

\*3 : Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for  $T_a = 25^\circ\text{C}$ .

\*4 : Do not apply current or voltage from outside to any pin not listed above.

In the circuit current (+) means the current flowing into IC and (-) means the current flowing out of IC.

## ■ Operating supply voltage range

Parameter	Symbol	Range	Unit	Notes
Supply voltage range 1	$V_M$	16.0 to 34.0	V	*
Supply voltage range 2	$V_{CC}$	4.5 to 5.5	V	*

Note) \* : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

### ■ Allowable Current and Voltage Range

Notes) • Voltage values, unless otherwise specified, are with respect to GND.

• Do not apply external currents or voltages to any pin not specifically mentioned.

• For the circuit currents, "+" denotes current flowing into the IC, and "-" denotes current flowing out of the IC.

Pin No.	Pin name	Rating	Unit	Notes
1	PHA1	-0.3 to 6	V	—
2	PHB1	-0.3 to 6	V	—
3	IN0	-0.3 to 6	V	—
4	IN1	-0.3 to 6	V	—
5	IN2	-0.3 to 6	V	—
6	IN3	-0.3 to 6	V	—
7	ENABLEA	-0.3 to 6	V	—
9	ENABLEB	-0.3 to 6	V	—
13	RCSB	2.5	V	—
16	RCSA	2.5	V	—
19	BC1	$V_M + 0.3$	V	*1
20	BC2	$(V_M - 1)$ to 43	V	*1
21	VPUMP	$(V_M - 1)$ to 43	V	*1
23	VREFA	-0.3 to 6	V	—
24	VREFB	-0.3 to 6	V	—
28	PWMSW	-0.3 to 6	V	—

Pin No.	Pin name	Rating	Unit	Notes
27	S5VOUT	-7 to 0	mA	*1

Notes) \*1 : External voltage must not be applied to these pins. Design so that the voltage does not exceed ratings even transiently.

■ Electrical Characteristics at  $V_M = 24.0\text{ V}$ ,  $V_{CC} = 5.0\text{ V}$

Note)  $T_a = 25^\circ\text{C} \pm 2^\circ\text{C}$  unless otherwise specified.

B No.	Parameter	Symbol	Conditions	Limits			Unit	Notes
				Min	Typ	Max		
Power Block								
1	High-level output saturation voltage	V <sub>OH</sub>	I = −0.8 A	V <sub>M</sub> − 0.75	V <sub>M</sub> − 0.50	—	V	—
2	Low-level output saturation voltage	V <sub>OL</sub>	I = 0.8 A	—	0.75	1.14	V	—
3	Flywheel diode forward voltage	V <sub>DI</sub>	I = 0.8 A	0.5	1.0	1.5	V	—
4	Output leakage current 1	I <sub>LEAK1</sub>	V <sub>M</sub> = 37 V, V <sub>RCS</sub> = 0 V	—	10	20	μA	—
5	Supply current	I <sub>M</sub>	ENABLEA = ENABLEB = 5 V	—	4	6	mA	—
I/O Block								
6	Supply current (with two circuits turned OFF)	I <sub>CC</sub>	ENABLEA = ENABLEB = 5 V	—	1.4	2.2	mA	—
7	High-level IN input voltage	V <sub>INH</sub>	—	2.2	—	V <sub>CC</sub>	V	—
8	Low-level IN input voltage	V <sub>INL</sub>	—	0	—	0.6	V	—
9	High-level IN input current	I <sub>INH</sub>	IN0 = IN1 = IN2 = IN3 = 5 V	−10	—	10	μA	—
10	Low-level IN input current	I <sub>INL</sub>	IN0 = IN1 = IN2 = IN3 = 0 V	−15	—	15	μA	—
11	High-level PHA1, PHB1 input voltage	V <sub>PHAH</sub> V <sub>PHBH</sub>	—	2.2	—	V <sub>CC</sub>	V	—
12	Low-level PHA1, PHB1 input voltage	V <sub>PHAL</sub> V <sub>PHBL</sub>	—	0	—	0.6	V	—
13	High-level PHA1, PHB1 input current	I <sub>PHAH</sub> I <sub>PHBH</sub>	PHA1 = PHB1 = 3.3 V	16.5	33	66	μA	—
14	Low-level PHA1, PHB1 input current	I <sub>PHAL</sub> I <sub>PHBL</sub>	PHA1 = PHB1 = 0 V	−15	—	15	μA	—
15	High-level ENABLEA, ENABLEB input voltage	V <sub>ENABLEAH</sub> V <sub>ENABLEBH</sub>	—	2.2	—	V <sub>CC</sub>	V	—
16	Low-level ENABLEA, ENABLEB input voltage	V <sub>ENABLEAL</sub> V <sub>ENABLEBL</sub>	—	0	—	0.6	V	—
17	High-level ENABLEA, ENABLEB input current	I <sub>ENABLEAH</sub> I <sub>ENABLEBH</sub>	ENABLEA = ENABLEB = 5 V	−10	—	10	μA	—
18	Low-level ENABLEA, ENABLEB input current	I <sub>ENABLEAL</sub> I <sub>ENABLEBL</sub>	ENABLEA = ENABLEB = 0 V	−15	—	15	μA	—
19	High-level PWMSW input voltage	V <sub>PWMSWH</sub>	—	2.2	—	V <sub>CC</sub>	V	—
20	Low-level PWMSW input voltage	V <sub>PWMSWL</sub>	—	0	—	0.6	V	—
21	High-level PWMSW input current	I <sub>PWMSWH</sub>	PWMSW = 3.3 V	16.5	33	66	μA	—
22	Low-level PWMSW input current	I <sub>PWMSWL</sub>	PWMSW = 0 V	−15	—	15	μA	—

■ Electrical Characteristics (continued) at  $V_M = 24.0\text{ V}$ ,  $V_{CC} = 5.0\text{ V}$

Note)  $T_a = 25^\circ\text{C} \pm 2^\circ\text{C}$  unless otherwise specified.

B No.	Parameter	Symbol	Conditions	Limits			Unit	Notes
				Min	Typ	Max		
Torque control Block								
23	Input bias current	$I_{\text{REFA}}$ $I_{\text{REFB}}$	$V_{\text{REFA}} = 5\text{ V}$ $V_{\text{REFB}} = 5\text{ V}$	83.3	100	125	$\mu\text{A}$	—
24	PWM frequency 1	$f_{\text{PWM1}}$	PWMSW = 0 V	34	52	70	kHz	—
25	PWM frequency 2	$f_{\text{PWM2}}$	PWMSW = 5 V	17	26	35	kHz	—
26	Pulse blanking time	$T_{\text{B}}$	$V_{\text{REFA}} = V_{\text{REFB}} = 0\text{ V}$	0.38	0.75	1.12	$\mu\text{s}$	—
27	Comp threshold H (100%)	$V_{\text{T}_{\text{H}}}$	IN0 = IN1 = 0.6 V IN2 = IN3 = 0.6 V	475	500	525	mV	—
28	Comp threshold C (67%)	$V_{\text{T}_{\text{C}}}$	IN0 = 2.2 V, IN1 = 0.6 V IN2 = 2.2 V, IN3 = 0.6 V	308	333	359	mV	—
29	Comp threshold L (33%)	$V_{\text{T}_{\text{L}}}$	IN0 = 0.6 V, IN1 = 2.2 V IN2 = 0.6 V, IN3 = 2.2 V	151	167	184	mV	—
Reference voltage Block								
30	Reference voltage	$V_{\text{SSVOUT}}$	$I_{\text{SSVOUT}} = -2.5\text{ mA}$	4.5	5.0	5.5	V	—
31	Output impedance	$Z_{\text{SSVOUT}}$	Impedance of $I_{\text{SSVOUT}} = -2.5\text{ mA}, -5\text{ mA}$	—	18	27	$\Omega$	—

■ Electrical Characteristics (Reference values for design) at  $V_M = 24.0\text{ V}$ ,  $V_{CC} = 5.0\text{ V}$

Notes)  $T_a = 25^\circ\text{C} \pm 2^\circ\text{C}$  unless otherwise specified.

The characteristics listed below are reference values derived from the design of the IC and are not guaranteed by inspection.

If a problem does occur related to these characteristics, we will respond in good faith to user concerns.

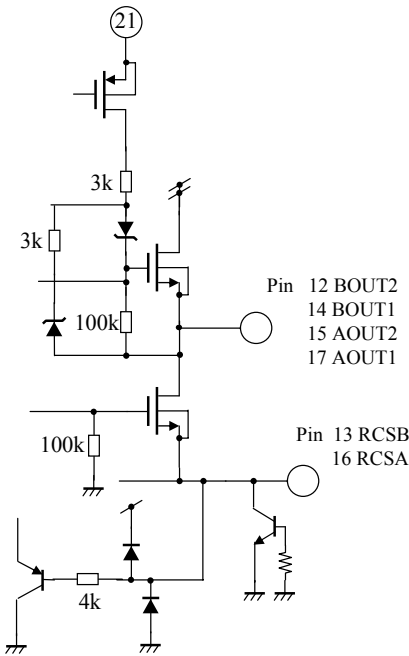
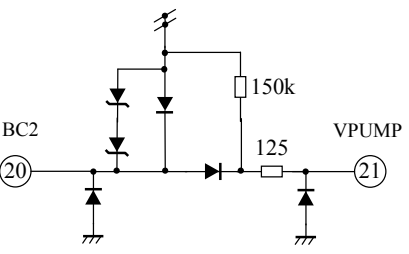
B No.	Parameter	Symbol	Conditions	Reference values			Unit	Notes
				Min	Typ	Max		
Output Drivers								
32	Output slew rate 1	$V_{T_r}$	Rising edge	—	270	—	V/ $\mu$ s	—
33	Output slew rate 2	$V_{T_f}$	Falling edge	—	330	—	V/ $\mu$ s	—
34	Dead time	$T_D$	—	—	2.8	—	$\mu$ s	—
Thermal Protection								
35	Thermal protection operating temperature	$TSD_{on}$	—	—	150	—	$^{\circ}$ C	—
36	Thermal protection hysteresis width	$\Delta TSD$	—	—	40	—	$^{\circ}$ C	—
I/O Block								
37	High-level PHA1, PHB1, PWMSW input current 2	$I_{PHAH2}$ $I_{PHBH2}$ $I_{PWMSWH2}$	—	—	68	—	$\mu$ A	*1

Note) \*1 : For the input current characteristic of PHA1, PHB1, and PWMSW, refer to Usage Notes described in Page 33.

■ Technical Data

- I/O block circuit diagrams and pin function descriptions

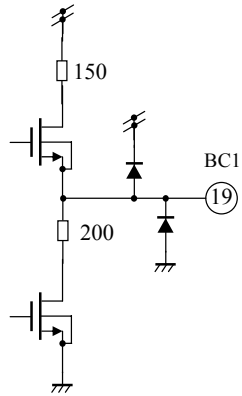
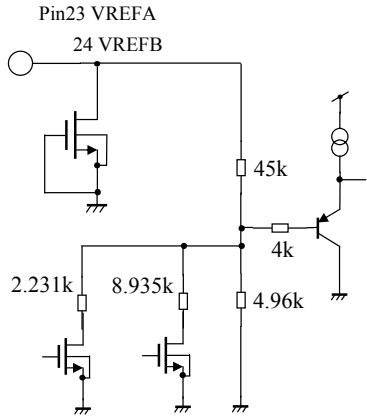
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
12 13 14 15 16 17	—		—	Pin 12 : Phase B motor drive output 2 Pin 13 : Phase B current detection Pin 14 : Phase B motor drive output 1 Pin 15 : Phase A motor drive output 2 Pin 16 : Phase A current detection Pin 17 : Phase A motor drive output 1
20 21	—		—	Pin20 : Charge pump capacitor connection 2 Pin21 : Charge pump circuit output

■ Technical Data (continued)

- I/O block circuit diagrams and pin function descriptions (continued)

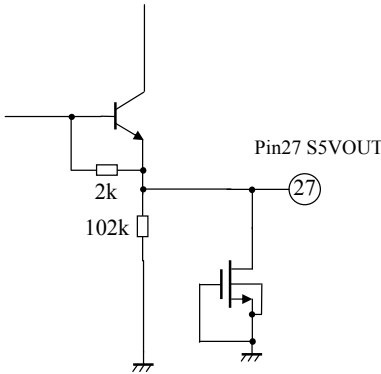
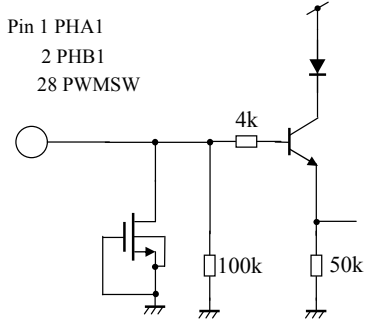
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
19	—		—	Pin 19 : Charge pump capacitor connection 1
23 24	—		50 kΩ	Pin 23 : Phase A torque reference voltage input 24 : Phase B torque reference voltage input

■ Technical Data (continued)

- I/O block circuit diagrams and pin function descriptions (continued)

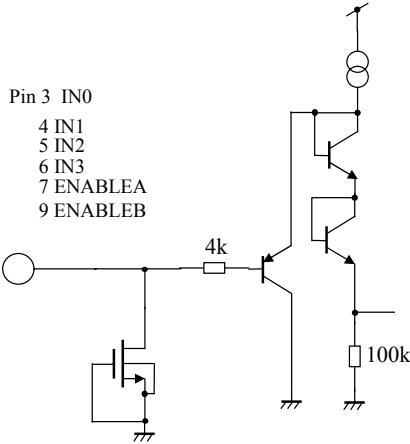
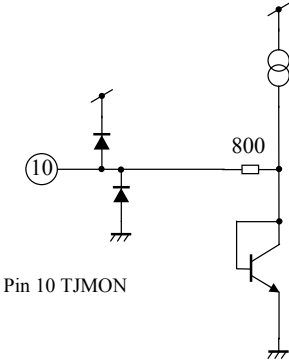
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
27	—		102 kΩ	Pin 27 : Internal reference voltage (5 V-output)
1 2 28	—		100 kΩ	Pin 1 : Phase A phase selection input 2 : Phase B phase selection input 28 : PWM frequency selection

■ Technical Data (continued)

- I/O block circuit diagrams and pin function descriptions (continued)






Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
3 4 5 6 7 9	—		—	Pin 3 : Phase A output torque control 1 4 : Phase A output torque control 2 5 : Phase B output torque control 1 6 : Phase B output torque control 2 7 : Phase A Enable/Disable signal input 9 : Phase B Enable/Disable signal input
10	—		—	Pin10 : VBE monitor

■ Technical Data (continued)

- I/O block circuit diagrams and pin function descriptions (continued)

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
Symbols	—	 VCC (Pin 25)  VM(Pin 8, Pin 22)  Diode  Zener diode  Ground	—	—

■ Technical Data (continued)

- Control mode

1. Truth table

ENABLEA/ENABLEB	PHA1/PHB1	AOUT1/BOUT1	AOUT2/BOUT2
"L"	"H"	"H"	"L"
"L"	"L"	"L"	"H"
"H"	—	OFF	OFF

IN0/IN2	IN1/IN3	Output current
"L"	"L"	$(V_{REF} / 10) \times (1 / R_s) = I_{OUT}$
"H"	"L"	$(V_{REF} / 10) \times (1 / R_s) \times (2 / 3) = I_{OUT}$
"L"	"H"	$(V_{REF} / 10) \times (1 / R_s) \times (1 / 3) = I_{OUT}$
"H"	"H"	0

Note 1)  $R_s$  : Current detection resistance

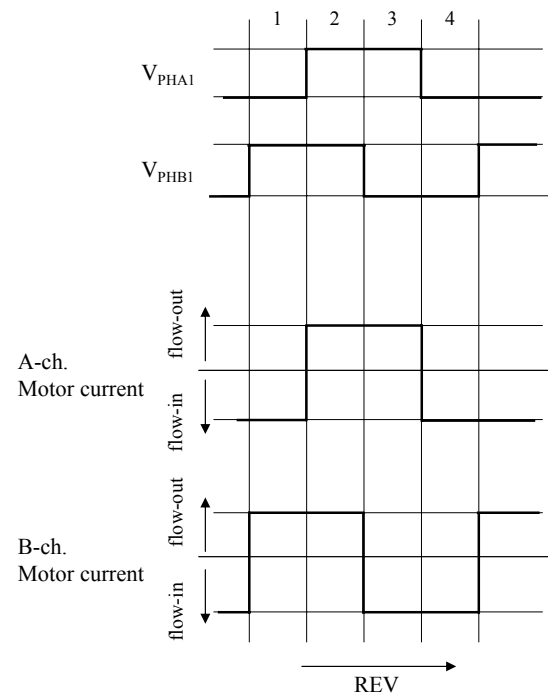
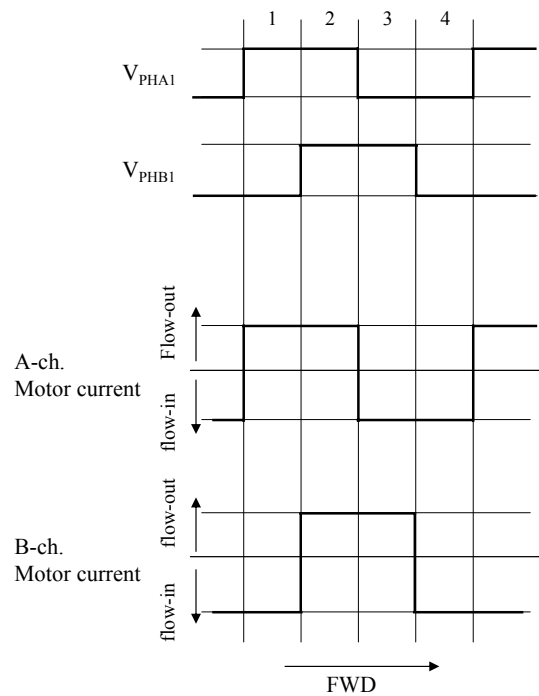
Note2) ENABLEA = ENABLEB = "H" or IN0 = IN1 = "H" / IN2 = IN3 = "H", all outputs transistors turn off at the same time.

## ■ Technical Data (continued)

- Control mode (continued)

## 2. Drive of full step (4steps sequence)

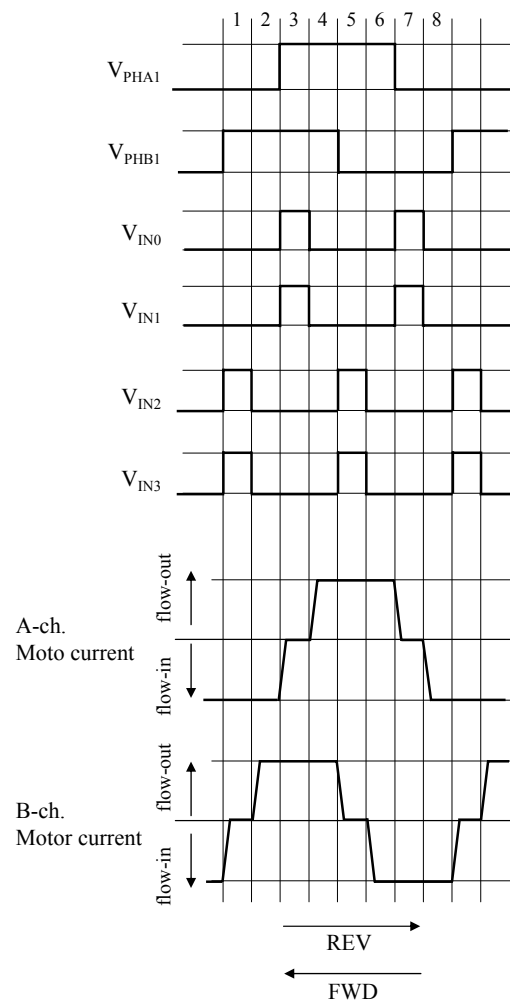
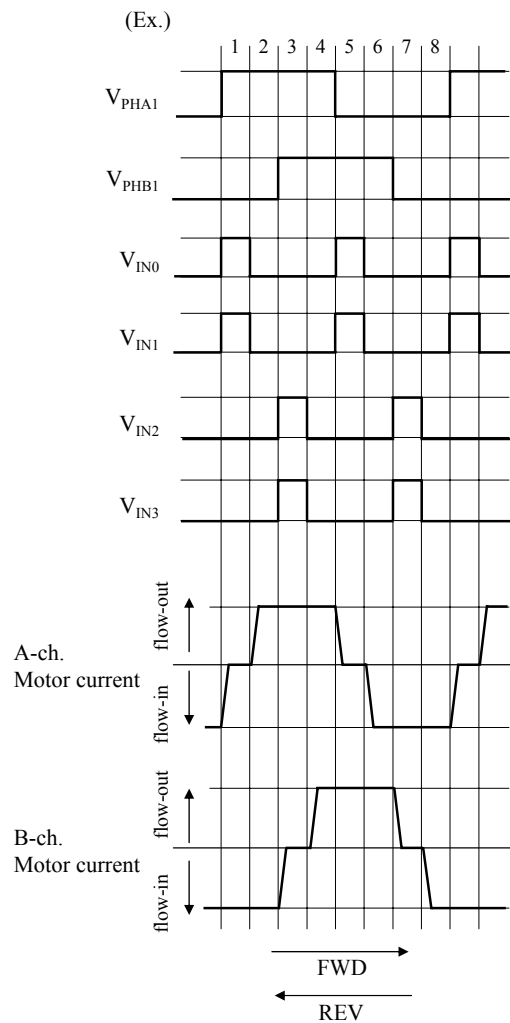
(IN0 to IN3 = const.)



# ■ Technical Data (continued)

- Control mode (continued)

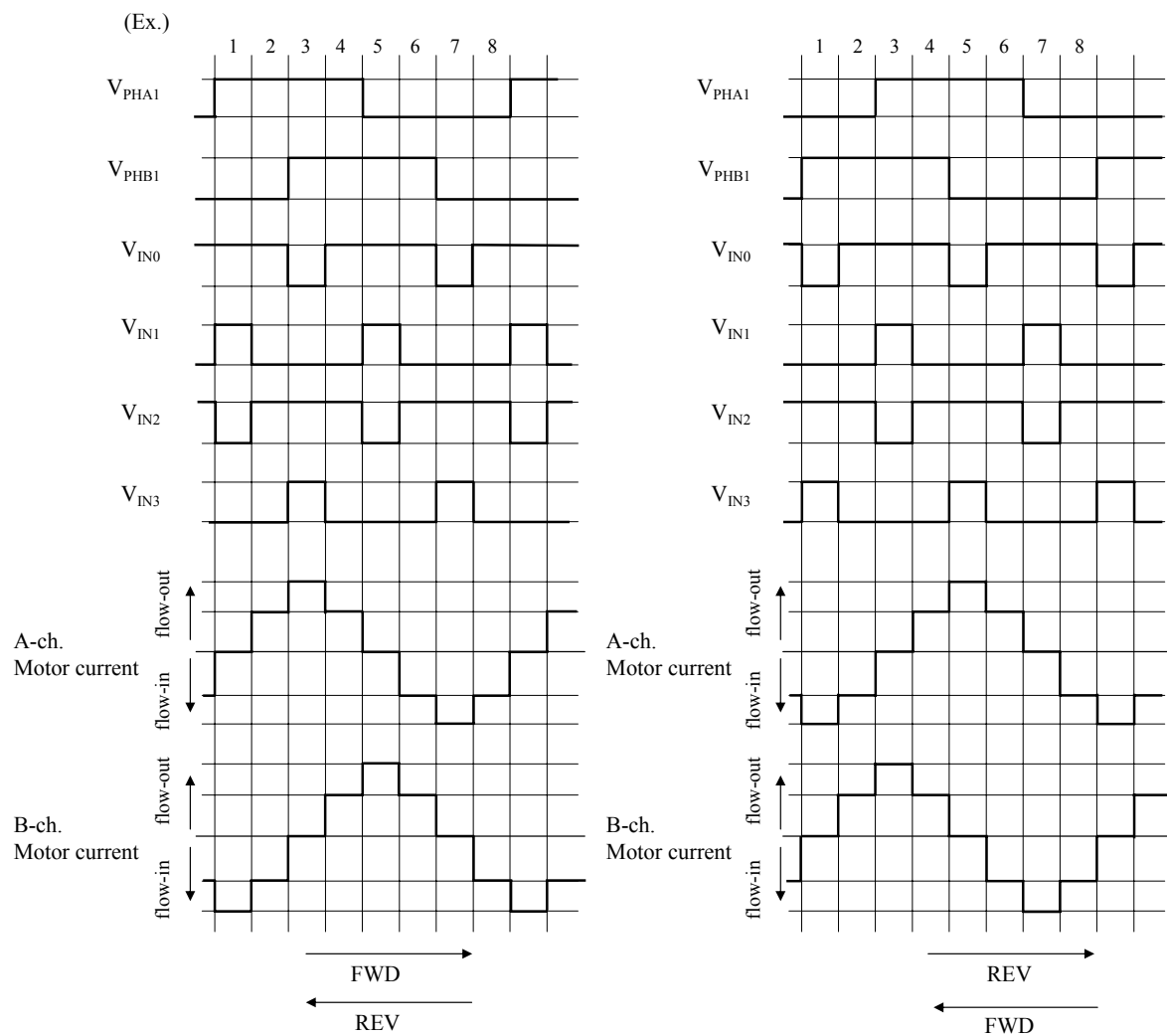
## 3. Drive of half step (8steps sequence)



## ■ Technical Data (continued)

- Control mode (continued)

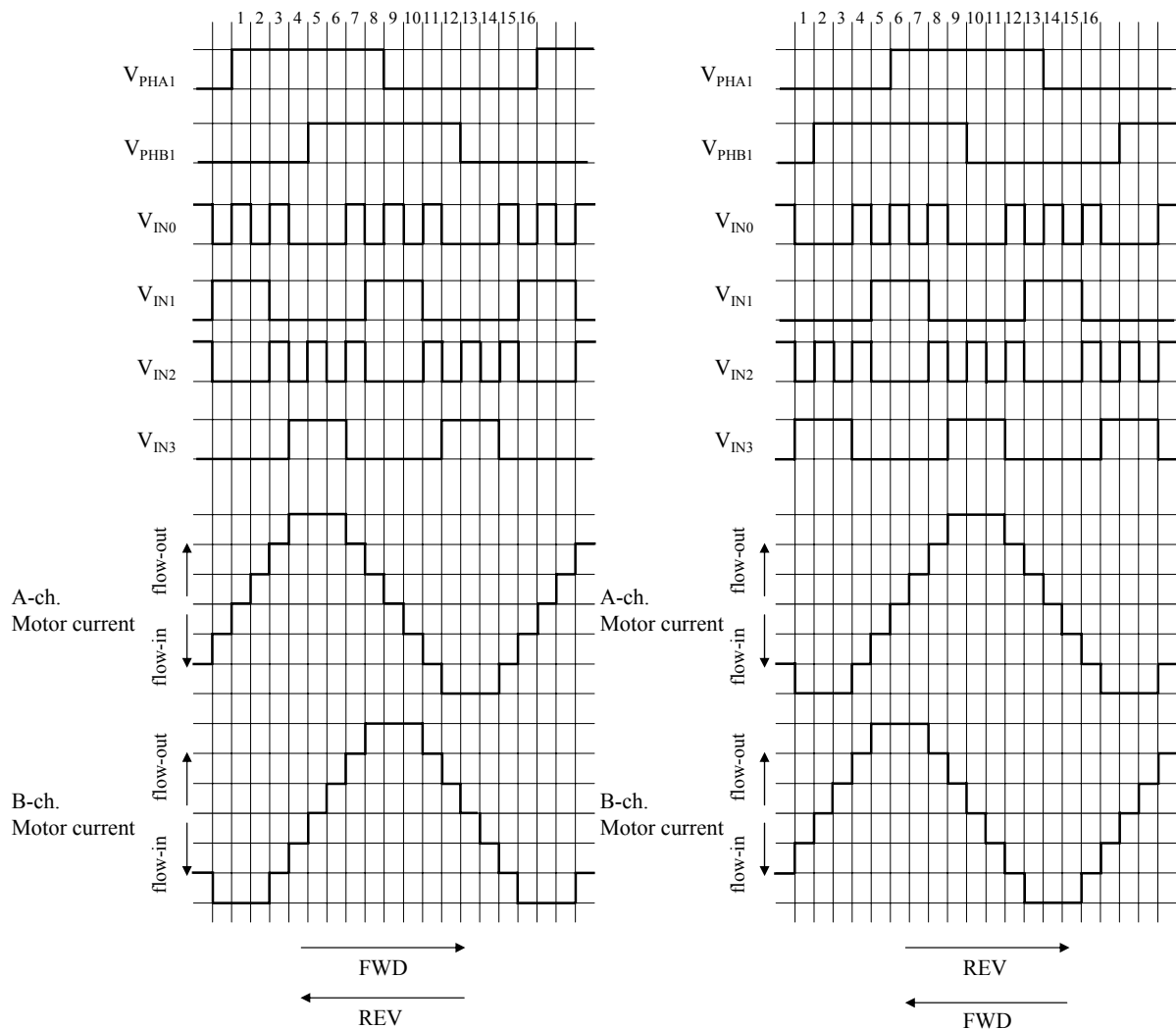
## 4. 1-2 phase excitation (8steps sequence)



## ■ Technical Data (continued)

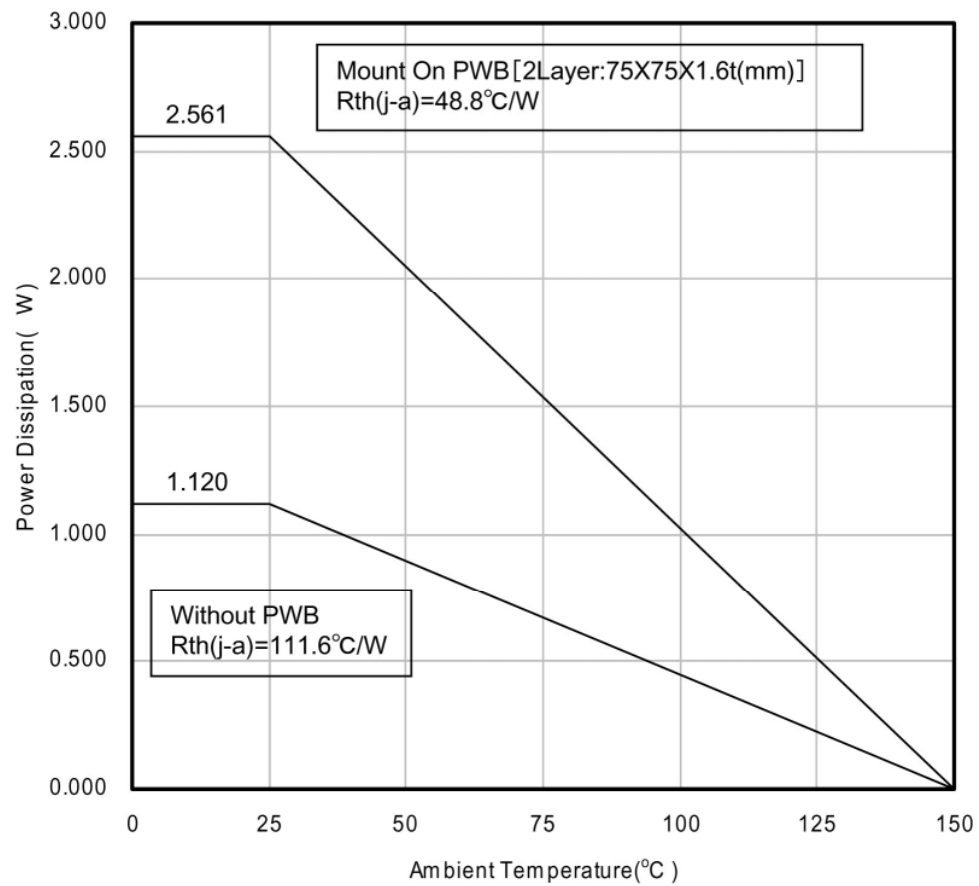
- Control mode (continued)

## 5. W1-2 phase excitation (16steps sequence)



## ■ Technical Data (continued)

- $P_D - T_a$  diagram



## ■ Usage Notes

### • Special attention and precaution in using

1. This IC is intended to be used for general electronic equipment [Stepping motor drive].  
Consult our sales staff in advance for information on the following applications:
  - Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this IC may directly jeopardize life or harm the human body.
  - Any applications other than the standard applications intended.
    - (1) Space appliance (such as artificial satellite, and rocket)
    - (2) Traffic control equipment (such as for automobile, airplane, train, and ship)
    - (3) Medical equipment for life support
    - (4) Submarine transponder
    - (5) Control equipment for power plant
    - (6) Disaster prevention and security device
    - (7) Weapon
    - (8) Others : Applications of which reliability equivalent to (1) to (7) is required
2. Pay attention to the direction of LSI. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might smoke or ignite.
3. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.
4. Perform a visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as a solder-bridge between the pins of the semiconductor device. Also, perform a full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the LSI during transportation.
5. Take notice in the use of this product that it might break or occasionally smoke when an abnormal state occurs such as output pin- $V_{CC}$  short (Power supply fault), output pin-GND short (Ground fault), output-to-output-pin short (load short), or leakage between pins.  
Especially, for the pins below, take notice of Power supply fault, Ground fault, load short, and short to the current detection pins.
  - (1) AOUT1(Pin 17), AOUT2(Pin 15), BOUT1(Pin 14), BOUT2(Pin 12)
  - (2) BC2(Pin 20), VPUMP(Pin 21)
  - (3) VM1(Pin 8), VM2(Pin 22), VCC(Pin 25), S5VOUT(Pin 27)
  - (4) RCSA(Pin 16), RCSB(Pin 13)

And, safety measures such as an installation of fuses are recommended because the extent of the above-mentioned damage and smoke emission will depend on the current capability of the power supply.
6. When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.  
Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.
7. When using the LSI for new models, verify the safety including the long-term reliability for each product.
8. When the application system is designed by using this LSI, be sure to confirm notes in this book.  
Be sure to read the notes to descriptions and the usage notes in the book.
9. Connect the metallic plate (fin) on the back side of the IC with the GND potential. The thermal resistance and the electrical characteristics are guaranteed only when the metallic plate (fin) is connected with the GND potential.

## ■ Usage Notes (continued)

### • Notes of Power LSI

1. Design the heat radiation with sufficient margin so that the allowable value might not be exceeded base on the conditions of power supply voltage, load, and ambient temperature.  
(It is recommended to design the junctions of the IC with 70% to 80% of absolute maximum rating or less.)
2. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.  
Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VM/VCC short (Power supply fault), or output pin to GND short (Ground fault), the LSI might be damaged before the thermal protection circuit could operate.
3. Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the device might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.
4. The product which has specified ASO (Area of Safe Operation) should be operated in ASO.
5. Verify the risks which might be caused by the malfunctions of external components.
6. Set the capacitance between VPUMP and GND so that VPUMP(Pin 21) must not be exceeded 43 V even transiently from motor standby to motor start.
7. This IC employs PWM drive method that switches the output transistor by high-current. Therefore it is apt to generate noises which might cause the IC to malfunction or have fatal damage. To prevent these problems, supply voltage must be stable enough. Take into consideration that the capacitor between VCC and GND is set to minimum 0.1  $\mu\text{F}$  and that between VM and GND is set to minimum 47  $\mu\text{F}$ .  
Moreover, set the capacitors to the IC as closely as possible to avoid malfunctions and damages caused by noises.
8. Pulse blanking time  
In order to prevent mistakes in current detection caused by noises, this IC is provided with pulse blanking time of 0.75  $\mu\text{s}$  (Typ. value). In the result, the motor current will not be less than the current determined by pulse blanking time. Therefore, pay attention to controlling minute current. The Figure 1 shows the relation between the pulse blanking time and minimum current. Increase and decrease in motor current is determined by L value, winding resistance, induced voltage, and PWM ON duty in the motor.

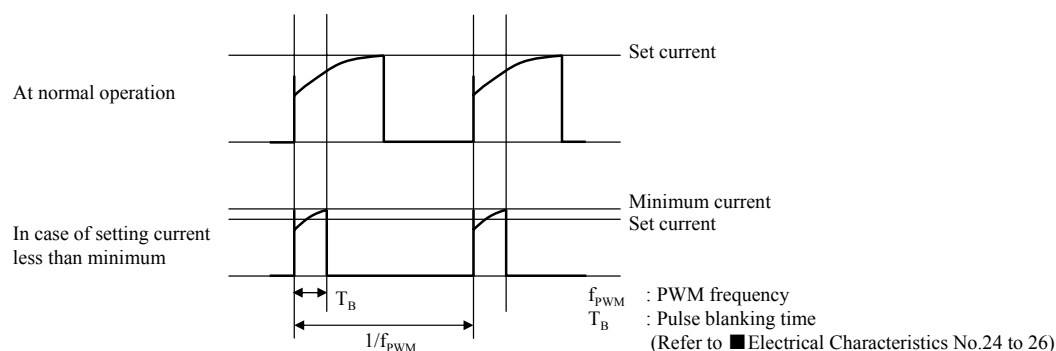


Figure 1. RCS current waveform

## ■ Usage Notes (continued)

### • Notes of Power LSI (continued)

#### 9. VREF voltage

In case of setting VREF voltage to low level, noises might cause malfunctions due to that Comp threshold (SPEC No. 27/28/29 in Page 10) gets low. Under the condition of set VREF voltage, use the IC after checking that malfunctions do not occur.

#### 10. Note of interface

For Pin 1 to 7, Pin 9, Pin 23, 24, and 28, absolute maximum ratings are  $-0.3$  to  $6$  V.

When current is set to high level for a motor and lead line of GND is long, the electric potential of GND of the LSI will be raised. Therefore, take notice that interface pin might get negative to the potential of reference of GND of the LSI though applying  $0$  V to interface pin. Even in this case, pay attention to not exceeding allowable voltage range.

#### 11. PWMSW(Pin 28), PHA1(Pin 1), PHB1(Pin 2)

The current flowing into PEMS, PHA1, and PHB1 changes from that determined by pull-down resistance owing to that parasitic elements in the LSI make the current flow when applying voltage of about  $0.7$  V or more to PWMSW, PHA1, and PHB1 under the condition of shutdown of VCC. The current flowing into PHA1/PHB1/PWMSW is set to  $341.4 \mu\text{A}$  (input impedance : about  $9.1 \text{ k}\Omega$ ) at  $3.3$  V. There is no problem that the voltage up to rating is applied to above-mentioned pins. Nonetheless, it is recommended that the voltage of  $0.7$  V or less is applied to above-mentioned pins at shutdown of VCC.

In addition, in case of the voltage of the above-mentioned pins  $> \text{VCC(Pin 25)} - 0.2$  V at power-on of VCC, the parasitic elements in the LSI also make the current flow and the current flowing into the above-mentioned pins will change (Refer to Figure 2). There is no problem that the voltage up to rating is applied to above-mentioned pins.

Nonetheless, it is recommended to set the voltage applied to the above-mentioned pins to  $4.3$  V or less.

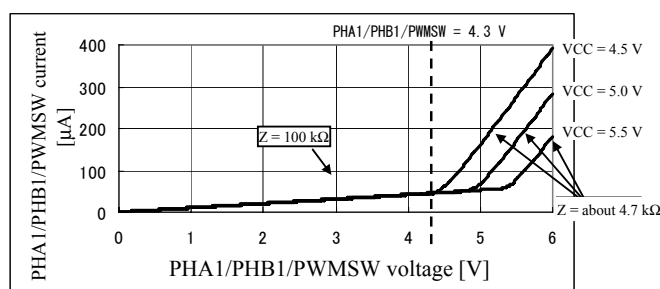
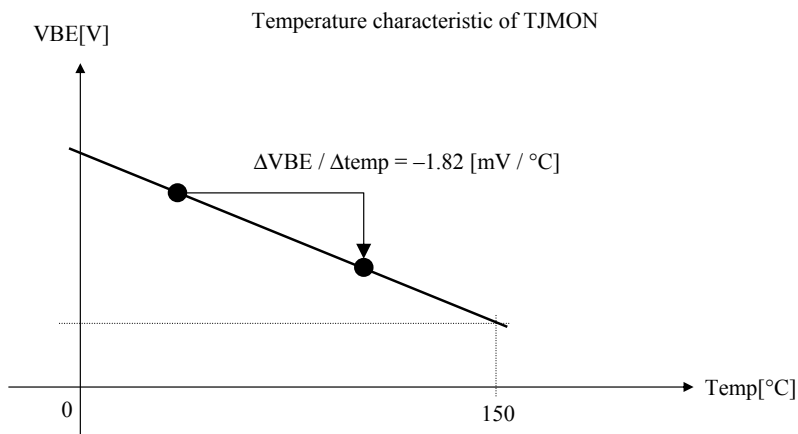


Figure 2. Input impedance of PHA1/PHB1/PWMSW at power-on of VCC

## ■ Usage Notes (continued)

### • Notes of Power LSI (continued)

12. In case of measuring the chip temperature of the IC, measure the voltage of TJMON(Pin 10) and presume the chip temperature from the following data. Use the following data as reference data. Before applying the IC to a product, conduct a sufficient reliability test of the IC along with the evaluation of the product with the IC incorporated



### 13. Power supply sequence

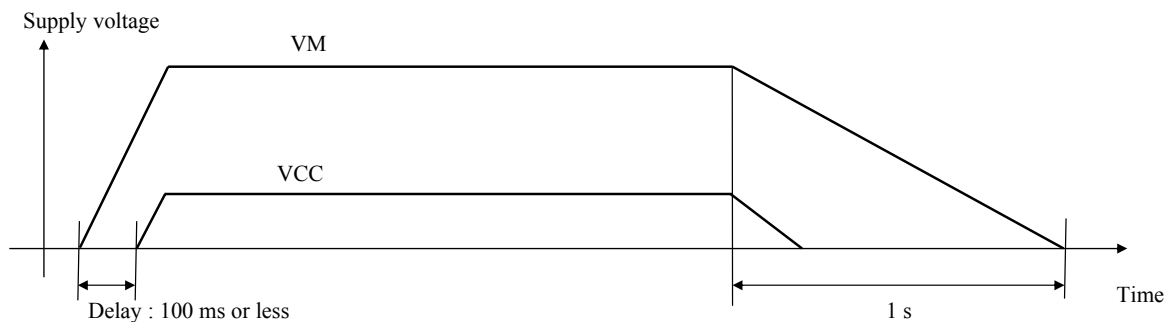
If two type of power supply are used;

Rise : It is recommended to comply with the sequence of [VCC power supply rise] → [VM power supply rise]

Fall : Although there is no particular specification, confirm that VM falls for about 1 s.

If it is difficult to perform the recommended sequence above, design based on the below sequence.

For slew rate of rise, design with [VM : 0.1 V/μs or less, VCC : 0.1 V/μs or less].



If one type of power supply is used;

Slew rate of rise : Design with [VM : 0.1 V/μs or less]

## ■ Usage Notes (continued)

### • Notes of Power LSI (continued)

#### 14. Notes of RCS line

Take the figure and points below into consideration and design PCB pattern.

##### (1) Point 1

Make the wiring to current detection pins (RCSA/RCSB) thick and short, and design so as to lower impedance. Or else current might not be detected properly due to wiring impedance and the current might not be applied to a motor sufficiently.

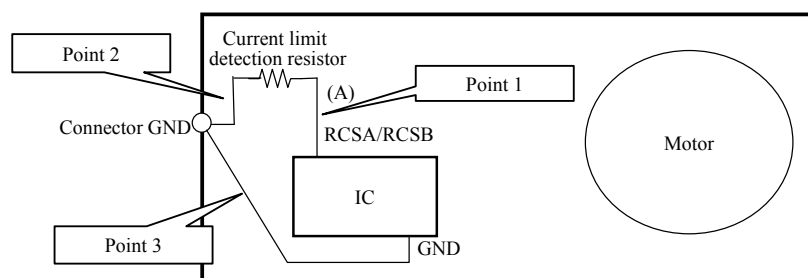
##### (2) Point 2

Make the wiring from current detection resistor shown at Point 2 in the figure below to connector GND thick and short, and design so as to lower impedance. As Point 1, sufficient current might not be applied due to wiring impedance.

Set the wirings on the side of GND of RCSA and RCSB independently because peak detection might not be detected properly if there is a common impedance on the side of GND of RCSA and RCSB.

##### (3) Point 3

Connect GND of the IC to a connector on the PBC independently. Set the wiring where current detection resistor with high current line is removed (Point 2) apart from the GND wiring of the IC and make them shorted at a point as shown in the below figure. That can minimize the fluctuation of GND of the IC.



15. A high current flows into the IC. Therefore, the common impedance of the PCB pattern cannot be ignored. Take the following points into consideration and design the PCB pattern of the motor.

A high current flows into the line between the VM1(Pin 8) and VM2(Pin 22). Therefore, noise is generated with ease when switching at the inductance (L) of the line, which may result in the malfunctioning or destruction of the IC (Figure 3).

As shown in Figure 4, the escape way of the noise is secured by connecting the capacitor to the connector from VM pin of the IC. This makes it possible to suppress the direct VM pin voltage of the IC. Make the settings based on Figure 4 as much as possible.

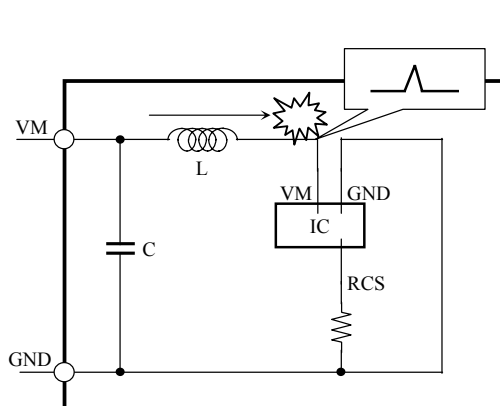


Figure 3. Non-recommended pattern

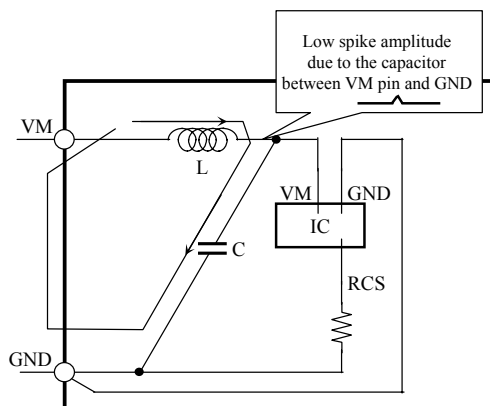


Figure 4. Recommended pattern

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