International
IOR Rectifier

Preliminary Data Sheet No. PD60083-K

(NOTE: For new designs, we recommend the IR53H(D)420-P)

IR51H(D)224
IR51H(D)320
IR51H(D)420

SELF-OSCILLATING HALF BRIDGE

Features

- Output Power MOSFETs in half-bridge configuration
- High side gate drive designed for bootstrap operation
- Bootstrap diode integrated into package (HD type)
- Accurate timing control for both Power MOSFETs
  - Matched delay to get 50% duty cycle
  - Matched deadtime of 1.2us
- Internal oscillator with programmable frequency

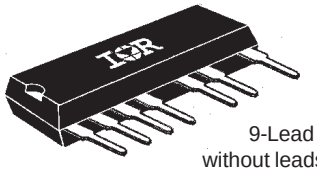
$$f = \frac{1}{1.4 \times (R_T + 75\Omega) \times C_T}$$

- 15.6V Zener clamped Vcc for offline operation
- Half-bridge output is out of phase with R_T
- Micropower startup

Product Summary

V_{IN} (max)	250V (IR51H(D)224) 400V (IR51H(D)320) 500V (IR51H(D)420)
Duty Cycle	50%
Deadtime	1.2µs
$R_{ds(on)}$	1.1Ω (IR51H(D)224) 3.0Ω (IR51H(D)320) 3.6Ω (IR51H(D)420)
P_D (T_A = 25oC)	2.0W

Package

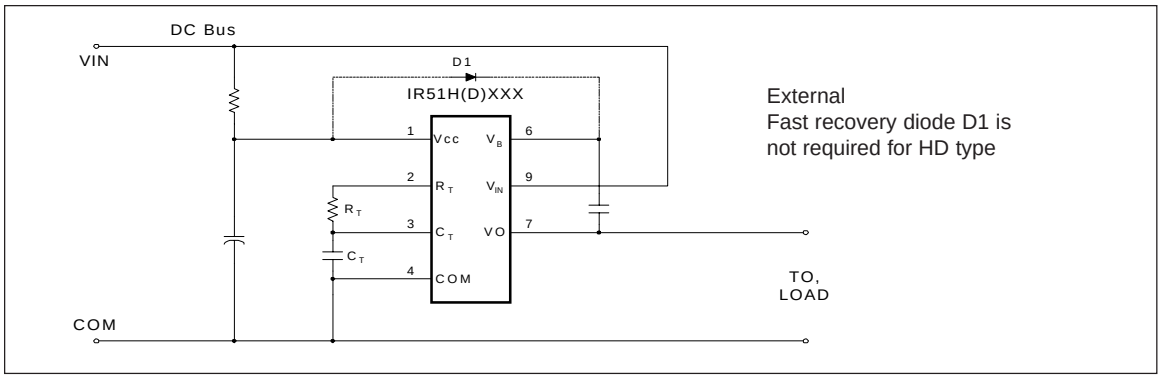


9-Lead SIP
without leads 5 and 8

Description

The IR51H(D)XXX are complete high voltage, high speed, self-oscillating half-bridge circuits. Proprietary HVIC and latch immune CMOS technologies, along with the HEXFET® power MOSFET technology, enable ruggedized single package construction. The front-end features a programmable oscillator which functions similar to the CMOS 555 timer. The supply to the control circuit has a zener clamp to simplify offline operation. The output features two HEXFETs in a half-bridge configuration with an internally set deadtime designed for minimum cross-conduction in the half-bridge. Propagation delays for the high and low side power MOSFETs are matched to simplify use in 50% duty cycle applications. The device can operate up to 500 volts.

Typical Connection



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Minimum	Maximum	Units
V_{IN}	High voltage supply	-224	- 0.3	250	V
		-320	- 0.3	400	
		-420	- 0.3	500	
V_B	High side floating supply		Vo - 0.3	Vo +2.5	
V_O	Half-bridge output		-0.3	V_{IN} + 0.3	
V_{RT}	R_T voltage		- 0.3	V_{cc} + 0.3	
V_{CT}	C_T voltage		- 0.3	V_{cc} + 0.3	
I_{cc}	Supply current (note 1)		—	25	mA
I_{RT}	R_T output current		- 5	5	
dV/dt	Peak diode recovery		—	3.5	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$		—	2.00	W
Rth_{JA}	Thermal resistance, junction to ambient		—	60	°C/W
T_J	Junction temperature		-55	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

NOTE 1:

This IC contains a zener clamp structure between V_{CC} and COM which has a nominal breakdown voltage of 15.6V. Please note that this supply pin should not be driven by a DC, low impedance power source greater than the V_{CLAMP} specified in the Electrical Characteristics Section

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation, the device should be used within the recommended conditions.

Symbol	Definition		Minimum	Maximum	Units
V_B	High side floating supply absolute voltage		V_O + 10	V_O + V_{clamp}	V
V_{IN}	High voltage supply	-224	—	250	
		-320	—	400	
		-420	—	500	
V_O	Half-bridge output voltage		-3.0 (note 2)	V_{IN}	
I_D	Continuous drain current (T_A = 25°C)	-224	—	1.1	A
		-320	—	0.9	
		-420	—	0.7	
	(T_A = 85°C)	-224	—	0.7	
		-320	—	0.6	
		-420	—	0.5	
I_{CC}	Supply current		(note 3)	5	mA
T_A	Ambient temperature		-40	125	°C

NOTE 2:

Care should be taken to avoid switching conditions where the V_S node flies inductively below ground by more than 5V.

NOTE 3:

Enough current should be supplied to the V_{CC} lead of the IC to keep the internal 15.6V zener diode clamping the voltage at this lead.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 12V, T_A = 25°C unless otherwise specified.

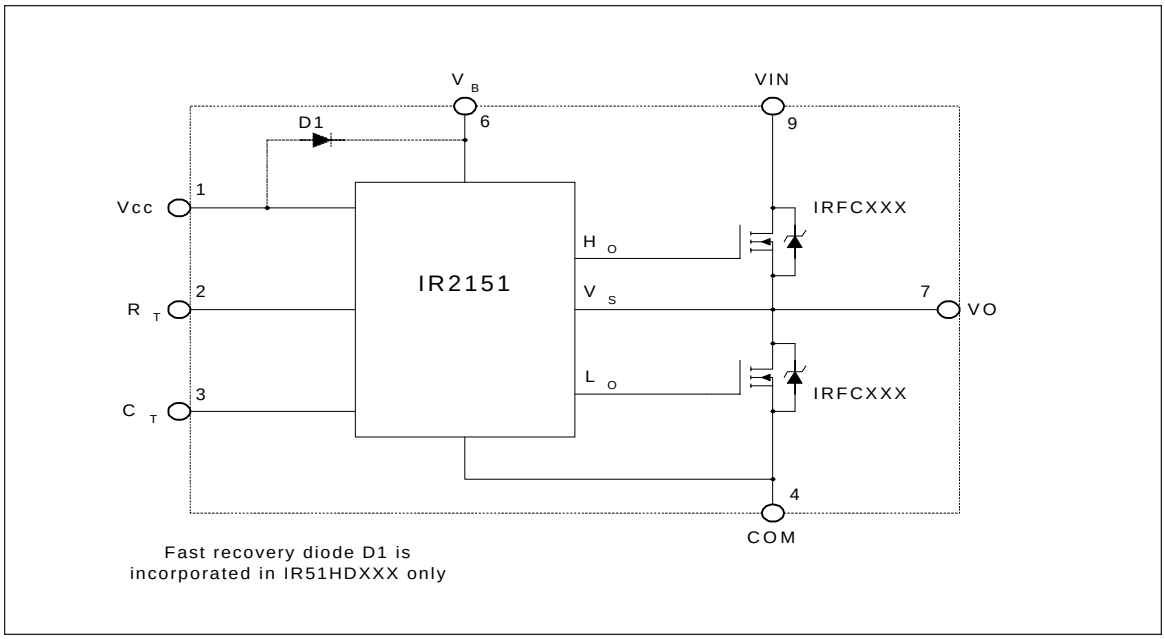
Symbol	Definition		Min.	Typ.	Max.	Units	Test Conditions	
t_{rr}	Reverse recovery time (MOSFET body diode)	-224	—	200	—	ns	I_F=1.1A	di/dt =100 A/µs
		-320	—	270	—		I_F=900mA	
		-420	—	240	—		I_F=700mA	
Q_{rr}	Reverse recovery charge (MOSFET body diode)	-224	—	0.7	—	µC	I_F=1.1A	
		-320	—	0.6	—		I_F=900mA	
		-420	—	0.5	—		I_F=700mA	
D	R_T duty cycle		—	50	—	%	fosc = 20 kHz	

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_B) = 12V, T_A = 25°C unless otherwise specified.

Symbol	Definition		Min.	Typ.	Max.	Units	Test Conditions	
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold		—	8.4	—	V		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold		—	8.0	—	V		
I_{QCC}	Quiescent V_{CC} supply current		—	300	—	µA	V_{CC} > V_{CCUV}	
V_{CLAMP}	V_{CC} zener shunt clamp voltage		—	15.6	—	V	I_{CC} = 5mA	
I_{QBS}	Quiescent V_{BS} supply current		—	30	—	µA		
I_{OS}	Offset supply leakage current		—	—	50		V_B = V_{IN} = 500V	
f_{OSC}	Oscillator frequency		—	20	—	kHz	R_T = 35.7 kΩ C_T = 1 nF	
			—	100	—		R_T = 7.04 kΩ C_T = 1 nF	
I_{CT}	C_T input current		—	0.001	1.0	µA		
V_{CTUV}	C_T undervoltage lockout		—	100	—	mV	Note 2	
V_{RT+}	R_T high level output voltage, V_{CC} - R_T		— —	20 200	— —		I_{RT} = 100µA I_{RT} = -1mA	
V_{RT-}	R_T low level output voltage		— —	20 200	— —		I_{RT} = 100µA I_{RT} = -1mA	
V_{RTUV}	R_T undervoltage lockout, V_{CC} - R_T		—	100	—		I_{RT} = 100µA	
V_{CT+}	2/3 V_{CC} threshold		—	8.0	—	kHz		
V_{CT-}	1/3 V_{CC} threshold		—	4.0	—			
Rds(on)	Static-drain-to-source on-resistance	-224	—	1.1	—	Ω	I_F=1.1A	di/dt =100 A/µs
		-320	—	1.8	—		I_F=900mA	
		-420	—	3.0	—		I_F=700mA	
V_{SD}	Diode forward voltage	-224	—	0.85	—	V	I_F=1.1A	
		-320	—	0.7	—		I_F=900mA	
		-420	—	0.8	—		I_F=700mA	

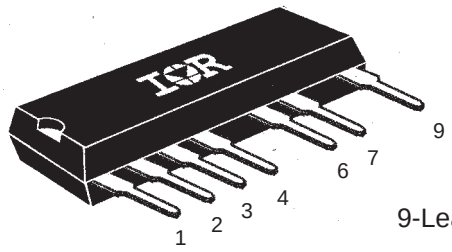
Functional Block Diagram



Lead Definitions

Symbol	Lead Description
V_{CC}	Logic and internal gate drive supply voltage. An internal zener clamp diode at 15.6 V nominal is included to allow the V_{CC} to be current fed directly from VIN typically by means of a high value resistor.
R_T	Oscillator timing resistor output; a resistor is connected from R_T to C_T. RT is out of phase with the half-bridge output (VO).
C_T	Oscillator timing capacitor input; a capacitor is connected from C_T to COM in order to program the oscillator frequency according to the following equation: $$f = \frac{1}{1.4 \times (R_T + 75\Omega) \times C_T}$$ C_T PIN also invokes shutdown function (see note 2) where 75Ω is the effective impedence of the R_T output stage.
V_B	High side gate drive floating supply. For bootstrap operation a high voltage fast recovery diode is needed to feed from V_{CC} to V_B. (HD type circuits incorporate this diode).
V_{IN}	High voltage supply
VO	Half Bridge output
COM	Logic and low side of half bridge return

Lead Assignments



1	V_{CC}	6	V_B
2	R_T	7	VO
3	C_T	9	V_{IN}
4	COM		

9-Lead SIP without Leads 5 and 8

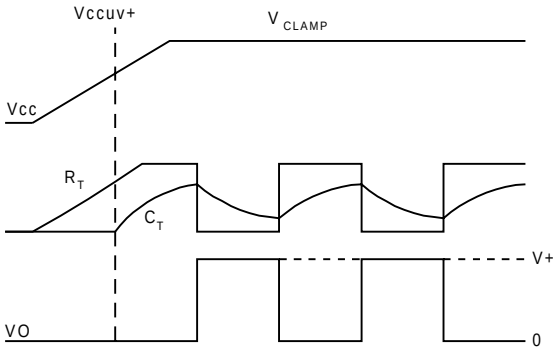
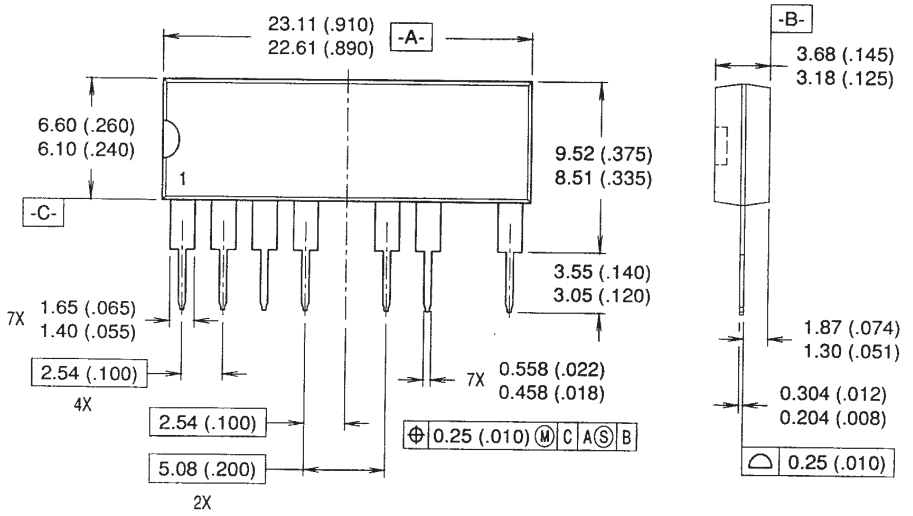


Figure 1. Input/Output Timing Diagram

Case outline



NOTES:
1. Dimensioning and tolerancing per ANSI Y14.5M-1982
2. Controlling Dimension: INCH
3. Dimensions are shown in millimeters (inches)

9-Lead SIP w/o leads 5 and 8