

FDMS8690

N-Channel Power Trench® MOSFET

30V, 27A, 9.0mΩ

Features

- Max $r_{DS(on)}$ = 9.0mΩ at $V_{GS} = 10V$, $I_D = 14.0A$
- Max $r_{DS(on)}$ = 12.5mΩ at $V_{GS} = 4.5V$, $I_D = 11.5A$
- High performance trench technology for extremely low $r_{DS(on)}$ and gate charge
- Minimal Qgd (2.9nC typical)
- RoHS Compliant

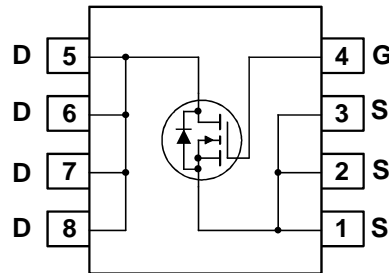
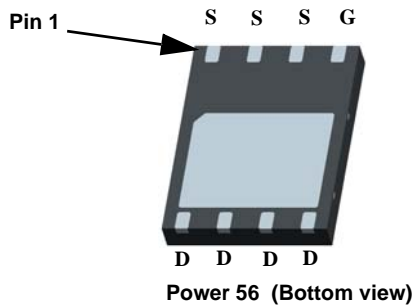


General Description

This device has been designed specifically to improve the efficiency of DC/DC converters. Using new techniques in MOSFET construction, the various components of gate charge and capacitance have been optimized to reduce switching losses. Low gate resistance and very low Miller charge enable excellent performance with both adaptive and fixed dead time gate drive circuits. Very low $r_{DS(on)}$ has been maintained to provide an extremely versatile device.

Application

- High Efficiency DC-DC converters.
- Notebook CPU power supply
- Multi purpose Point of Load



MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current -Continuous (Package limited) $T_C = 25^\circ\text{C}$	27	A
	-Continuous (Silicon limited) $T_C = 25^\circ\text{C}$	52	
	-Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	14	
	-Pulsed	100	
P_D	Power Dissipation $T_C = 25^\circ\text{C}$	37.8	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.3	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS8690	FDMS8690	Power 56	13"	12mm	3000 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, referenced to 25°C		34		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{V}, V_{GS} = 0\text{V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$			± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	1	1.6	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, referenced to 25°C		-4.5		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 14.0\text{A}$		7.4	9.0	m Ω
		$V_{GS} = 4.5\text{V}, I_D = 11.5\text{A}$		9.9	12.5	
		$V_{GS} = 10\text{V}, I_D = 14.0\text{A}, T_J = 125^\circ\text{C}$		10.6	13.3	

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 15\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$		1260	1680	pF
C_{oss}	Output Capacitance			535	715	pF
C_{rss}	Reverse Transfer Capacitance			80	120	pF
R_g	Gate Resistance		$f = 1\text{MHz}$		1.1	5.0

Switching Characteristics

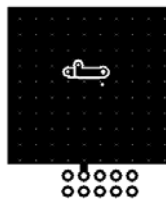
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{V}, I_D = 1.0\text{A}$ $V_{GS} = 10\text{V}, R_{GEN} = 6\Omega$		8	16	ns
t_r	Rise Time			1.8	10	ns
$t_{d(off)}$	Turn-Off Delay Time			26	42	ns
t_f	Fall Time			19	35	ns
$Q_{g(TOT)}$	Total Gate Charge at 10V		$V_{GS} = 0\text{V to } 10\text{V}$	$V_{DD} = 15\text{V}$ $I_D = 14.0\text{A}$	18.8	27
$Q_{g(5)}$	Total Gate Charge at 5V	$V_{GS} = 0\text{V to } 5\text{V}$	10		14	nC
Q_{gs}	Gate to Source Gate Charge		3.5			nC
Q_{gd}	Gate to Drain "Miller" Charge		2.9			nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 2.1\text{A}$ (Note 2)		0.7	1.2	V
t_{rr}	Reverse Recovery Time	$I_F = 14.0\text{A}, di/dt = 100\text{A}/\mu\text{s}$			45	ns
Q_{rr}	Reverse Recovery Charge				33	nC

Notes:

1: $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a $1.5 \times 1.5\text{in.}$ board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $50^\circ\text{C}/\text{W}$ when mounted on a 1in^2 pad of 2 oz copper



b. $125^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper

2: Pulse Test: Pulse Width < $300\mu\text{s}$, Duty cycle < 2.0%.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

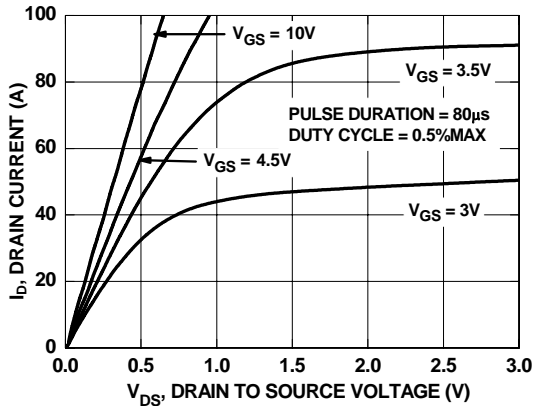


Figure 1. On-Region Characteristics

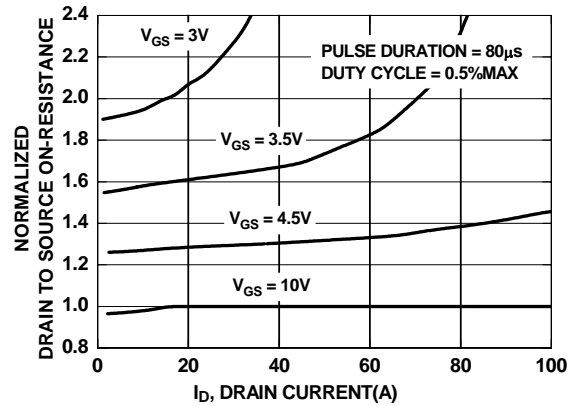


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

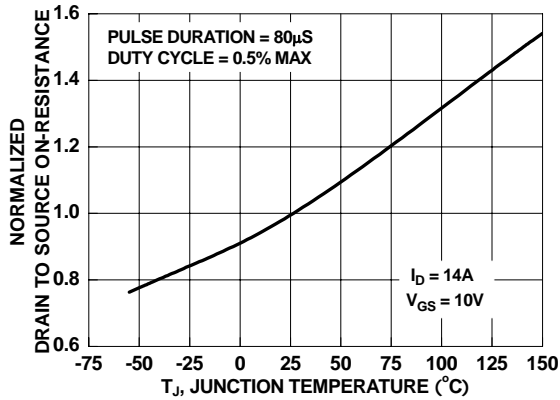


Figure 3. Normalized On-Resistance vs Junction Temperature

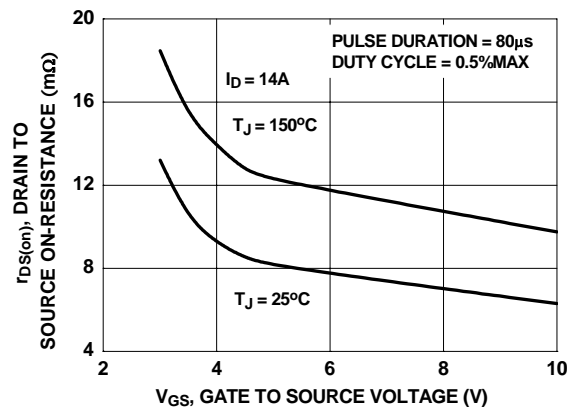


Figure 4. On-Resistance vs Gate to Source Voltage

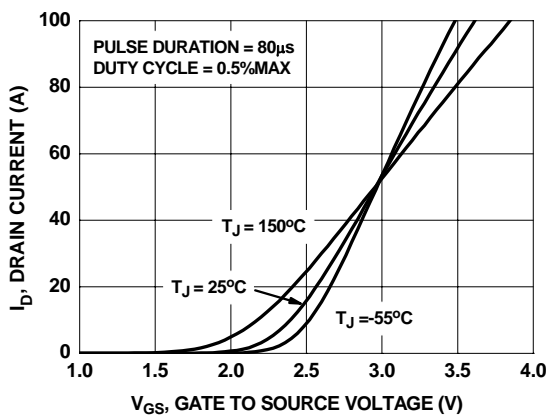


Figure 5. Transfer Characteristics

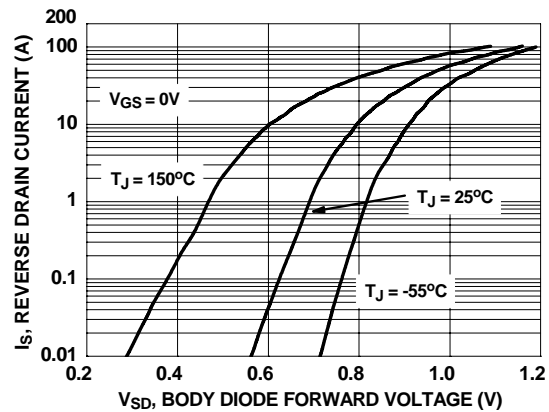


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

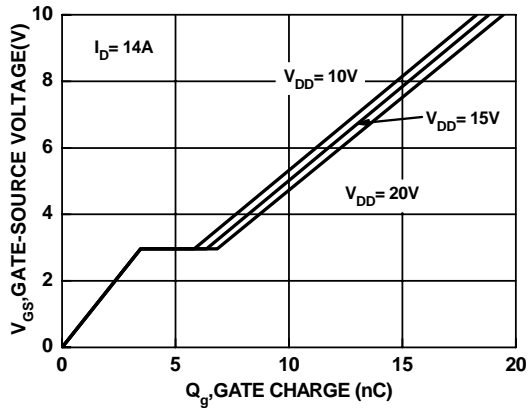


Figure 7. Gate Charge Characteristics

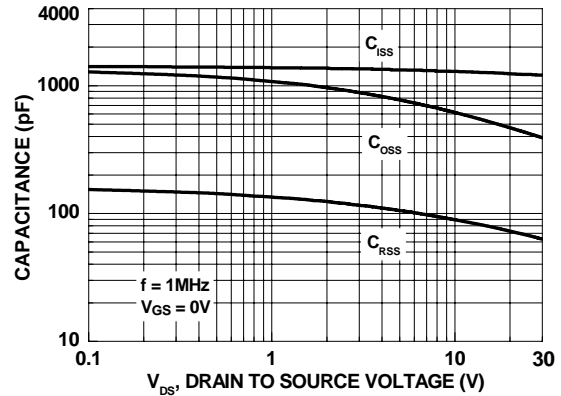


Figure 8. Capacitance vs Drain to Source Voltage

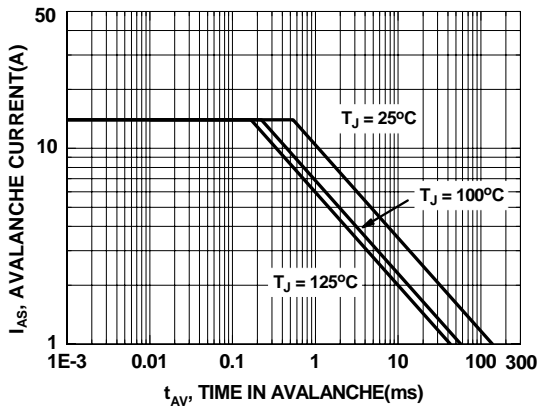


Figure 9. Unclamped Inductive Switching Capability

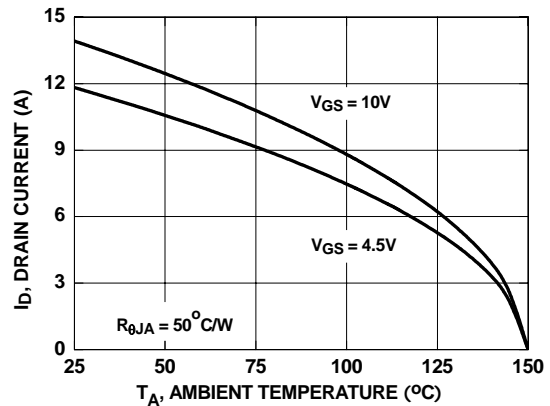


Figure 10. Maximum Continuous Drain Current vs Ambient Temperature

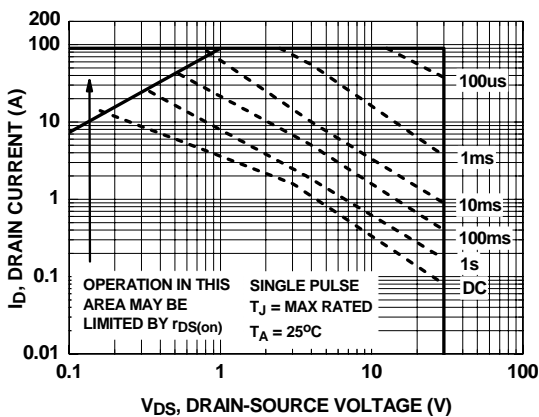


Figure 11. Forward Bias Safe Operating Area

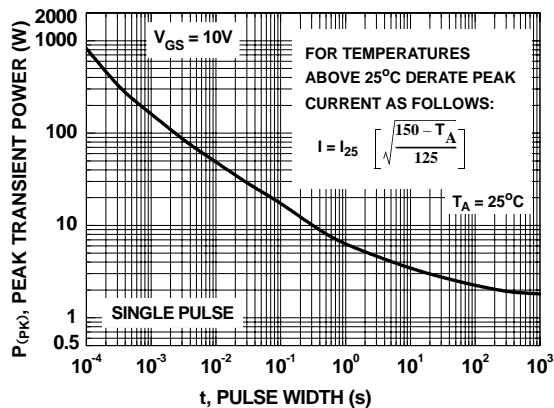


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

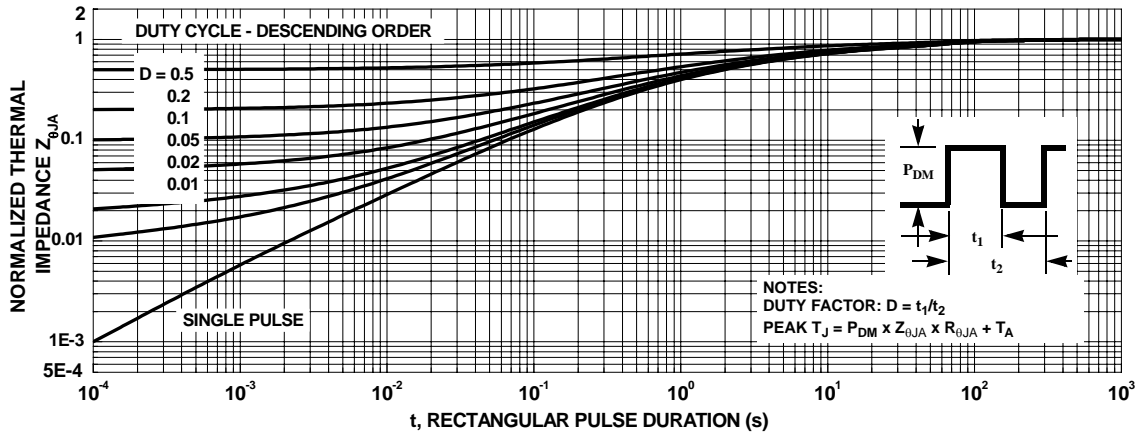
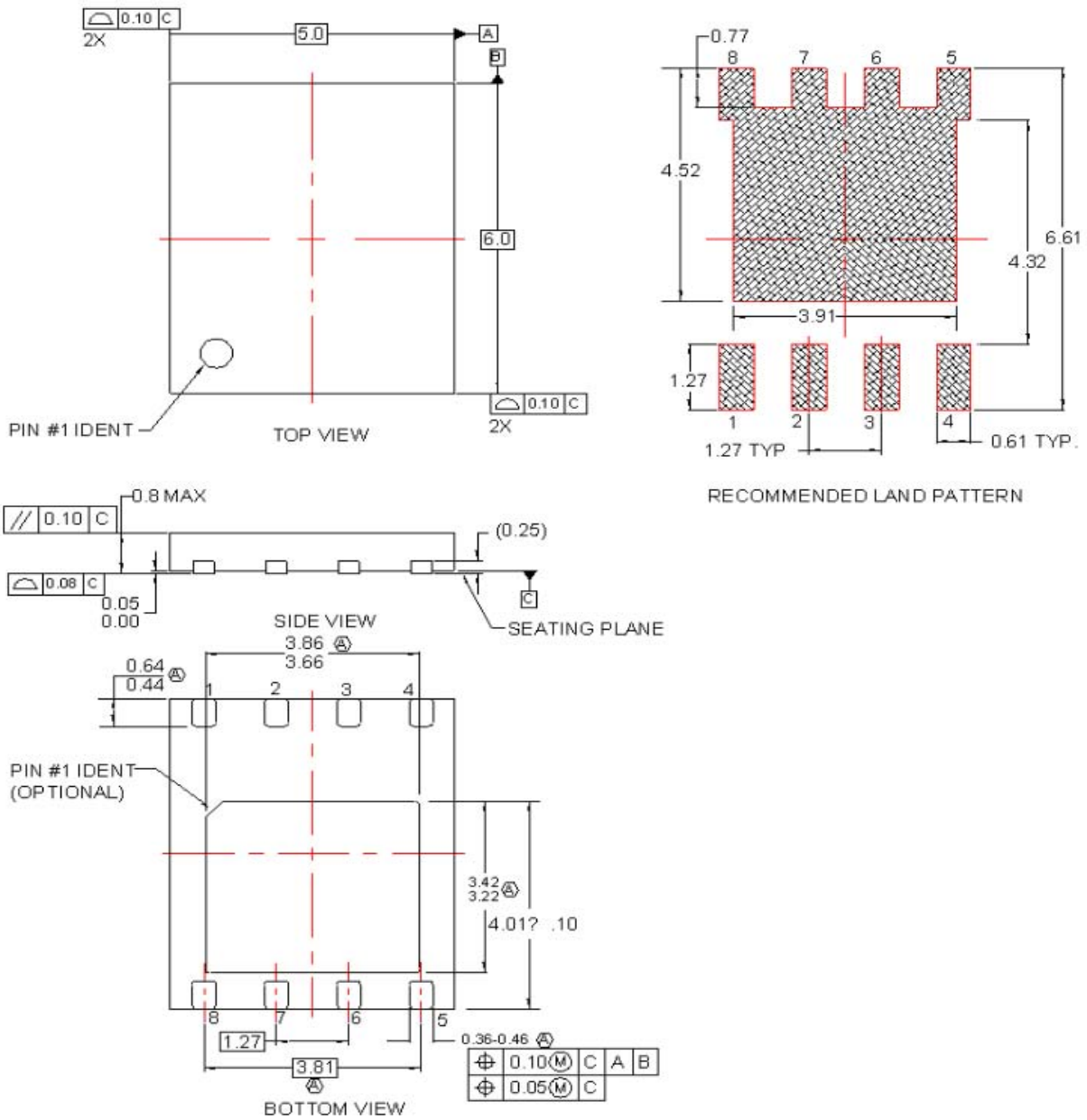


Figure 13. Transient Thermal Response Curve



NOTES:


- (A) DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229, DATED 11/2001.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- D. TERMINALS 5,6,7 AND 8 ARE TIED TO THE EXPOSED PADDLE

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