

NCV8440

Protected Power MOSFET

2.6 A, 52 V, N-Channel, Logic Level, Clamped MOSFET w/ ESD Protection

Benefits

- High Energy Capability for Inductive Loads
- Low Switching Noise Generation

Features

- Diode Clamp Between Gate and Source
- ESD Protection – HBM 5000 V
- Active Over-Voltage Gate to Drain Clamp
- Scalable to Lower or Higher $R_{DS(on)}$
- Internal Series Gate Resistance
- These are Pb-Free Devices

Applications

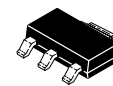
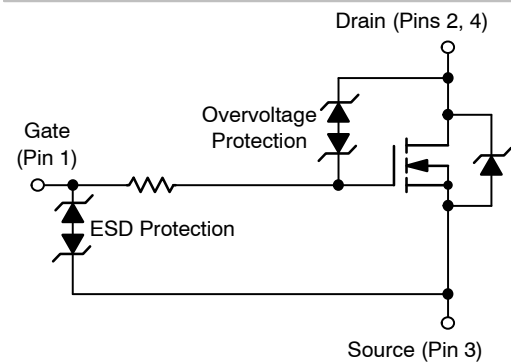
- Automotive and Industrial Markets:
Solenoid Drivers, Lamp Drivers, Small Motor Drivers
- NCV Prefix for Automotive and Other Applications Requiring Site and Control Changes



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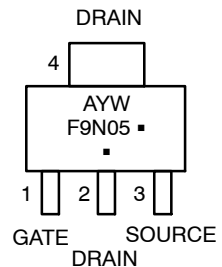
V_{DSS} (Clamped)	$R_{DS(on)}$ TYP	I_D MAX
52 V	95 mΩ @ 10 V	2.6 A



SOT-223
CASE 318E
STYLE 3

- 1 = Gate
- 2 = Drain
- 3 = Source

MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NCV8440STT1G	SOT-223 (Pb-Free)	1000/Tape & Reel
NCV8440STT3G	SOT-223 (Pb-Free)	4000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NCV8440

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage Internally Clamped	V_{DSS}	52-59	V
Gate-to-Source Voltage – Continuous	V_{GS}	± 15	V
Drain Current – Continuous @ $T_A = 25^\circ\text{C}$ – Single Pulse ($t_p = 10 \mu\text{s}$) (Note 1)	I_D	2.6	A
	I_{DM}	10	A
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 1)	P_D	1.69	W
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy ($V_{DD} = 50 \text{ V}$, $I_{D(pk)} = 1.17 \text{ A}$, $V_{GS} = 10 \text{ V}$, $L = 160 \text{ mH}$, $R_G = 25 \Omega$)	E_{AS}	110	mJ
Thermal Resistance, Junction-to-Ambient (Note 1) Junction-to-Ambient (Note 2)	$R_{\theta JA}$	74	$^\circ\text{C/W}$
	$R_{\theta JA}$	169	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 10 Seconds	T_L	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. When surface mounted to a FR4 board using 1" pad size, (Cu area 1.127 in²).
2. When surface mounted to a FR4 board using minimum recommended pad size, (Cu area 0.412 in²).

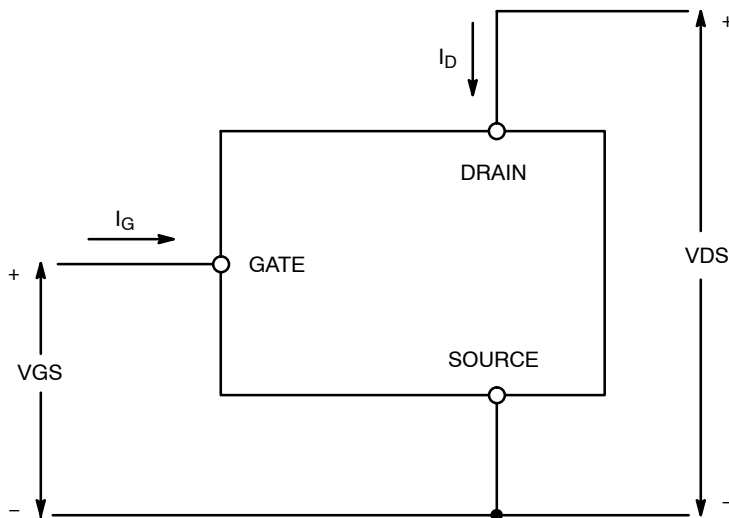


Figure 1. Voltage and Current Convention

NCV8440

MOSFET ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 3) ($V_{GS} = 0\text{ V}$, $I_D = 1.0\text{ mA}$, $T_J = 25^\circ\text{C}$) ($V_{GS} = 0\text{ V}$, $I_D = 1.0\text{ mA}$, $T_J = -40^\circ\text{C}$ to 125°C) Temperature Coefficient (Negative)	$V_{(BR)DSS}$	52 50.8	55 54 -9.3	59 59.5	V V mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current ($V_{DS} = 40\text{ V}$, $V_{GS} = 0\text{ V}$) ($V_{DS} = 40\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125^\circ\text{C}$)	I_{DSS}			10 25	μA
Gate-Body Leakage Current ($V_{GS} = \pm 8\text{ V}$, $V_{DS} = 0\text{ V}$) ($V_{GS} = \pm 14\text{ V}$, $V_{DS} = 0\text{ V}$)	I_{GSS}		± 35	± 10	μA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (Note 3) ($V_{DS} = V_{GS}$, $I_D = 100\text{ }\mu\text{A}$) Threshold Temperature Coefficient (Negative)	$V_{GS(th)}$	1.1	1.5 -4.1	1.9	V mV/ $^\circ\text{C}$
Static Drain-to-Source On-Resistance (Note 3) ($V_{GS} = 3.5\text{ V}$, $I_D = 0.6\text{ A}$) ($V_{GS} = 4.0\text{ V}$, $I_D = 1.5\text{ A}$) ($V_{GS} = 10\text{ V}$, $I_D = 2.6\text{ A}$)	$R_{DS(on)}$		135 150 95	180 160 110	m Ω
Forward Transconductance (Note 3) ($V_{DS} = 15\text{ V}$, $I_D = 2.6\text{ A}$)	g_{FS}		3.8		Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	$V_{DS} = 35\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 10\text{ kHz}$	C_{iss}		155		μF
Output Capacitance		C_{oss}		60		
Transfer Capacitance		C_{rss}		25		
Input Capacitance	$V_{DS} = 25\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 10\text{ kHz}$	C_{iss}		170		μF
Output Capacitance		C_{oss}		70		
Transfer Capacitance		C_{rss}		30		

- Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.
- Switching characteristics are independent of operating junction temperatures.

NCV8440

MOSFET ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS (Note 4)						
Turn-On Delay Time	$V_{GS} = 4.5\text{ V}, V_{DD} = 40\text{ V},$ $I_D = 2.6\text{ A}, R_D = 15.4\ \Omega$	$t_{d(on)}$		375		ns
Rise Time		t_r		1525		
Turn-Off Delay Time		$t_{d(off)}$		1530		
Fall Time		t_f		1160		
Turn-On Delay Time	$V_{GS} = 4.5\text{ V}, V_{DD} = 40\text{ V},$ $I_D = 1.0\text{ A}, R_D = 40\ \Omega$	$t_{d(on)}$		325		ns
Rise Time		t_r		1275		
Turn-Off Delay Time		$t_{d(off)}$		1860		
Fall Time		t_f		1150		
Turn-On Delay Time	$V_{GS} = 10\text{ V}, V_{DD} = 15\text{ V},$ $I_D = 2.6\text{ A}, R_D = 5.8\ \Omega$	$t_{d(on)}$		190		ns
Rise Time		t_r		710		
Turn-Off Delay Time		$t_{d(off)}$		2220		
Fall Time		t_f		1180		
Gate Charge	$V_{GS} = 4.5\text{ V}, V_{DS} = 40\text{ V},$ $I_D = 2.6\text{ A (Note 3)}$	Q_T		4.5		nC
		Q_1		0.9		
		Q_2		2.6		
Gate Charge	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V},$ $I_D = 1.5\text{ A (Note 3)}$	Q_T		3.9		nC
		Q_1		1.0		
		Q_2		1.7		

SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	$I_S = 2.6\text{ A}, V_{GS} = 0\text{ V (Note 3)}$ $I_S = 2.6\text{ A}, V_{GS} = 0\text{ V}, T_J = 125^\circ\text{C}$	V_{SD}		0.81 0.66	1.5	V
Reverse Recovery Time	$I_S = 1.5\text{ A}, V_{GS} = 0\text{ V},$ $di_S/dt = 100\text{ A}/\mu\text{s (Note 3)}$	t_{rr}		730		ns
		t_a		200		
		t_b		530		
Reverse Recovery Stored Charge		Q_{RR}		6.3		μC

ESD CHARACTERISTICS

Electro-Static Discharge Capability	Human Body Model (HBM)	ESD	5000			V
	Machine Model (MM)		500			

3. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

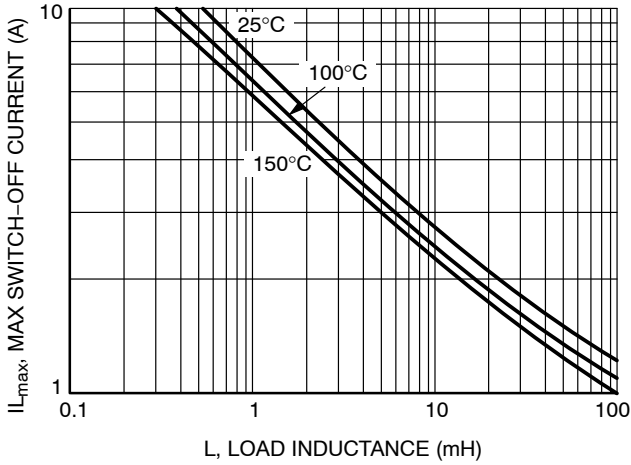


Figure 1. Single Pulse Maximum Switch-off Current vs. Load Inductance

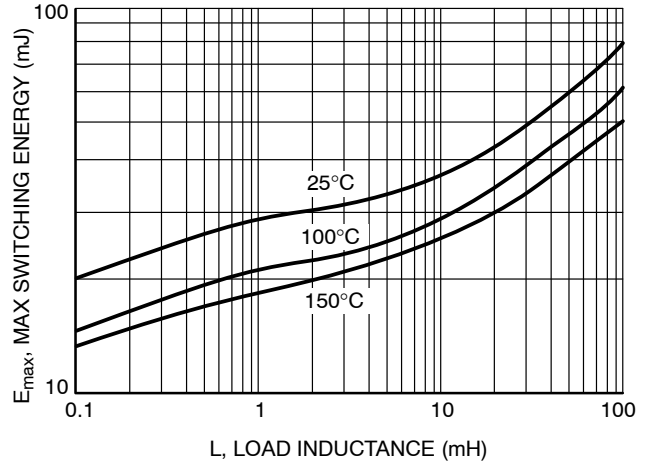


Figure 2. Single Pulse Maximum Switching Energy vs. Load Inductance

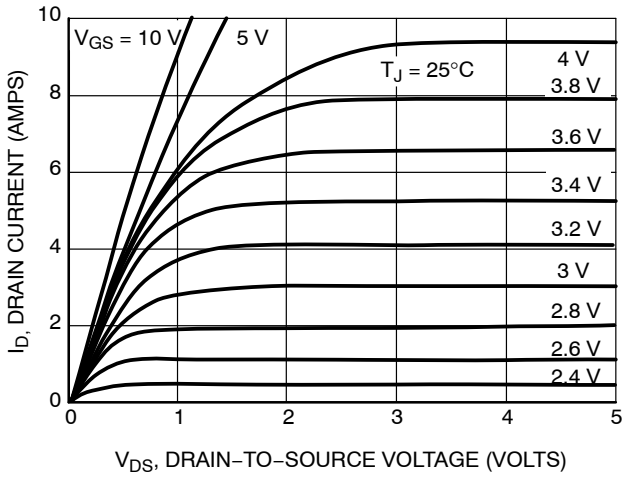


Figure 3. On-State Output Characteristics

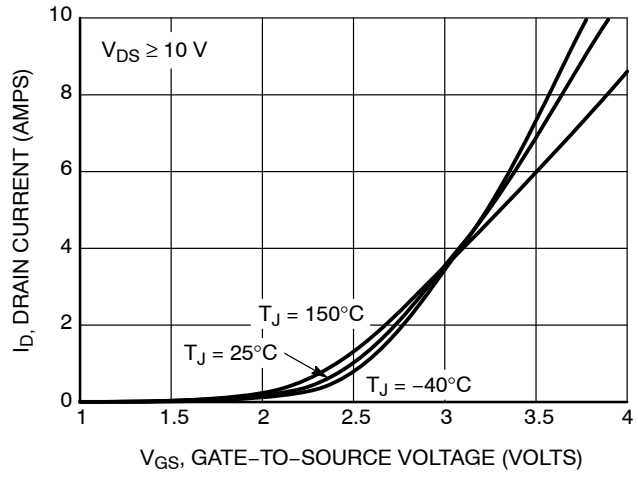


Figure 4. Transfer Characteristics

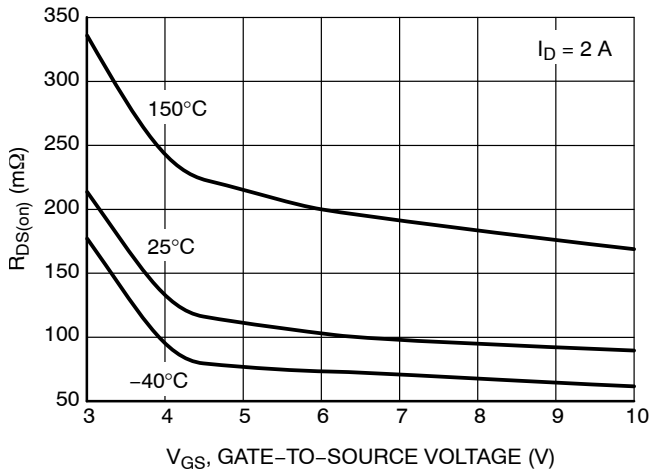


Figure 5. $R_{DS(on)}$ vs. Gate-Source Voltage

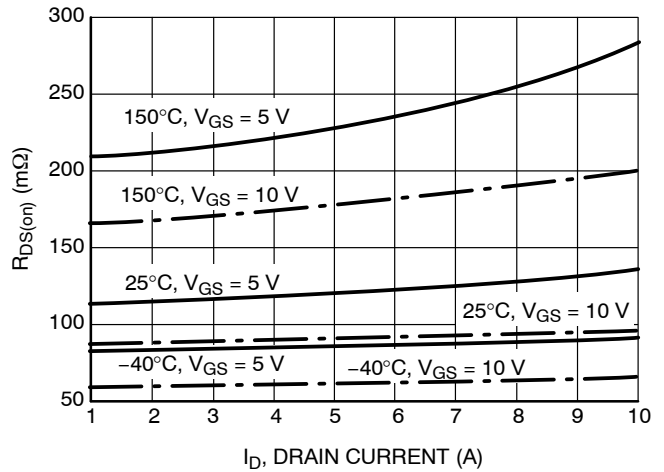


Figure 6. $R_{DS(on)}$ vs. Drain Current

TYPICAL PERFORMANCE CURVES

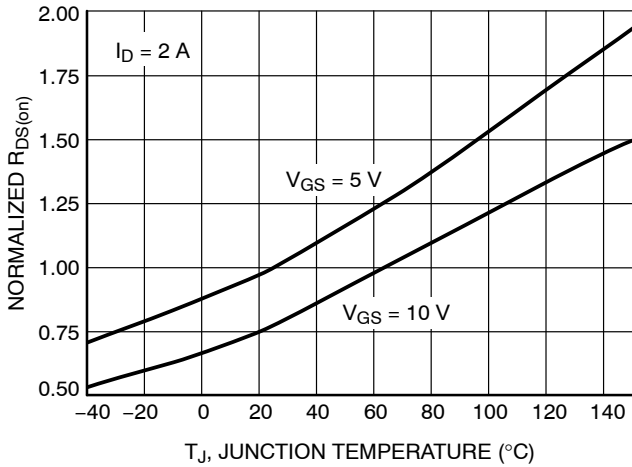


Figure 7. Normalized $R_{DS(on)}$ vs. Temperature

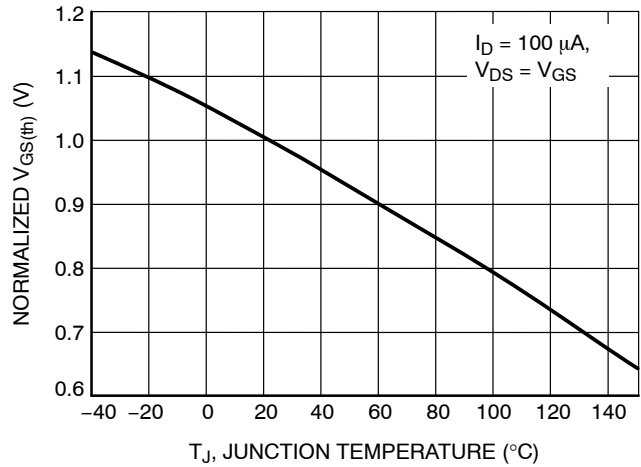


Figure 8. Normalized Threshold Voltage vs. Temperature

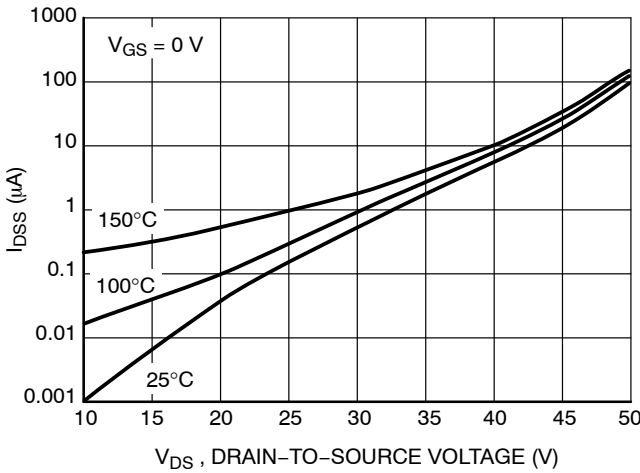


Figure 9. Drain-to-Source Leakage Current

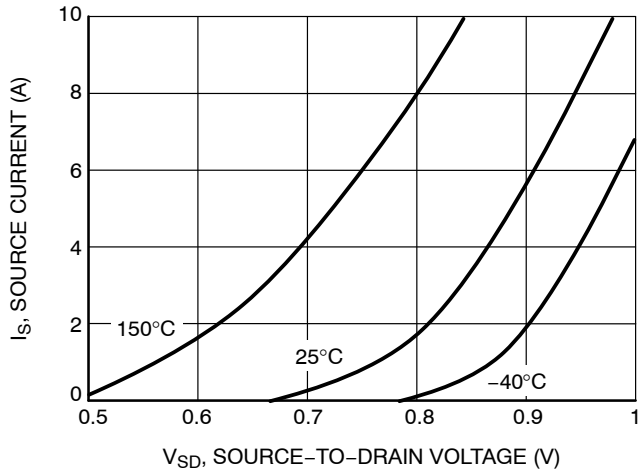


Figure 10. Source-Drain Diode Forward Characteristics

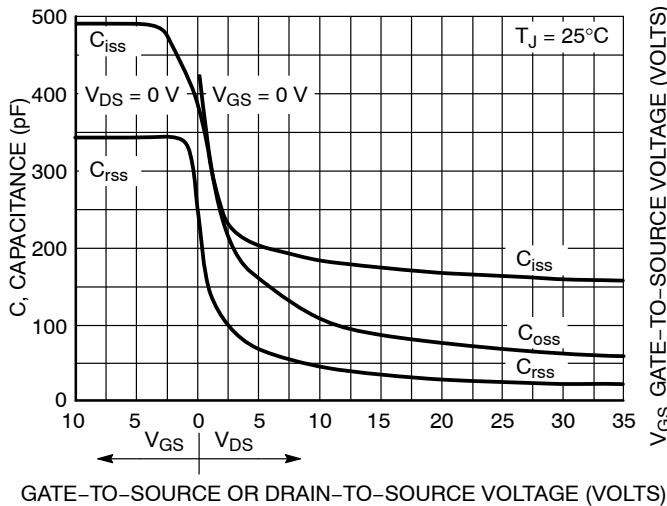


Figure 11. Capacitance Variation

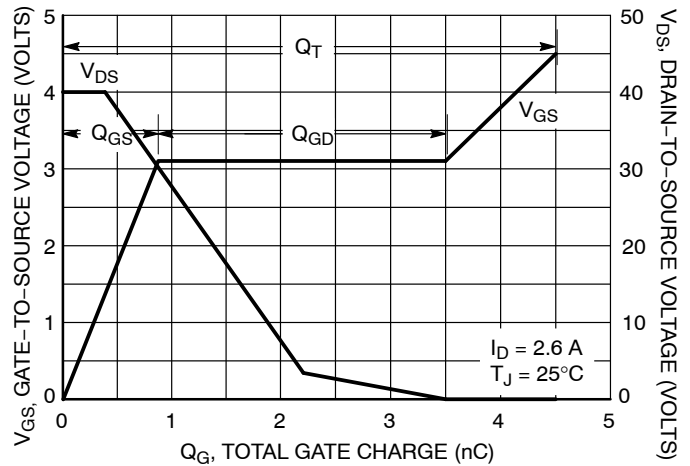


Figure 12. Gate-to-Source Voltage vs. Total Gate Charge

TYPICAL PERFORMANCE CURVES

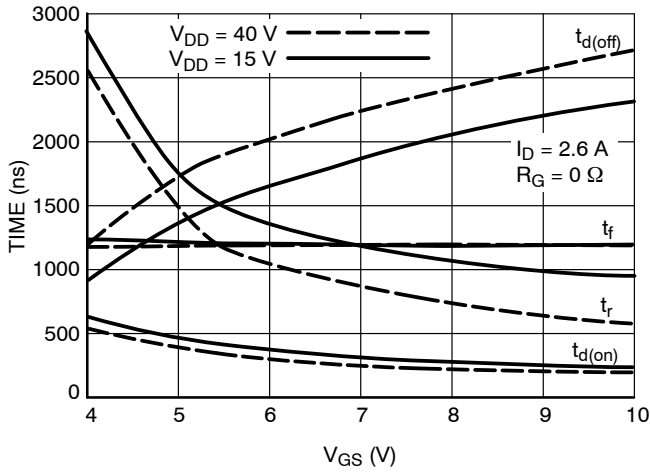


Figure 13. Resistive Load Switching Time vs. Gate-Source Voltage

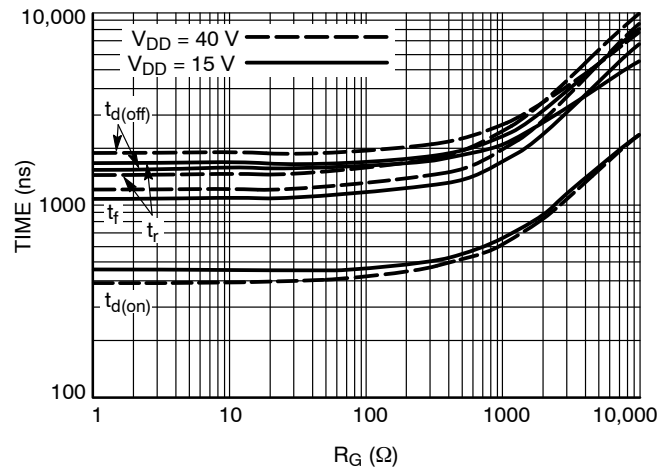


Figure 14. Resistive Load Switching Time vs. Gate Resistance ($V_{GS} = 5$ V, $I_D = 2.6$ A)

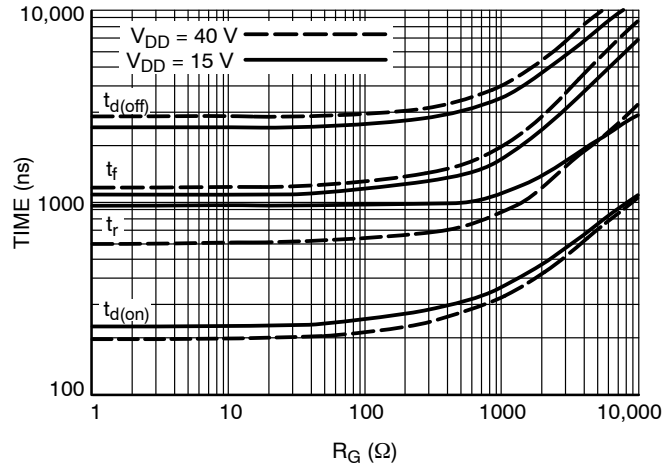


Figure 15. Resistive Load Switching Time vs. Gate Resistance ($V_{GS} = 10$ V, $I_D = 2.6$ A)

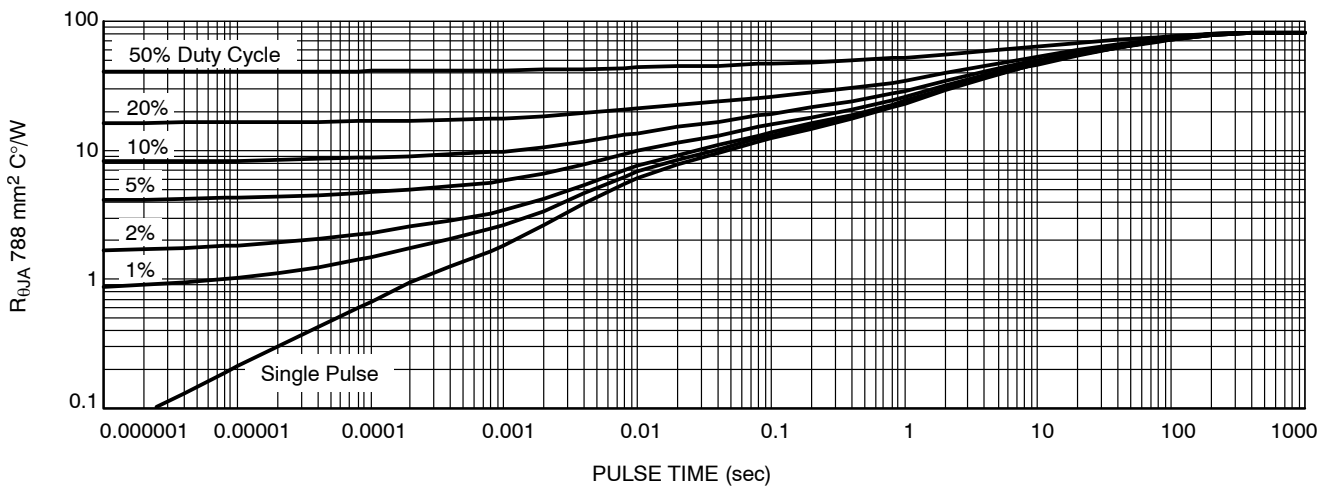
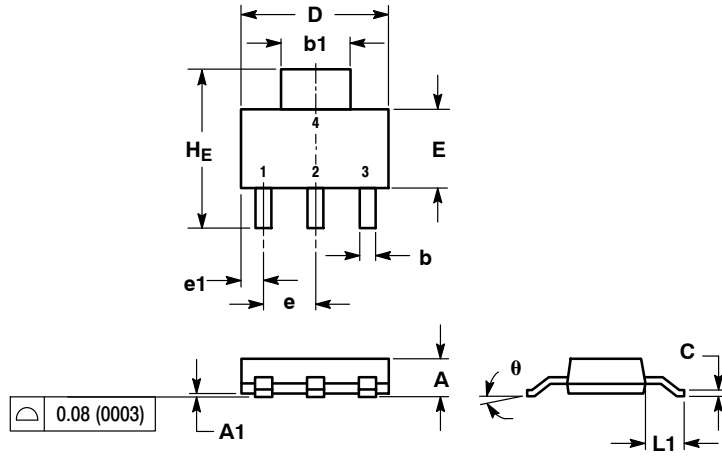


Figure 16. Transient Thermal Resistance

NCV8440

PACKAGE DIMENSIONS

SOT-223 (TO-261)
CASE 318E-04
ISSUE L



NOTES:

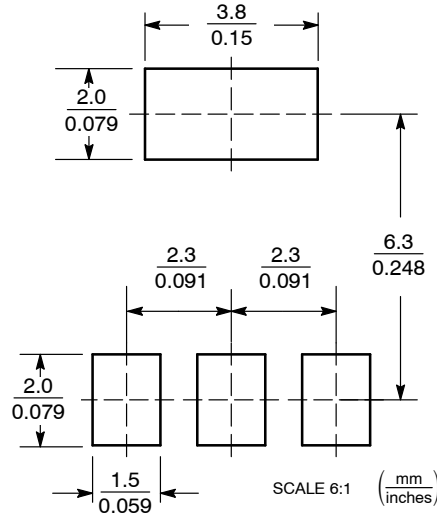
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.63	1.75	0.060	0.064	0.068
A1	0.02	0.06	0.10	0.001	0.002	0.004
b	0.60	0.75	0.89	0.024	0.030	0.035
b1	2.90	3.06	3.20	0.115	0.121	0.126
c	0.24	0.29	0.35	0.009	0.012	0.014
D	6.30	6.50	6.70	0.249	0.256	0.263
E	3.30	3.50	3.70	0.130	0.138	0.145
e	2.20	2.30	2.40	0.087	0.091	0.094
e1	0.85	0.94	1.05	0.033	0.037	0.041
L1	1.50	1.75	2.00	0.060	0.069	0.078
HE	6.70	7.00	7.30	0.264	0.276	0.287
θ	0°	-	10°	0°	-	10°

STYLE 3:

- PIN 1. GATE
- 2. DRAIN
- 3. SOURCE
- 4. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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