# **Protected Power MOSFET**

# 2.6 A, 52 V, N-Channel, Logic Level, Clamped MOSFET w/ ESD Protection

## MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise specified)

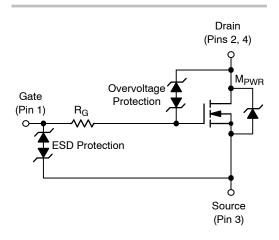
| Rating                                     |               | Symbol                            | Value       | Unit |
|--|---------------|-----------------------------------|-------------|------|
| Drain-to-Source Voltage Internally Clamped |               | $V_{DSS}$                         | 52-59       | ٧    |
| Gate-to-Source Voltage - Continuous        |               | $V_{GS}$                          | ±15         | ٧    |
| Operating and Storage Temperature Range    |               | T <sub>J</sub> , T <sub>stg</sub> | -55 to 150  | °C   |
| Electro-Static Discharge Capability        | (HBM)<br>(MM) | ESD                               | 5000<br>500 | ٧    |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.



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#### **ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

## $\textbf{MOSFET ELECTRICAL CHARACTERISTICS} \ (T_J = 25^{\circ}C \ unless \ otherwise \ specified) \ (Note \ 1)$

| Charac   | teristic   | Symbol               | Min | Тур               | Max               | Unit |
|--|--|----------------------|-----|-------------------|-------------------|------|
| OFF CHARACTERISTICS  |  |                      | •   |                   | •                 |      |
| Drain-to-Source Breakdown Voltage (V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1.0 mA, T <sub>J</sub> = 25°C)  |  | V <sub>(BR)DSS</sub> | 52  | 55                | 59                | V    |
| Zero Gate Voltage Drain Current (V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V)  |  | I <sub>DSS</sub>     |     |                   | 10                | μΑ   |
| Gate-Body Leakage Current $(V_{GS} = \pm 8 \text{ V}, V_{DS} = 0 \text{ V})$ $(V_{GS} = \pm 14 \text{ V}, V_{DS} = 0 \text{ V})$   |  | I <sub>GSS</sub>     |     | ±22               | ±10               | μΑ   |
| ON CHARACTERISTICS   |  |                      |     |                   |                   |      |
| Gate Threshold Voltage $(V_{DS} = V_{GS}, I_D = 100 \mu A)$  |  | V <sub>GS(th)</sub>  | 1.3 | 1.75              | 2.5               | V    |
| Static Drain-to-Source On-Resistance ( $V_{GS} = 3.5 \text{ V}$ , $I_D = 0.6 \text{ A}$ ) ( $V_{GS} = 4.0 \text{ V}$ , $I_D = 1.5 \text{ A}$ ) ( $V_{GS} = 10 \text{ V}$ , $I_D = 2.6 \text{ A}$ ) |  | R <sub>DS(on)</sub>  |     | 190<br>165<br>107 | 380<br>200<br>125 | mΩ   |
| SOURCE-DRAIN DIODE CHARACTERISTICS   |  |                      |     |                   |                   |      |
| Forward On-Voltage   | I <sub>S</sub> = 2.6 A, V <sub>GS</sub> = 0 V<br>I <sub>S</sub> = 2.6 A, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125°C | V <sub>SD</sub>      |     | 0.81<br>0.66      | 1.5               | V    |

<sup>1.</sup> Wafers tested prior to sawing or shipped as whole wafers.

## **ORDERING INFORMATION**

| Device     | Shipping     |
|------------|--------------|
| NCV8440CWP | Whole Wafers |

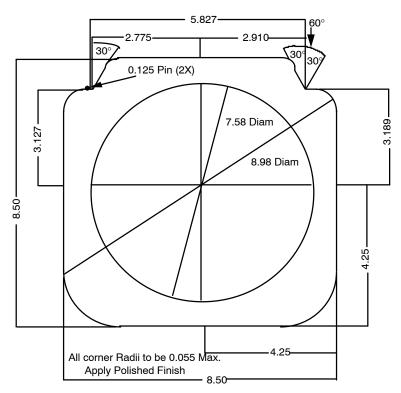


Figure 1. Wafer Mounted on Frame

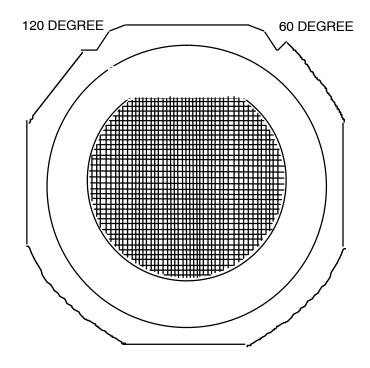


Figure 2. Wafer Orientation on Frame

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