

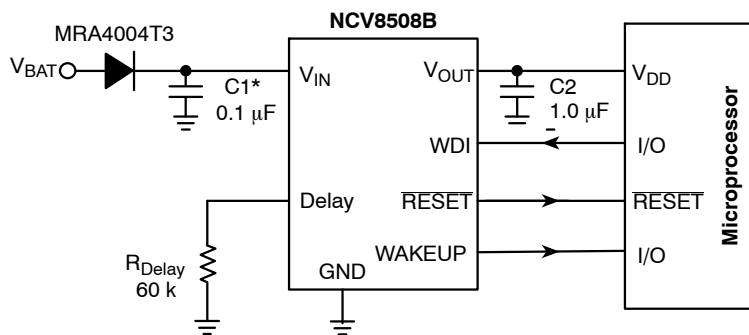
NCV8508B

5.0 V, 250 mA LDO with Watchdog and $\overline{\text{RESET}}$

The NCV8508B is a precision micropower Low Dropout (LDO) voltage regulator. The part contains many of the required features for powering microprocessors. Its robustness makes it suitable for severe automotive environments. In addition, the NCV8508B is ideal for use in battery operated, microprocessor controlled equipment because of its extremely low quiescent current.

Features

- Output Voltage: 5.0 V
- $\pm 3.0\%$ Output Voltage
- I_{OUT} Up to 250 mA
- Quiescent Current Independent of Load
- Micropower Compatible Control Functions:
 - ◆ Wakeup
 - ◆ Watchdog
 - ◆ $\overline{\text{RESET}}$
- Low Quiescent Current (100 μA typ)
- Protection Features:
 - ◆ Thermal Shutdown
 - ◆ Short Circuit
 - ◆ 45 V Operation
- NCV Prefix for Automotive and Other Applications Requiring Site and Change Controls
- AEC Qualified
- PPAP Capable
- These are Pb-Free Devices



*C1 required if regulator is located far from power supply filter.

Figure 1. Application Circuit



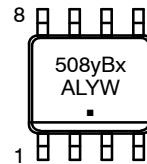
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MARKING DIAGRAM

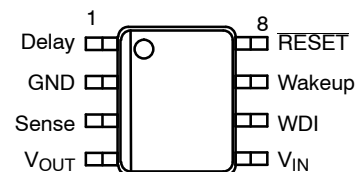


**SO-8 EP
PD SUFFIX
CASE 751AC**



- x = Voltage Option
5.0 V (x = 5)
- y = Timing Option
(see Page 4 for more details)
1 (Delay Time = 3 ms @ $R_{\text{Delay}} = 60\text{k}$)
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

PIN CONNECTION



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.

NCV8508B

PACKAGE PIN DESCRIPTION

PACKAGE PIN #		
SO-8 EP	PIN SYMBOL	FUNCTION
4	V _{OUT}	Regulated output voltage $\pm 3.0\%$.
5	V _{IN}	Supply Voltage to the IC.
6	WDI	CMOS compatible input lead. The Watchdog function monitors the falling edge of the incoming signal.
2	GND	Ground connection.
7	Wakeup	CMOS compatible output consisting of a continuously generated signal used to "wake up" the microprocessor from sleep mode.
8	$\overline{\text{RESET}}$	CMOS compatible output lead $\overline{\text{RESET}}$ goes low whenever V _{OUT} drops by more than 7.0% from nominal, or during the absence of a correct Watchdog signal.
1	Delay	Buffered bandgap voltage used to create timing current for $\overline{\text{RESET}}$ and Wakeup from R _{Delay} .
3	Sense	Kelvin connection which allows remote sensing of the output voltage for improved regulation. Connect to V _{OUT} if remote sensing is not required.
EPAD	EPAD	Connect to Ground potential or leave unconnected.

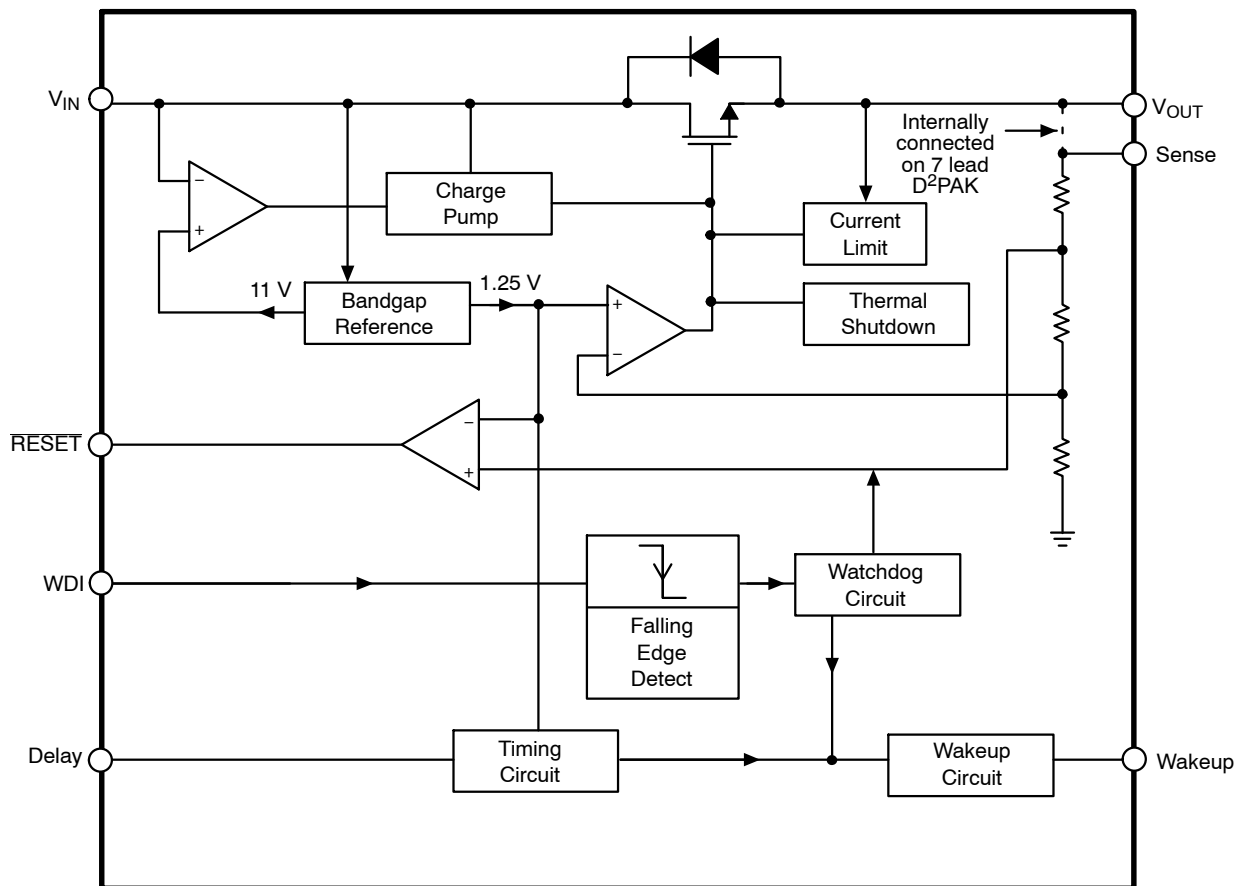


Figure 2. Block Diagram

NCV8508B

MAXIMUM RATINGS

Rating	Value	Unit
Input Voltage, V_{IN} (DC)	-0.3 to 45	V
Peak Transient Voltage (46 V Load Dump @ $V_{IN} = 14$ V)	60	V
Output Voltage, V_{OUT}	-0.3 to 18	V
ESD Susceptibility:	Human Body Model	2.0 kV
	Machine Model	200 V
Logic Inputs/Outputs (RESET, WDI, Wakeup)	-0.3 to +7.0	V
Operating Junction Temperature, T_J	-40 to 150	°C
Storage Temperature Range, T_S	-55 to +150	°C
Peak Reflow Soldering Temperature:	Reflow: (Note 1)	240 Peak 260 Peak (Pb-Free) (Note 3)
Moisture Sensitivity Level:	SO-16	1
	D2PAK	1
	SO-8EP	2

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. 60 second maximum above 183°C.
2. Depending on thermal properties of substrate $R_{\theta JA} = R_{\theta JC} + R_{\theta JCA}$.
3. -5°C/+0°C allowable conditions, applies to both Pb and Pb-Free devices.

THERMAL CHARACTERISTICS

See Package Thermal Data Section (Page 10)

NCV8508B

ELECTRICAL CHARACTERISTICS ($-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$; $6.0\text{ V} \leq V_{\text{IN}} \leq 28\text{ V}$, $100\ \mu\text{A} \leq I_{\text{OUT}} \leq 150\text{ mA}$, $C_2 = 1.0\ \mu\text{F}$, $R_{\text{Delay}} = 60\text{ k}$; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit	
OUTPUT						
Output Voltage	5.0 V	-	4.85	5.00	5.15	V
Dropout Voltage ($V_{\text{IN}} - V_{\text{OUT}}$)	5.0 V	$I_{\text{OUT}} = 150\text{ mA}$. Note 4	-	450	900	mV
Load Regulation	$V_{\text{IN}} = 14\text{ V}$, $100\ \mu\text{A} \leq I_{\text{OUT}} \leq 150\text{ mA}$	-	5.0	30	mV	
Line Regulation	$6.0\text{ V} \leq V_{\text{IN}} \leq 28\text{ V}$, $I_{\text{OUT}} = 5.0\text{ mA}$	-	5.0	50	mV	
Current Limit	-	250	400	-	mA	
Thermal Shutdown	Guaranteed by Design	150	180	210	$^{\circ}\text{C}$	
Quiescent Current	$V_{\text{IN}} = 12\text{ V}$, $I_{\text{OUT}} = 150\text{ mA}$, (see Figure 6)	-	100	150	μA	

RESET

Threshold	5.0 V	-	4.50	4.65	4.80	V
Output Low		$R_{\text{LOAD}} = 10\text{ k to } V_{\text{OUT}}$, $V_{\text{OUT}} \geq 1.0\text{ V}$ $R_{\text{LOAD}} = 5.1\text{ k to } V_{\text{OUT}}$, $V_{\text{OUT}} \geq 1.0\text{ V}$	-	0.2 0.4	0.4 0.8	V
Output High		$R_{\text{LOAD}} = 10\text{ k to GND}$ $R_{\text{LOAD}} = 5.1\text{ k to GND}$	$V_{\text{OUT}} - 0.5$ $V_{\text{OUT}} - 1.0$	$V_{\text{OUT}} - 0.25$ $V_{\text{OUT}} - 0.5$	-	V
Delay Time	NCV85081B	$V_{\text{IN}} = 14\text{ V}$, $R_{\text{Delay}} = 60\text{ k}$, $I_{\text{OUT}} = 5.0\text{ mA}$ $V_{\text{IN}} = 14\text{ V}$, $R_{\text{Delay}} = 120\text{ k}$, $I_{\text{OUT}} = 5.0\text{ mA}$	2.0 -	3.0 6.0	4.0 -	ms ms

WATCHDOG INPUT

Threshold High	-	70	-	-	$\%V_{\text{OUT}}$
Threshold Low	-	-	-	30	$\%V_{\text{OUT}}$
Hysteresis	-	-	100	-	mV
Input Current	$\text{WDI} = 6.0\text{ V}$	-	0.1	+10	μA
Pulse Width	50% WDI falling edge to 50% WDI rising edge and 50% WDI rising edge to 50% WDI falling edge, (see Figure 5)	5.0	-	-	μs

WAKEUP OUTPUT ($V_{\text{IN}} = 14\text{ V}$, $I_{\text{OUT}} = 5.0\text{ mA}$)

Wakeup Period	NCV85081B	See Figures 4 and 5, $R_{\text{DELAY}} = 60\text{ k}$ See Figures 4 and 5, $R_{\text{DELAY}} = 120\text{ k}$	18 -	25 50	32 -	ms ms
Wakeup Duty Cycle Nominal		See Figure 3	45	50	55	%
RESET HIGH to Wakeup Rising Delay Time	NCV85081B	$R_{\text{DELAY}} = 60\text{ k}$, 50% RESET rising edge to 50% Wakeup edge $R_{\text{DELAY}} = 120\text{ k}$ (see Figures 3 and 4)	9.0 -	12.5 25	16 -	ms ms
Wakeup Response to Watchdog Input		50% WDI falling edge to 50% Wakeup falling edge	-	0.1	5.0	μs
Wakeup Response to RESET		50% RESET falling edge to 50% Wakeup falling edge $V_{\text{OUT}} = V_{\text{OUT_NOM}} \rightarrow 90\%$ of $V_{\text{OUT_NOM}}$	-	0.1	5.0	μs
Output Low		$R_{\text{LOAD}} = 10\text{ k to } V_{\text{OUT}}$, $V_{\text{OUT}} \geq 1.0\text{ V}$ $R_{\text{LOAD}} = 5.1\text{ k to } V_{\text{OUT}}$, $V_{\text{OUT}} \geq 1.0\text{ V}$	-	0.2 0.4	0.4 0.8	V
Output High		$R_{\text{LOAD}} = 10\text{ k to GND}$ $R_{\text{LOAD}} = 5.1\text{ k to GND}$	$V_{\text{OUT}} - 0.5$ $V_{\text{OUT}} - 1.0$	$V_{\text{OUT}} - 0.25$ $V_{\text{OUT}} - 0.5$	-	V

DELAY

Output Voltage	$I_{\text{DELAY}} = 50\ \mu\text{A}$. Note 5	-	1.25	-	V
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4. Measured when the output voltage has dropped 100 mV from the nominal value. (see Figure 12)
5. Current drain on the Delay pin directly affects the Delay Time, Wakeup Period, and the RESET to Wakeup Delay Time.

TIMING DIAGRAMS

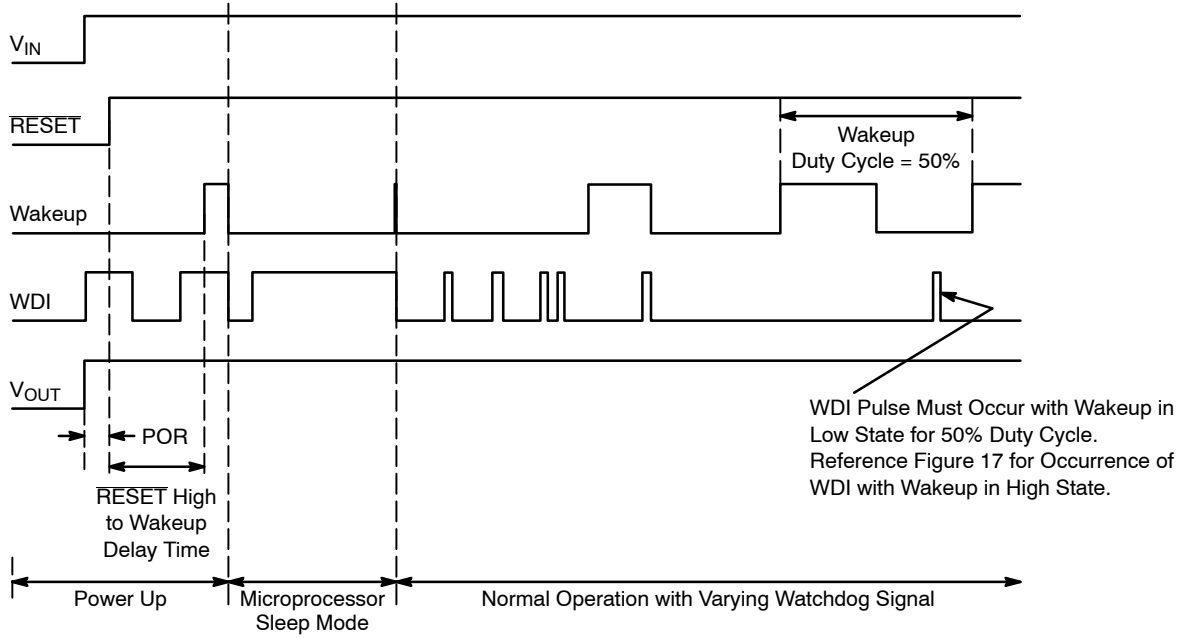


Figure 3. Power Up, Sleep Mode and Normal Operation

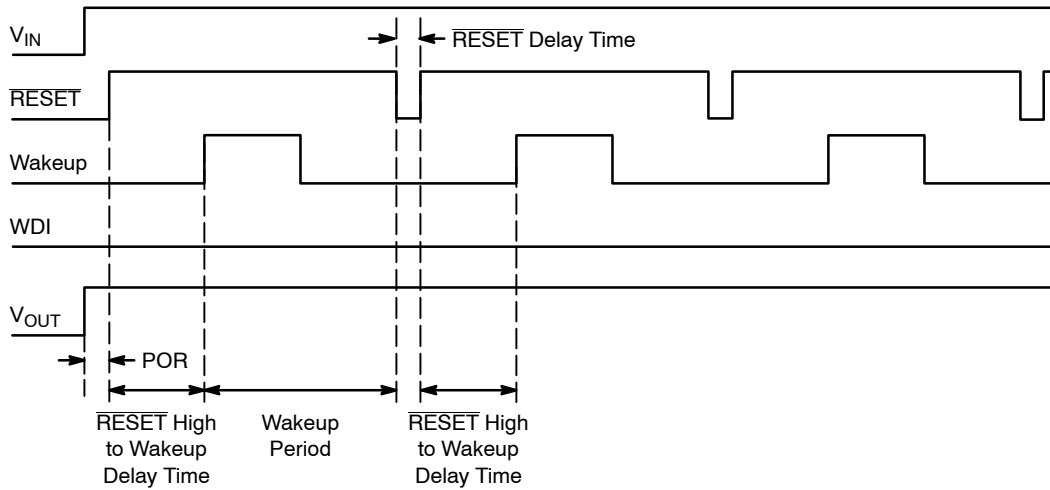


Figure 4. Error Condition: Watchdog Remains Low and a RESET Is Issued

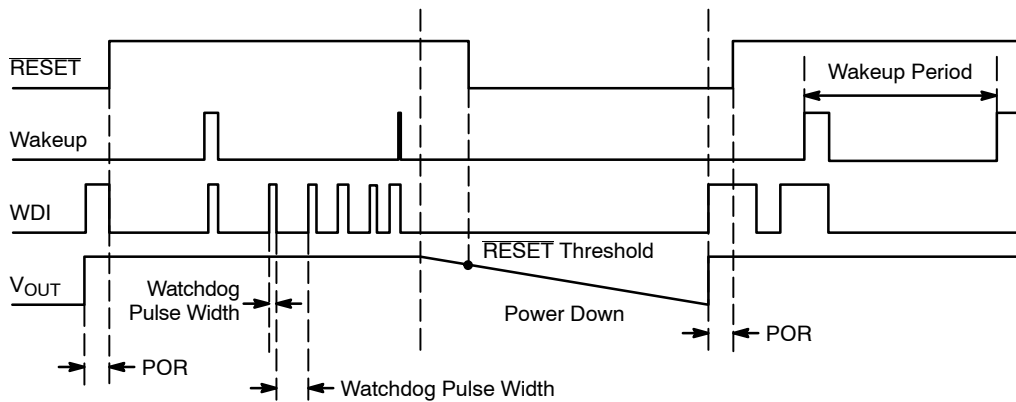


Figure 5. Power Down and Restart Sequence

TYPICAL PERFORMANCE CHARACTERISTICS

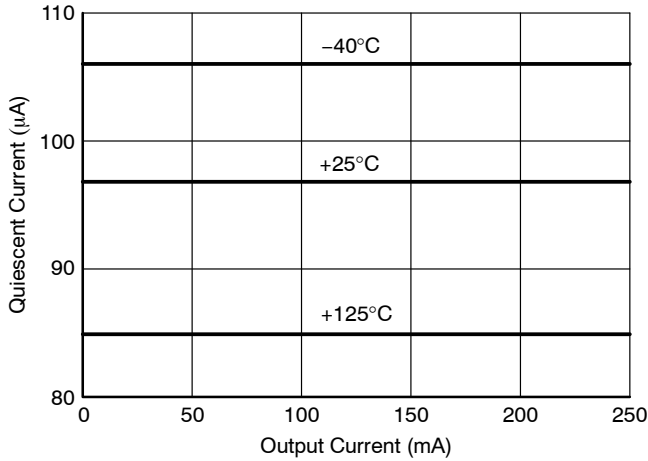


Figure 6. Quiescent Current vs Output Current

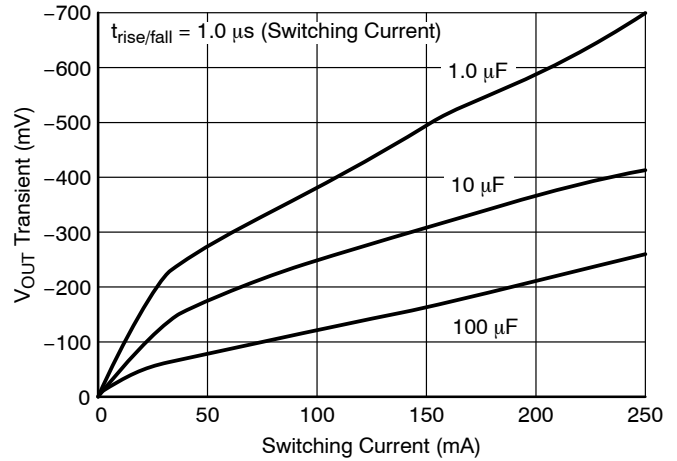


Figure 7. Load Transient Response

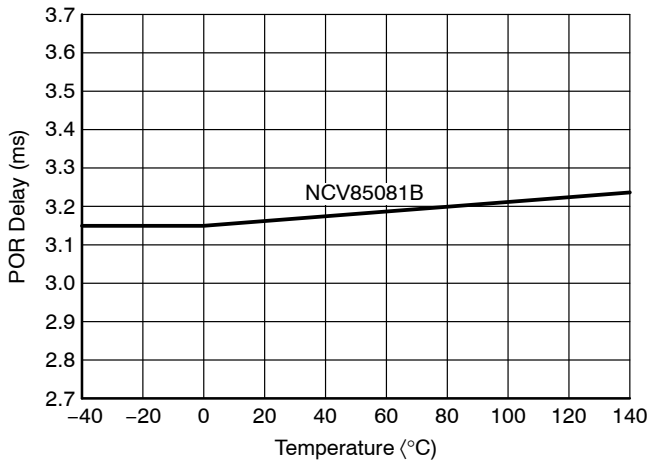


Figure 8. POR Delay vs Temp, $R_{DELAY} = 60\text{ k}\Omega$

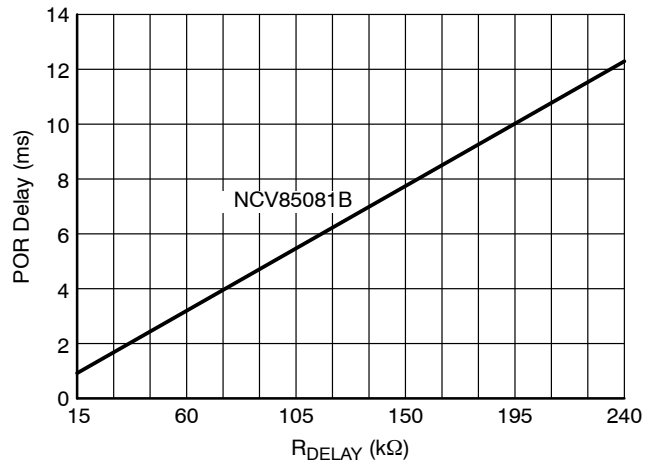


Figure 9. POR Delay vs R_{DELAY}

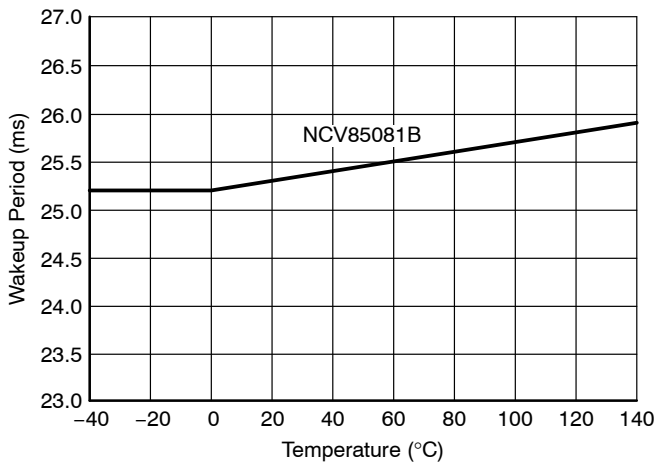


Figure 10. Wakeup Period vs Temp, $R_{DELAY} = 60\text{ k}\Omega$

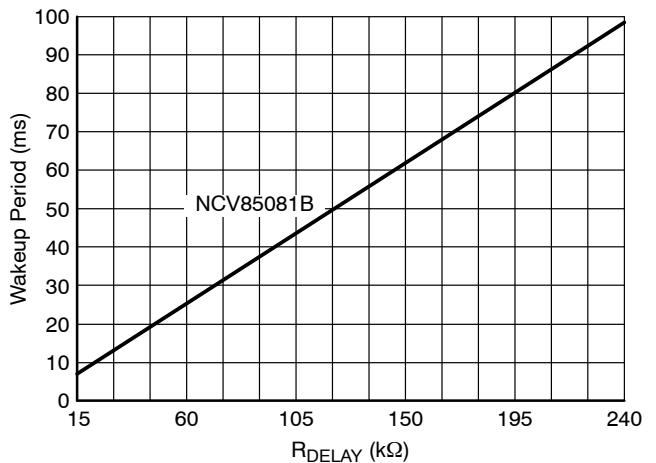


Figure 11. Wakeup Period vs R_{DELAY}

TYPICAL PERFORMANCE CHARACTERISTICS

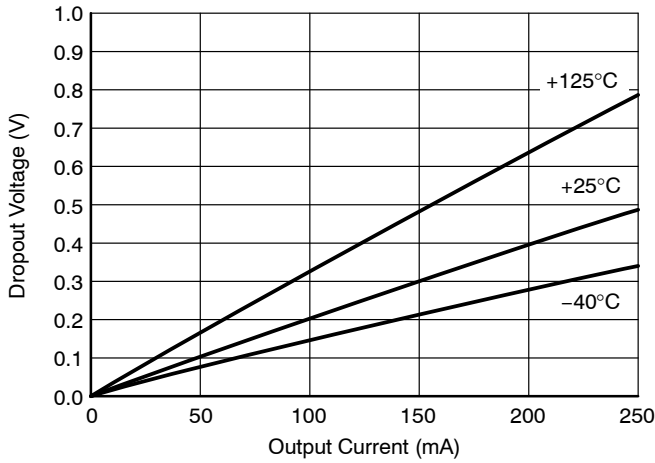


Figure 12. Dropout Voltage vs Output Current

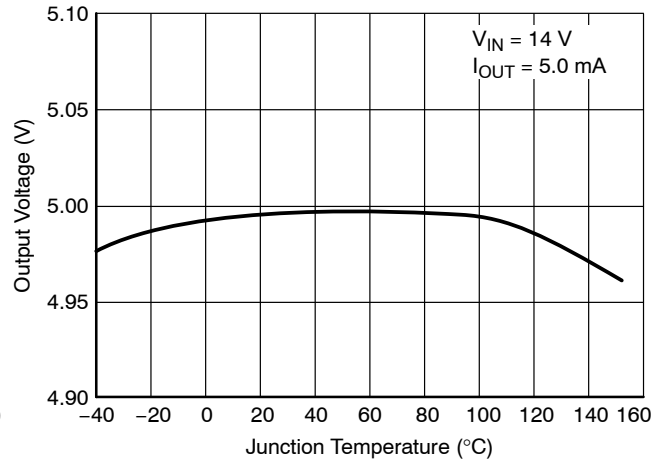


Figure 13. Output Voltage vs Temperature

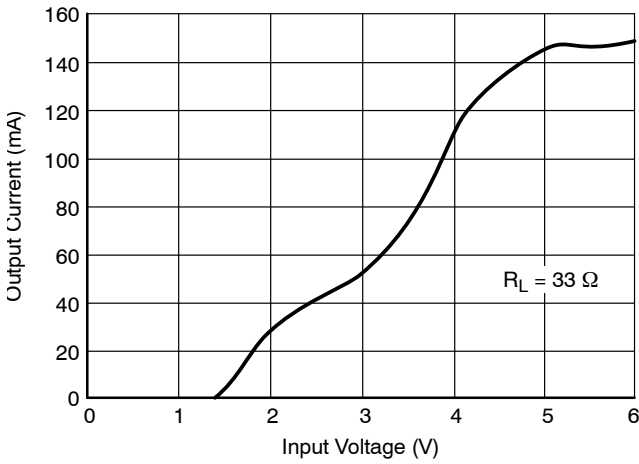


Figure 14. Output Current vs Input Voltage

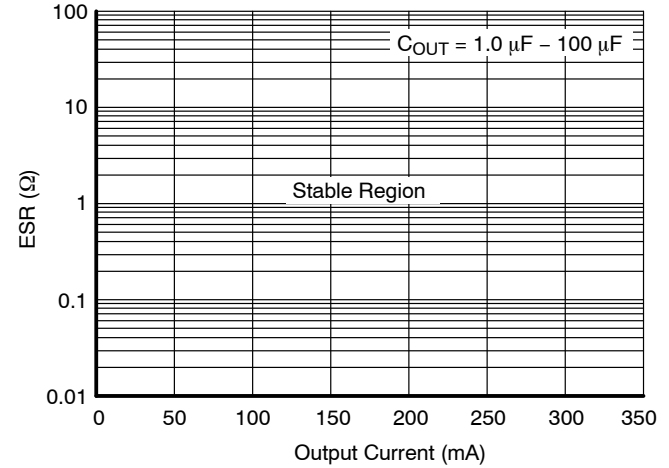


Figure 15. Output Capacitor ESR

DEFINITION OF TERMS

Dropout Voltage: The input–output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14 V input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques

such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Quiescent Current: The part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

Ripple Rejection: The ratio of the peak–to–peak input ripple voltage to the peak–to–peak output ripple voltage.

Current Limit: Peak current that can be delivered to the output.

NCV8508B

DETAILED OPERATING DESCRIPTION

The NCV8508B is a precision micropower voltage regulator with very low quiescent current (100 μ A typical at 250 mA load). A typical dropout voltage is 450 mV at 150 mA for 5 V option. Microprocessor control logic includes Watchdog, Wakeup and $\overline{\text{RESET}}$. This unique combination of extremely low quiescent current and full microprocessor control makes the NCV8508B ideal for use in battery operated, microprocessor controlled equipment in addition to being a good fit in the automotive environment.

The NCV8508B Wakeup function brings the microprocessor out of Sleep mode. The microprocessor in turn signals its Wakeup status back to the NCV8508B by issuing a Watchdog signal.

The Watchdog logic function monitors an input signal (WDI) from the microprocessor. The NCV8508B responds to the falling edge of the Watchdog signal which it expects at least once during each Wakeup period. When the correct Watchdog signal is received, a falling edge is issued on the Wakeup signal line.

$\overline{\text{RESET}}$ is independent of V_{IN} and operates correctly to an output voltage as low as 1.0 V. A signal is issued in any of three situations. During power up, the $\overline{\text{RESET}}$ is held low until the output voltage is in regulation. During operation, if the output voltage shifts below the regulation limits, the $\overline{\text{RESET}}$ toggles low and remains low until proper output voltage regulation is restored. Finally, a $\overline{\text{RESET}}$ signal is issued if the regulator does not receive a Watchdog signal within the Wakeup period.

The $\overline{\text{RESET}}$ pulse width, Wakeup signal frequency, and Wakeup delay time are all set by one external resistor, R_{Delay} .

The Delay pin is a buffered bandgap voltage (1.25 V). It can be used as a reference for an external tracking regulator as shown in Figure 16.

The regulator is protected against short circuit and thermal runaway conditions. The device runs through 45 volt transients, making it suitable for use in automotive environments.

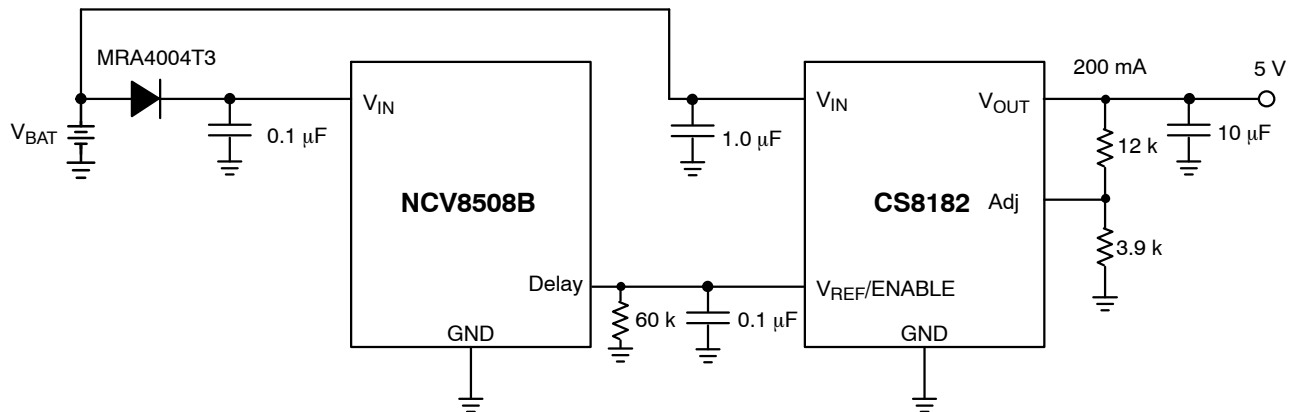


Figure 16. Application Circuit

CIRCUIT DESCRIPTION

Functional Description

To reduce the drain on the battery, a system can go into a low current consumption mode whenever it is not performing a main routine. The Wakeup signal is generated continuously and is used to interrupt a microcontroller that is in sleep mode. The nominal output is a 5.0 V square wave (voltage generated from V_{OUT}) with a duty cycle of 50% at a frequency that is determined by a timing resistor, R_{Delay} .

When the microprocessor receives a rising edge from the Wakeup output, it must issue a Watchdog pulse and check its inputs to decide if it should resume normal operations or remain in the sleep mode.

The first falling edge of the Watchdog signal causes the Wakeup to go low within 2.0 μ s (typ) and remain low until the next Wakeup cycle (see Figure 17). Other Watchdog pulses received within the same cycle are ignored (Figure 3).

During power up, \overline{RESET} is held low until the output voltage is in regulation. During operation, if the output voltage shifts below the regulation limits, the \overline{RESET} toggles low and remains low until proper output voltage regulation is restored. After the \overline{RESET} delay, \overline{RESET} returns high.

The Watchdog circuitry continuously monitors the input Watchdog signal (WDI) from the microprocessor. The absence of a falling edge on the Watchdog input during one Wakeup cycle will cause a \overline{RESET} pulse to occur at the end of the Wakeup cycle. (see Figure 4).

The Wakeup output is pulled low during a \overline{RESET} regardless of the cause of the \overline{RESET} . After the \overline{RESET} returns high, the Wakeup cycle begins again (see Figure 4).

The \overline{RESET} Delay Time, Wakeup signal frequency and \overline{RESET} high to Wakeup delay time are all set by one external resistor R_{Delay} .

$$\text{Wakeup Period} = (4.17 \times 10^{-7})R_{Delay}$$

$$\overline{RESET} \text{ Delay Time} = (5.21 \times 10^{-8})R_{Delay}$$

$$\overline{RESET} \text{ HIGH to Wakeup Delay Time} = (2.08 \times 10^{-7})R_{Delay}$$

Resistor temperature coefficient and tolerance as well as the tolerance of the NCV8508B must be taken into account

in order to get the correct system tolerance for each parameter.

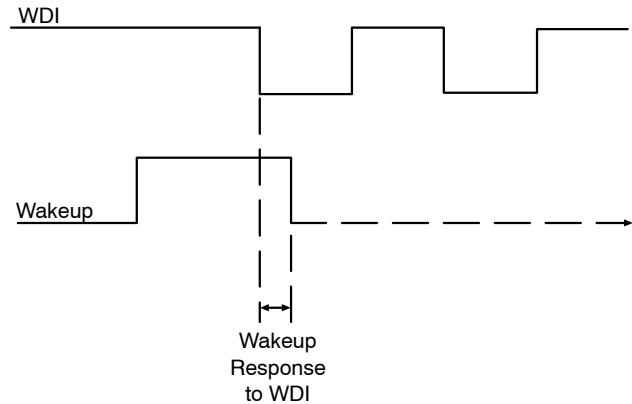


Figure 17. Wakeup Response to WDI

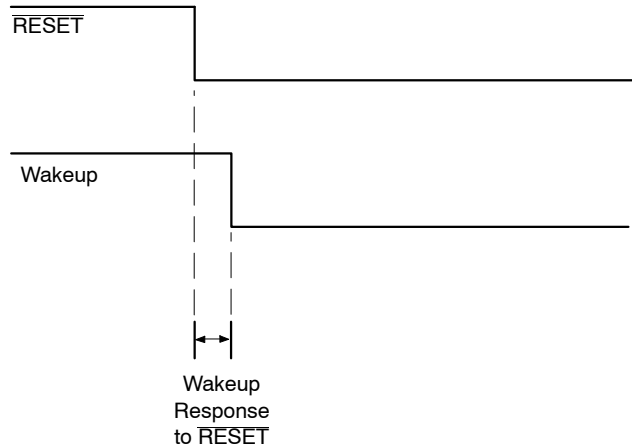


Figure 18. Wakeup Response to \overline{RESET} (Low Voltage)

NCV8508B

Recommend Thermal Data for SOIC-8 EP Package

Parameter	Test Conditions Typical Value		Units
	min-pad board (Note 6)	1"-pad board (Note 7)	
Junction-to-Lead (ψ_{JL} , Ψ_{JL})	38	24	°C/W
Junction-to-Lead (ψ_{Jp} , Ψ_{Jp})	8.0	9.0	°C/W
Junction-to-Ambient ($R_{\theta JA}$, θ_{JA})	126	64	°C/W

6. 1 oz. copper, 54 mm² copper area, 0.062" thick FR4.
 7. 1 oz. copper, 717 mm² copper area, 0.062" thick FR4.

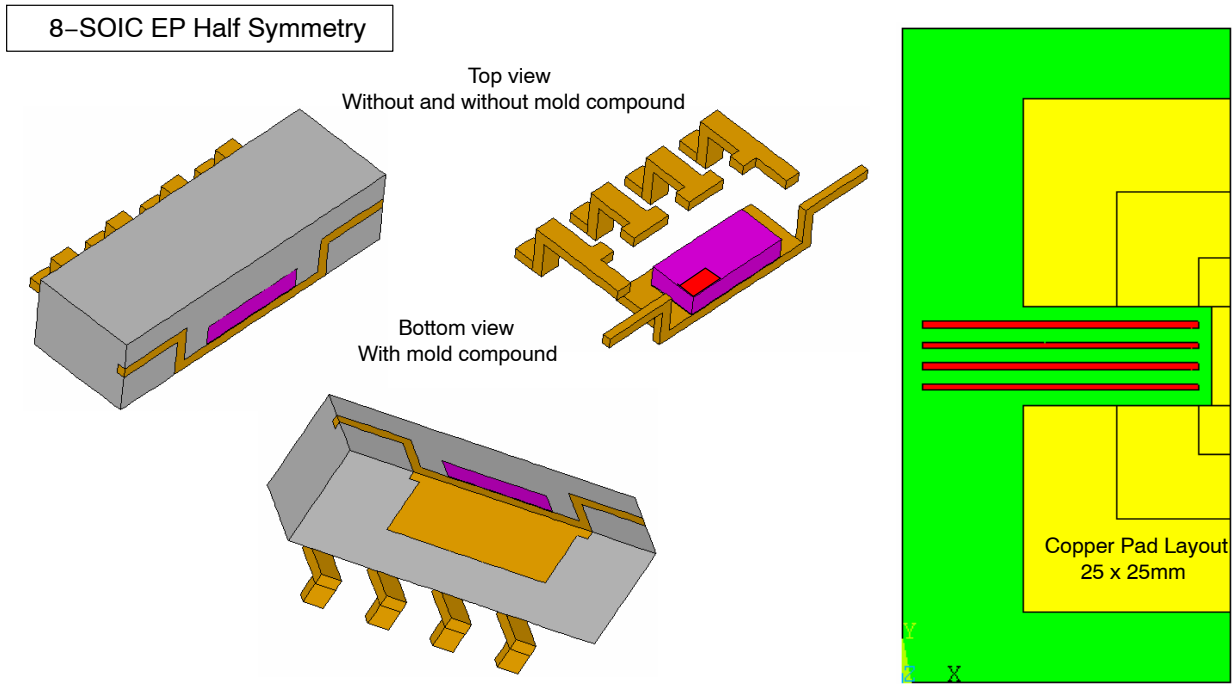


Figure 19. Internal Construction of the Package and PCB Layout for Multiple Pad Area

NCV8508B

Table 1. SOIC 8-Lead EP Thermal RC Network Models

	54 mm ²	717 mm ²		54 mm ²	717 mm ²	Cu Area
	Cauer Network			Foster Network		
	C's	C's	Units	Tau	Tau	units
1	2.7E-06	2.7E-06	W-s/C	1.00E-06	1.00E-06	sec
2	1.1E-05	1.1E-05	W-s/C	1.00E-05	1.00E-05	sec
3	3.2E-05	3.2E-05	W-s/C	1.00E-04	1.00E-04	sec
4	1.3E-04	1.3E-04	W-s/C	9.39E-04	9.39E-04	sec
5	1.8E-03	1.8E-03	W-s/C	3.13E-03	3.13E-03	sec
6	7.9E-03	8.3E-03	W-s/C	3.30E-02	3.30E-02	sec
7	2.5E-02	3.1E-02	W-s/C	6.00E-01	6.00E-01	sec
8	1.4E-01	5.1E-01	W-s/C	4.00E+00	4.00E+00	sec
9	4.1E-01	2.1E+00	W-s/C	1.16E+01	4.83E+01	sec
10	1.6E+00	6.3E+01	W-s/C	5.58E+01	2.37E+02	sec
	R's	R's		R's	R's	
1	0.474	0.474	C/W	0.282	0.282	C/W
2	1.086	1.086	C/W	0.610	0.610	C/W
3	3.011	3.010	C/W	1.929	1.929	C/W
4	5.883	5.874	C/W	5.825	5.825	C/W
5	1.944	1.911	C/W	2.700	2.700	C/W
6	4.655	4.264	C/W	3.000	3.000	C/W
7	21.431	15.678	C/W	15.000	15.000	C/W
8	40.130	9.238	C/W	11.494	7.797	C/W
9	23.392	18.454	C/W	34.982	20.473	C/W
10	24.381	3.581	C/W	50.566	5.953	C/W

NOTE: Bold face items in the Cauer network above, represent the package without the external thermal system. The Bold face items in the Foster network are computed by the square root of time constant $R(t) = 225 * \text{sqrt}(\text{time}(\text{sec}))$. The constant is derived based on the active area of the device with silicon and epoxy at the interface of the heat generation.

The Cauer networks generally have physical significance and may be divided between nodes to separate thermal behavior due to one portion of the network from another. The Foster networks, though when sorted by time constant (as above) bear a rough correlation with the Cauer networks, are really only convenient mathematical models. Cauer networks can be easily implemented using circuit simulating tools, whereas Foster networks may be more easily implemented using mathematical tools (for instance, in a spreadsheet program), according to the following formula:

$$R(t) = \sum_{i=1}^n R_i (1 - e^{-t/\tau_i})$$

θ_{JA} vs Copper Spreader Area

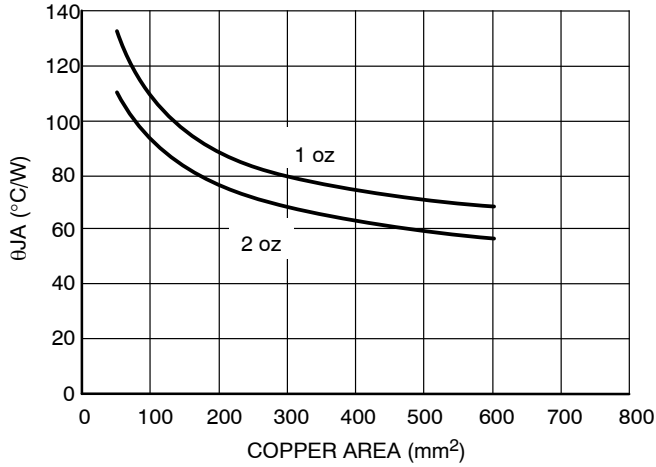


Figure 20. SOIC 8-Lead EP θ_{JA} as a Function of the Pad Copper Area Including Traces, Board Material

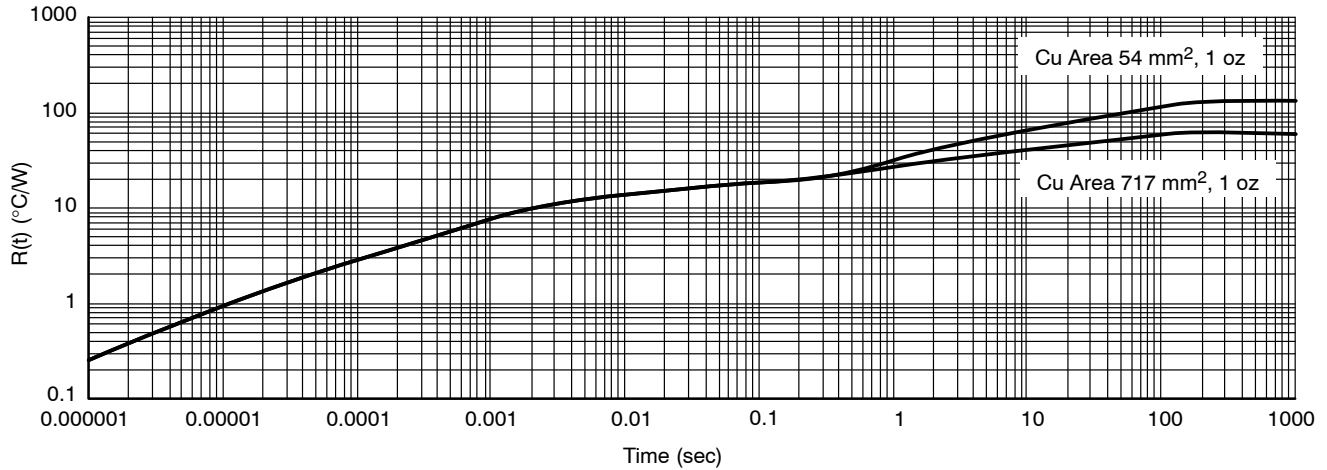


Figure 21. SOIC 8-Lead EP Single Pulse Heating Curve

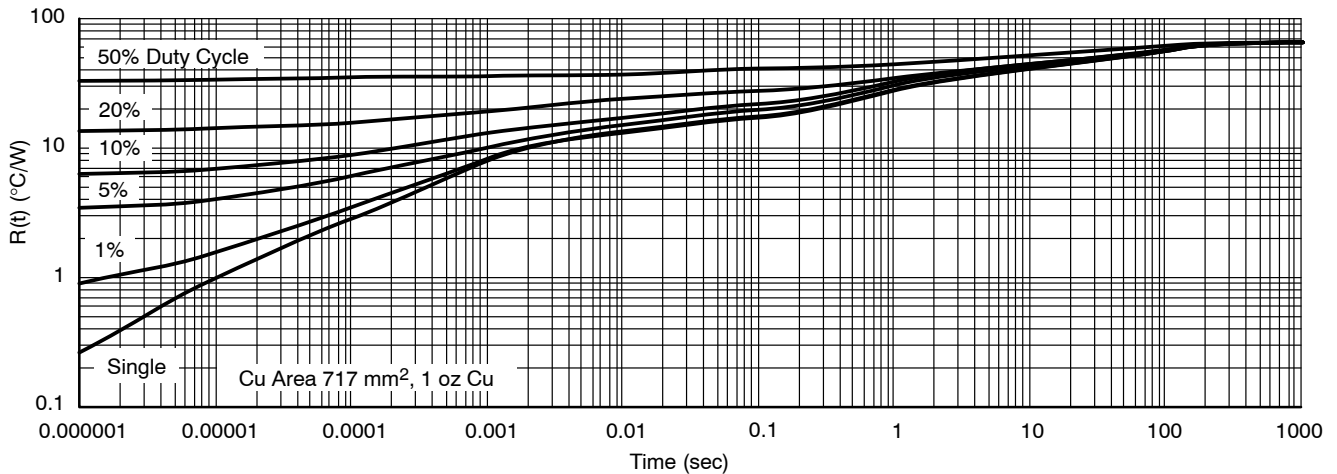
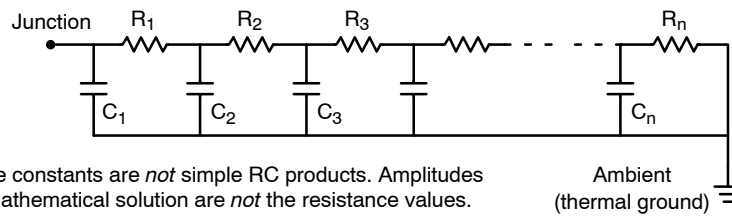


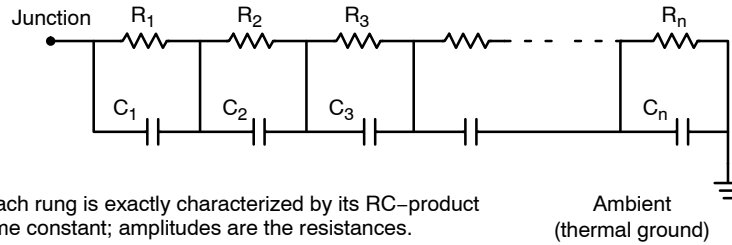
Figure 22. SOIC 8-Lead Thermal Duty Cycle Curves on 1" Spreader Test Board

NCV8508B



Time constants are *not* simple RC products. Amplitudes of mathematical solution are *not* the resistance values.

Figure 23. Grounded Capacitor Thermal Network (“Cauer” Ladder)



Each rung is exactly characterized by its RC-product time constant; amplitudes are the resistances.

Figure 24. Non-Grounded Capacitor Thermal Ladder (“Foster” Ladder)

APPLICATION NOTES

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 25) is:

$$P_{D(max)} = [V_{IN(max)} - V_{OUT(min)}]I_{OUT(max)} + V_{IN(max)}I_Q \quad (1)$$

where:

- $V_{IN(max)}$ is the maximum input voltage,
- $V_{OUT(min)}$ is the minimum output voltage,
- $I_{OUT(max)}$ is the maximum output current for the application, and
- I_Q is the quiescent current the regulator consumes at $I_{OUT(max)}$.

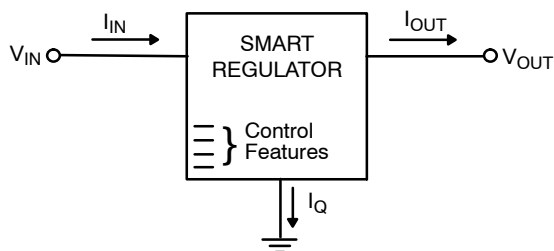


Figure 25. Single Output Regulator with Key Performance Parameters Labeled

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\theta JA} = \frac{150^{\circ}\text{C} - T_A}{P_D} \quad (2)$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$ s less than the calculated value in Equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

Heatsinks

A heatsink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (3)$$

where:

- $R_{\theta JC}$ = the junction-to-case thermal resistance,
- $R_{\theta CS}$ = the case-to-heatsink thermal resistance, and
- $R_{\theta SA}$ = the heatsink-to-ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in data sheets of heatsink manufacturers.

ORDERING INFORMATION

Device	Output Voltage	Timing Option ($R_{Delay} = 60\text{ k}\Omega$)	Package	Shipping†
NCV85081BPD50R2G	5.0 V	Delay Time = 3 ms Wakeup Period = 25 ms RESET HIGH to Wakeup Rising Delay Time = 12.5 ms	SO-8 EP (Pb-Free)	2500 / Tape & Reel

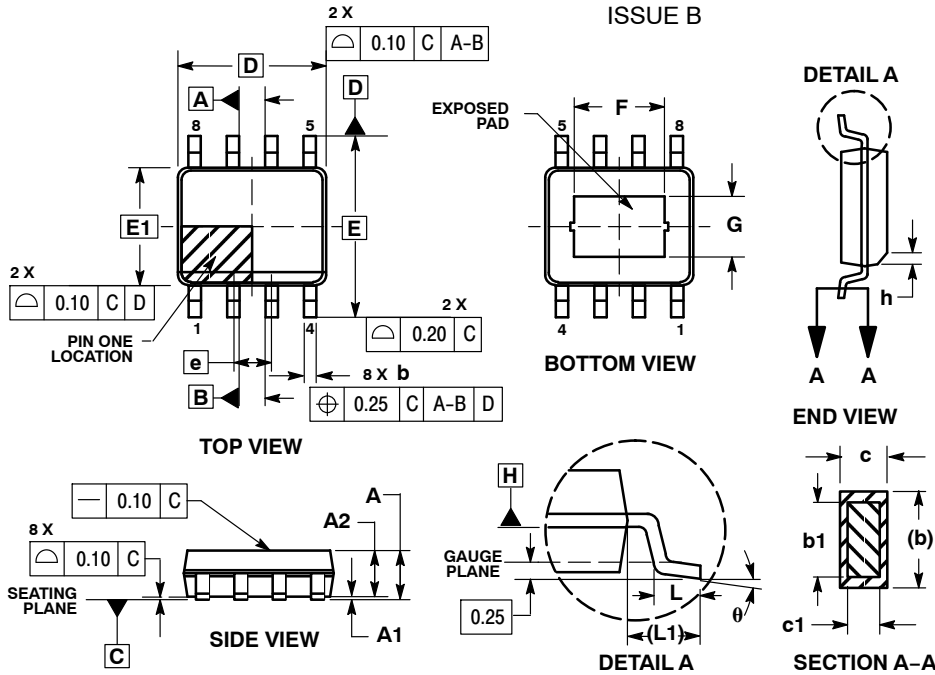
NOTE: Contact factory for other options.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NCV8508B

PACKAGE DIMENSIONS

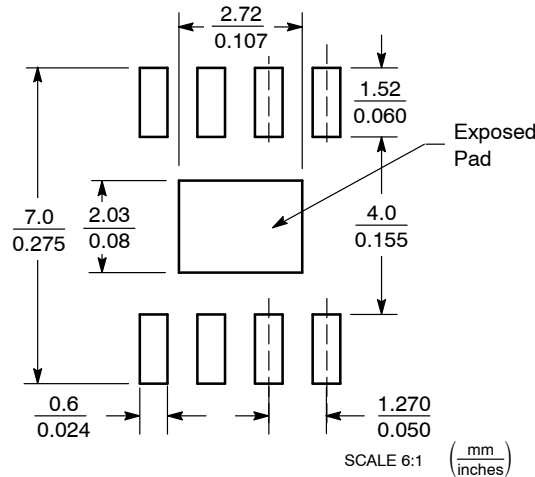
SOIC-8 EP CASE 751AC-01 ISSUE B



NOTES:

- DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
- DIMENSIONS IN MILLIMETERS (ANGLES IN DEGREES).
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION.
- DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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