AOZ1977

High Voltage LED Driver IC

General Description

The AOZ1977 is a high-efficiency LED driver controller for high voltage LED backlighting applications. It is designed to drive a high-brightness LED light bar in LED TV applications. The AOZ1977 can support a wide range of input and output voltages. The input bias voltage of the AOZ1977 is from 8 V to 30 V.

The AOZ1977 has multiple features to protect the regulator under fault conditions. A control pin can disable an external switch to disconnect the LEDs current path from the output in PWM dimming or under catastrophic failure conditions. Cycle-by-cycle current protection limits the peak inductor current. Thermal shutdown provides an additional level of protection.

Low feedback voltage (500 mV) helps reduce power loss.

The AOZ1977 features a sync function to allow for synchronization with an external clock or multiple AOZ1977 devices.

The AOZ1977 is available in a standard SO-16 package and operates over the -40 °C to +85 °C temperature range.

Features

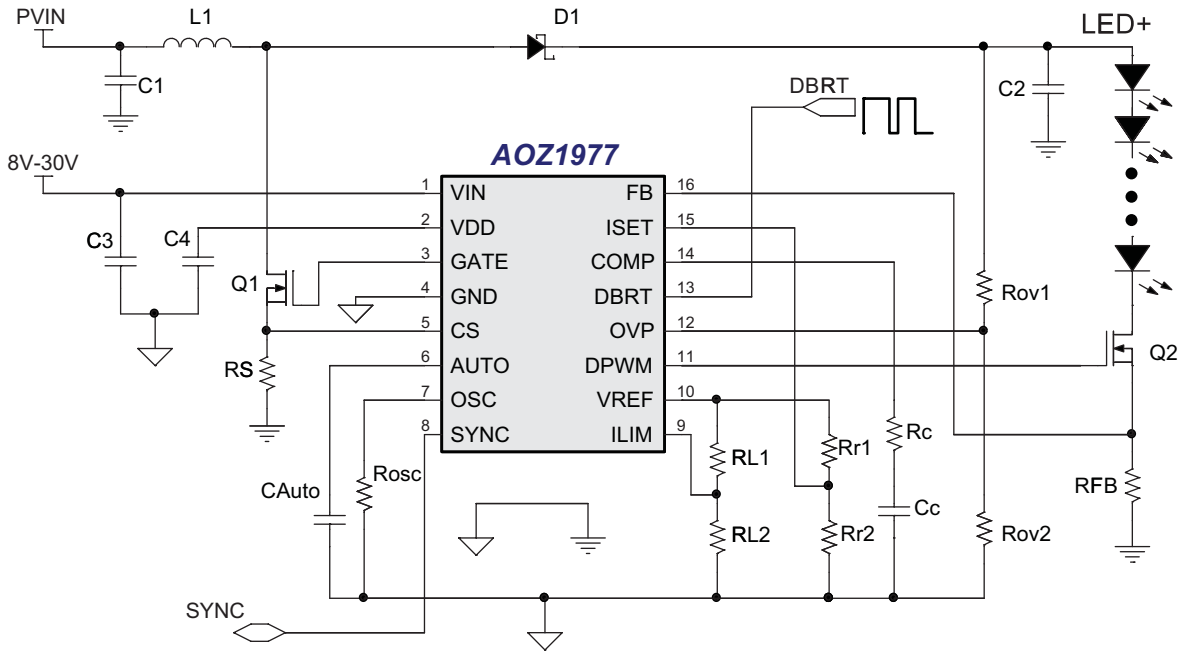
- 8 V to 30 V input bias voltage
- Up to 16 V driving capability at GATE pin and DPWM pin.
- Disconnect control pin for PWM dimming or fault conditions.
- Bi-directional clock synchronization
- 500 mV feedback regulation
- 8 bit PWM dimming resolution
- Cycle-by-cycle current limit
- Output over-voltage protection
- LED short and open protection
- Thermal shutdown protection
- SO-16 package

Applications

- LCD TV LED backlight
- Monitor LED backlight

Green Product

Typical Application

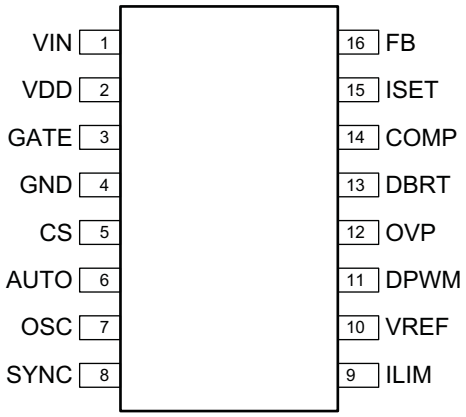


Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ1977AI	-40 °C to +85 °C	SOIC-16	Green Product

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/web/quality/rohs_compliant.jsp for additional information.

Pin Configuration



SOIC-16
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	VIN	Input supply pin.
2	VDD	Internal 8 V linear regulator output pin for date driver. Connect a minimum 0.22 μF ceramic capacitor from VDD to ground.
3	GATE	External boost NMOS gate controller pin. Connect to the gate of external NMOS switch.
4	GND	Ground pin.
5	CS	NMOS switch current sense pin.
6	AUTO	Auto restart mode control for protection. Connect appropriate capacitor to set desired Auto restart time or connect to GND for latch off.
7	OSC	Frequency set pin. Connect OSC to ground via a resistor to set the switching frequency.
8	SYNC	Frequency synchronous pin. Connect SYNC to external clock for desired switching frequency or connect to multiple controllers for phase locked frequency synchronization.
9	ILIM	Current limit set pin.
10	VREF	Reference voltage.
11	DPWM	Fault and dimming control output pin. DPWM = High for LED connect. DPWM = Low for LED disconnect. Connect to the gate of external NMOS switch.
12	OVP	Over-voltage feedback input pin. Use a voltage divider to set the boost regulator output over-voltage protection threshold.
13	DBRT	PWM brightness control input. DBRT controls the LED brightness by turning the LED on and off using a PWM signal. The brightness is proportional to the PWM duty cycle.
14	COMP	Compensation pin. COMP is the output of the internal error amplifier. For loop compensation connect a RC network from COMP to ground.
15	ISET	LED current set pin. Connect ISET to VREF resistor divider to set the LED current level.
16	FB	Feedback input pin. Connect to sense resistor at LED string.

Pin Functions

Pin 1: VIN

This is the input power for the controller IC. If the input of the boost converter is less than 30 V, VIN can be connected directly to the boost supply voltage. If the boost supply voltage is higher than 30 V, a separate supply rail between 8 V to 30 V is required for the VIN pin. It is recommended that an RC filter is added between VIN and the boost supply voltage if they are connected directly.

Please note that when VIN is not directly connected to the boost supply voltage, proper power up sequence will be required. Boost supply voltage must be ready before powering up VIN. There is no power down sequence required.

Pin 2: VDD

This is the output of an internal 8 V regulator. It requires a 2.2 μF decoupling capacitor to be connected to ground. The internal regulator can be over-driven by an external supply between 8 V to 16 V if higher gate drive is desired.

PIN3: GATE

This is the driver output for the gate of the boost NMOS switch. The GATE = high voltage is equal to VDD voltage. It is recommended to add a 1 Ω resistor between this pin and the NMOS gate. The resistor value can be optimized depending on the switching frequency and selection of the NMOS switch.

PIN 4: GND

This is the signal and power ground for the IC controller. It is recommended that all the low current paths are connected to this pin as close as possible to the IC controller. It is not recommended to connect any output or input filter capacitors and any current sense resistors to this pin directly. The IC controller ground should be an island around the IC connected to the PWR GND at a single point in the layout.

PIN 5: CS

This is the input for peak current sense. This pin serves the functions of current feedback, peak current limit detection, and fault current detection. The pin current limit is set by the voltage defined at PIN 9 ILIM. The current limit is defined as voltage at ILIM divided by the sense resistor connected from this pin to ground.

If the CS pin detect a fault current detection such as short circuit condition, it will trigger a fault signal. The IC controller sets to either latch-off mode or auto restart mode depends on the setting at PIN 6 AUTO.

PIN 6: AUTO

This is the mode control for fault condition. The selection of control when under fault condition is either auto restart mode or latch-off mode. For latch-off mode, this pin should be connected directly to ground. For auto restart mode, this pin should connect a capacitor to ground. The auto restart period will be determined by the following equation:

$$T_{AUTORESTART} = \frac{C(AUTO)}{1.25uA}$$

PIN 7: OSC

OSC is the pin to select the switching frequency for the boost controller. A resistor should be connected between this pin to ground. The switching frequency is determined by the following equation:

$$F_{SW} = \frac{1}{R_{OSC}\Omega \times 10pF}$$

It is recommended that the switching frequency for normal operation is between 50 kHz to 350 kHz.

Pin 8: SYNC

This is a bidirectional pin for oscillator clock synchronization. Clock synchronization will choose either the internal clock or the external clock through this pin, whichever is faster. The faster external clock must be ready before power is applied to this IC controller. If the internal clock is faster, the SYNC pin will have the same frequency as the internal clock. When multiple IC controllers are used in the design, it is recommended to connect all SYNC pins together. This will reduce the interference of “beat” frequencies associated with multiple switching frequencies.

PIN 9: ILIM

This is the current limit set point. The voltage at this pin will determine the CS current limit threshold detected at PIN 5: CS. The voltage can be derived from a resistor divider from the 1.2 V reference voltage at PIN 10: VREF. To minimize power consumption, it is recommended that the total resistance for the divider is approximately 20 kΩ.

PIN 10: VREF

This is a 1.2 V voltage reference for all external bias. This reference voltage can be used for PIN 15: ISET and PIN 9: ILIM bias.

PIN 11: DPWM

This is the driver output for the gate of the LED current control NMOS switch. DPWM = low if PIN13: DBRT signal is low or fault condition is triggered. DPWM = high if PIN 13: DBRT signal is high under normal operation. The high voltage is equal to VDD voltage. It is recommended to add a 1 Ω resistor between this pin and the NMOS gate. The resistor value can be optimized depending on the switching frequency and selection of the NMOS.

PIN 12: OVP

This is the input for LED Over-Voltage Protection. OVP monitors the LED output voltage through a resistor divider. When the voltage at this pin is higher than 1 V, the controller will stop switching immediately until the voltage at this pin is below 0.8 V.

PIN 13: DBRT

This is the input for digital brightness control. A PWM logic signal is applied to this pin to vary the brightness of the LED. The brightness of the LED is proportional to the duty cycle of the PWM logic signal. The input signal will control the output driver at DPWM pin. This input pin cannot be left floating.

PIN 14: COMP

This is for feedback loop compensation. It is the output of the error amplifier that controls PWM logic for the boost controller. An RC network should be used to generate the compensation for boost feedback loop.

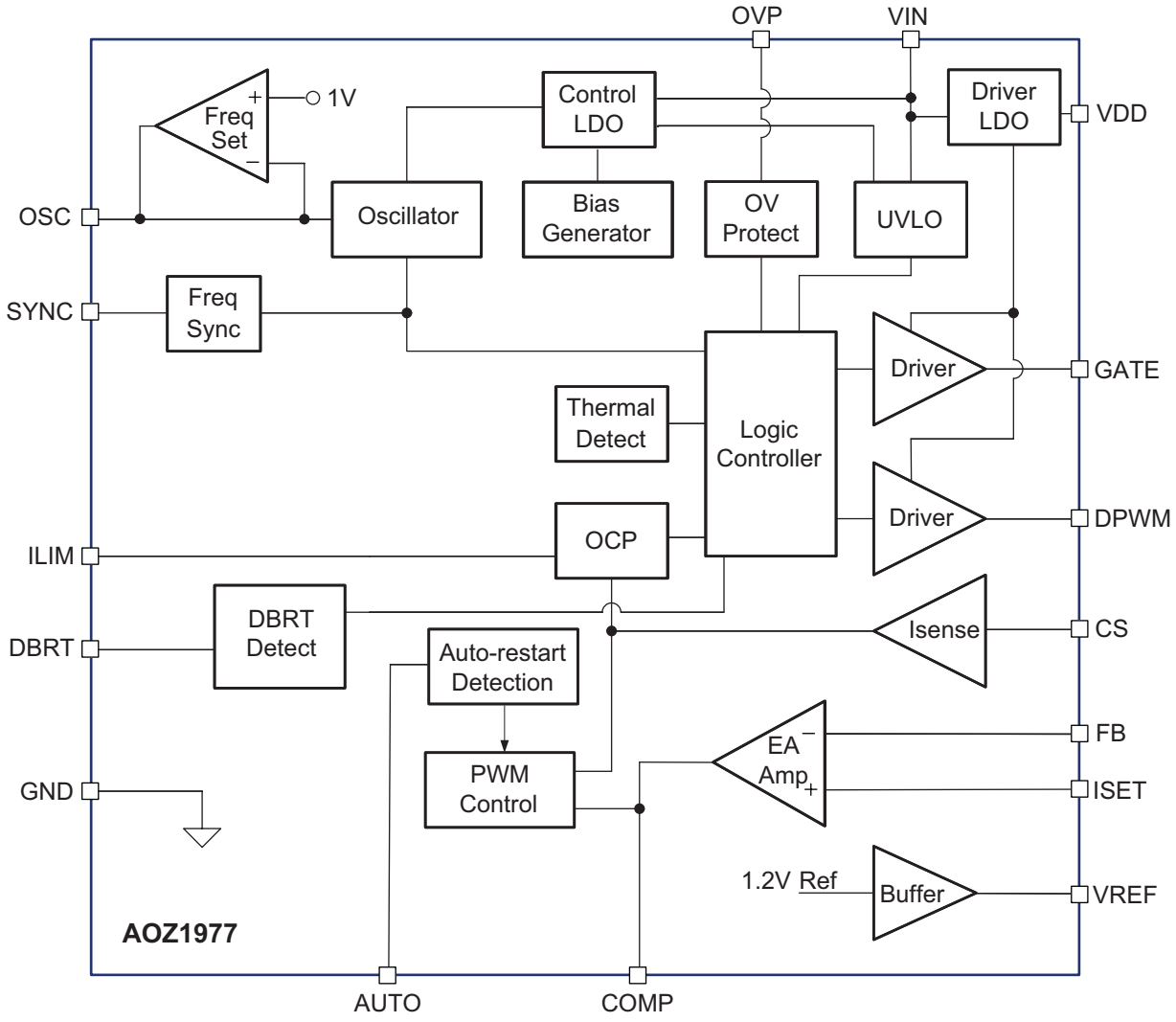
PIN 15: ISET

This is for full scale LED current setting. A reference voltage between 0.5 V and 0.8 V should be applied to this pin. The voltage can be derived from a resistor divider from the 1.2 V reference voltage at PIN 10: VREF.
To minimize power consumption, it is recommended that the total resistance for the divider is approximately 20 kΩ. The FB voltage will regulate to this voltage level. The full scale LED current is derived by the FB voltage divided by the Sense resistor.

PIN 16: FB

This is the feedback input for boost controller. This pin should connect to a resistor that senses the LED current. The FB voltage will be regulated to ISET voltage to determine the desired LED current when LED current control NMOS switch is on.

Block Diagram



Absolute Maximum Ratings

Exceeding the Absolute Maximum Ratings may damage the device.

Parameter	Rating
VIN to GND	-0.3 V to +32 V
GATE, DPWM to GND	-0.3 V to +16 V
VDD to GND	-0.3 V to +16 V
DBRT, OSC, ISET, COMP, FB, AUTO, SYNC, CS, ILIM, VREF, OVP to GND	-0.3 V to +6 V
Storage Temperature (T_S)	-65 °C to +150 °C
ESD Rating[1]	2 kV

Note:
1. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5 kΩ in series with 100 pF.

Recommended Operating Conditions

The device is not guaranteed to operate beyond the maximum Recommended Operating Conditions.

Parameter	Rating
Supply Voltage (V_{VIN})	8 V to 30 V
Ambient Temperature (T_A)	-40 °C to +85 °C
Package Thermal Resistance SOIC-16 (Θ_{JA})[2]	105 °C/W

Note:
2. The value of Θ_{JA} is measured with the device mounted on a 1-in^2 FR-4 board with 2 oz. Copper, in a still air environment with T_A = 25 °C. The value in any given application depends on the user's specific board design.

Electrical Characteristics

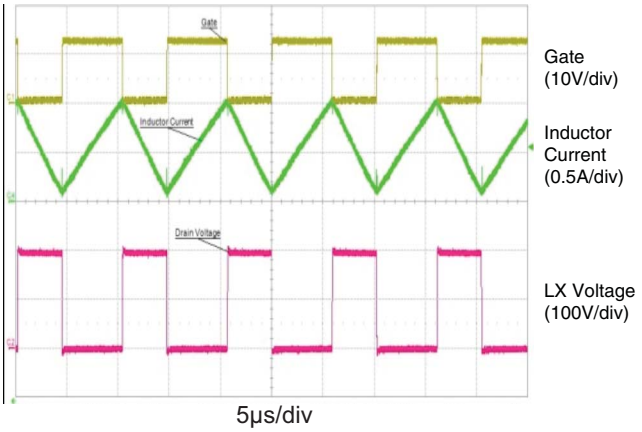
T_A = 25 °C, V_{VIN} = 24 V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
V_{VIN}	VIN Supply Voltage		8		30	V
I_{VIN_ON}	VIN Quiescent Current	Not Switching			2	mA
V_{UVLO_RISE}	VIN UVLO Threshold	VIN Rising		7	7.3	V
V_{UVLO_FALL}		VIN Falling	6.2	6.5		
V_{VIN_HYS}	VIN UVLO Hysteresis			500		mV
V_{VDD}	VDD Regulation Voltage	8.5 V < V_{VIN} < 30 V	7.5	8	8.5	V
OSCILLATOR						
F_{SW}	Switching Frequency	R_{OSC} = 1 MΩ	85	100	115	kHz
		R_{OSC} = 285 kΩ	298	350	402	kHz
T_{ON}	Minimum ON Time (PWM)	R_{OSC} = 1 MΩ		150	200	ns
GATE DRIVER						
I_{GATE_SOURCE}	Source Current	GATE = 0 V, VDD = 8 V	200	250		mA
I_{GATE_SINK}	Sink Current	GATE = 8 V, VDD = 8 V	400	450		mA
T_{GATE_RISE}	Rise Time	C_{GATE} = 1 nF, VDD = 8 V, 10 % to 90 % of VDD		50	85	ns
T_{GATE_FALL}	Fall Time	C_{GATE} = 1 nF, VDD = 8V, 90 % to 10 % of VDD		25	45	ns
INPUTS						
I_{CS}	CS Input Current	CS = 0.3 V			5	µA
I_{ISET}	ISET Input Current	ISET = 0.5 V			5	µA
I_{ILIM}	ILIM Input Current	ILIM = 0.4 V (140 % of CS)			5	µA
I_{DBRT}	DBRT Input Current	DBRT = 5 V			5	µA
I_{OVP}	OVP Input Current	OVP = 1.2 V			5	µA
I_{FB}	FB Input Current	FB = 0.5 V			5	µA
F_{DBRT}	DBRT Dimming Frequency	PWM duty cycle 0.1 % to 99.9 %	100		2000	Hz
OUTPUTS						
I_{VREF}	VREF Output Source Current	R_{VREF} = 6 kΩ to GND			200	µA
V_{VREF}	VREF Reference Voltage	R_{VREF} = 6 kΩ to GND	1.188	1.2	1.212	V
PROTECTION						
V_{ILIM}	Current Limit Set	CS = 0.3 V	120	133	146	% of V_{CS}
V_{OVP}	OVP Threshold Voltage		0.9	1	1.1	V
V_{OVP_HYS}	OVP Hysteresis			200		mV
I_{AUTO}	Auto-Restart Charge Current			1.25		µA
$T_{THERMAL\_SD}$	Thermal Shutdown Threshold			145		°C
$T_{THERMAL\_HYS}$	Thermal Shutdown Hysteresis			35		°C
DPWM DRIVE						
I_{DPWM_SOURCE}	DPWM Source current	GATE = 0 V	36			mA
I_{DPWM_SINK}	DPWM Sink current	GATE = 8 V	46			mA
LOGIC INPUT						
V_{DBRT_HI}	DBRT Logic High		2.0			V
V_{DBRT_LO}	DBRT Logic Low				0.8	V

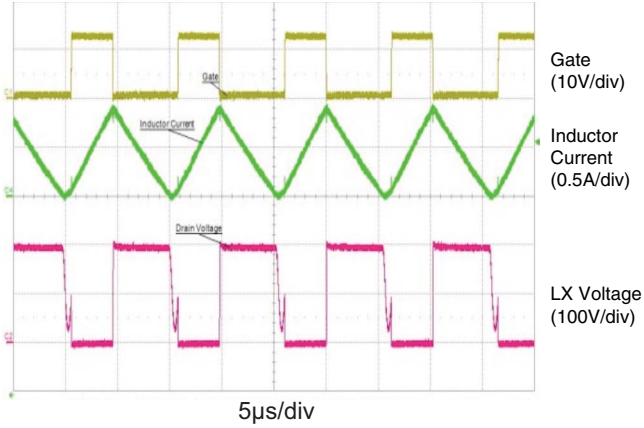
Typical Performance Characteristics

Switching Waveforms of Gate, Inductor Current and LX Voltage OUT = 195 V, LED = 200 mA

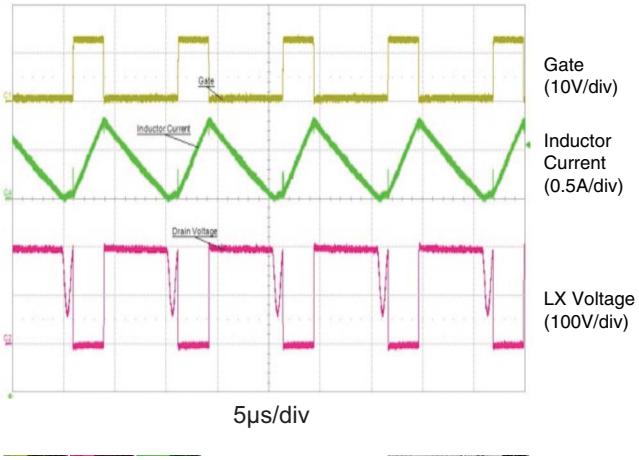
PVIN = 85V



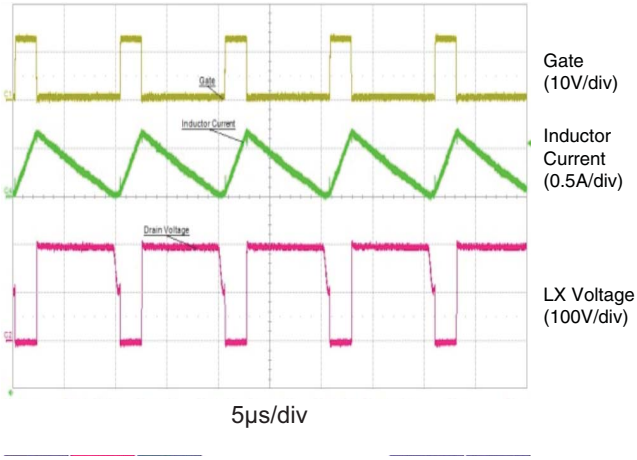
PVIN = 110V



PVIN = 130V

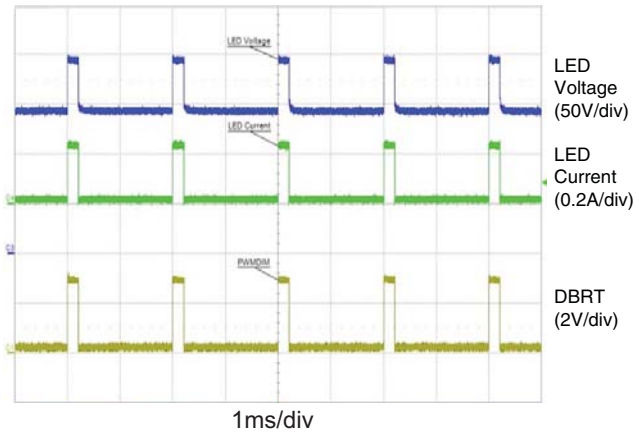


PVIN = 150V

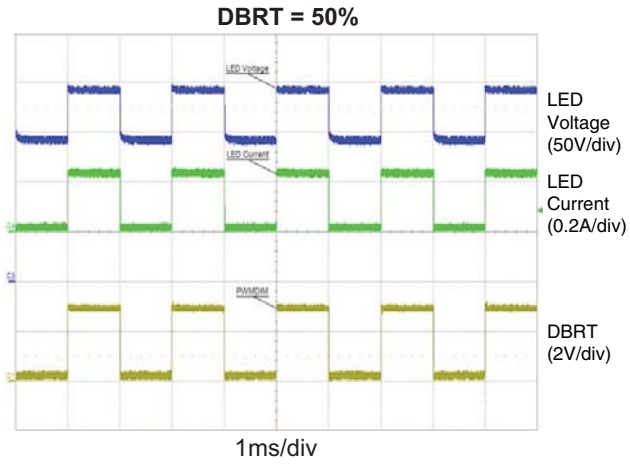


PWM Dimming Waveforms for PVIN = 130 V, VOUT = 195 V, ILED = 0.2 A, DBRT = 400 Hz

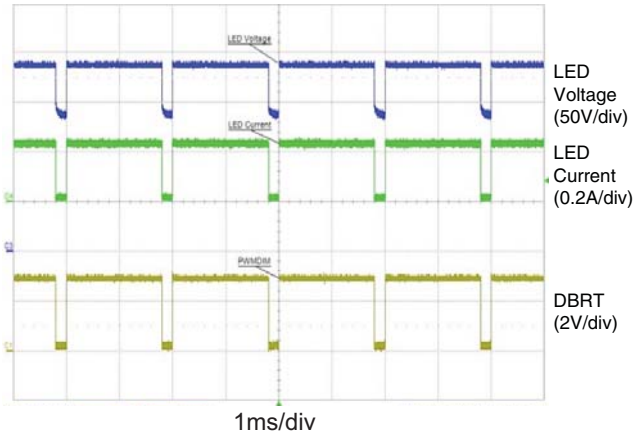
DBRT = 10%



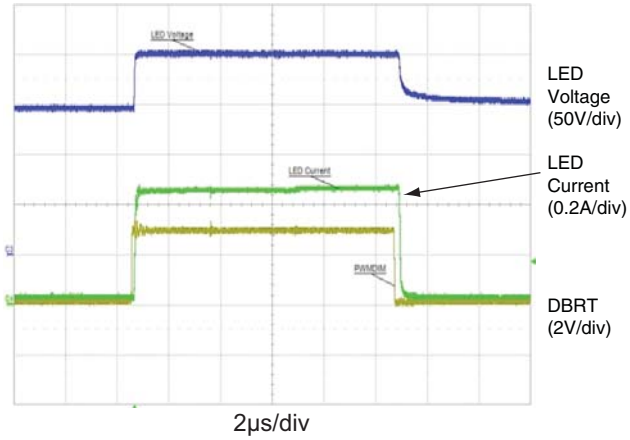
DBRT = 50%



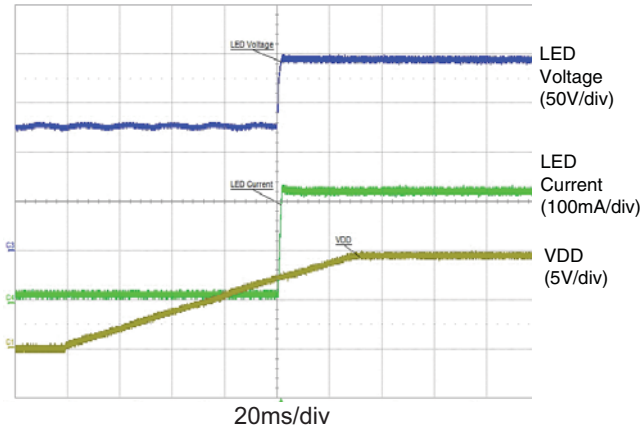
DBRT = 90%



Zoomed DBRT = 0.5%

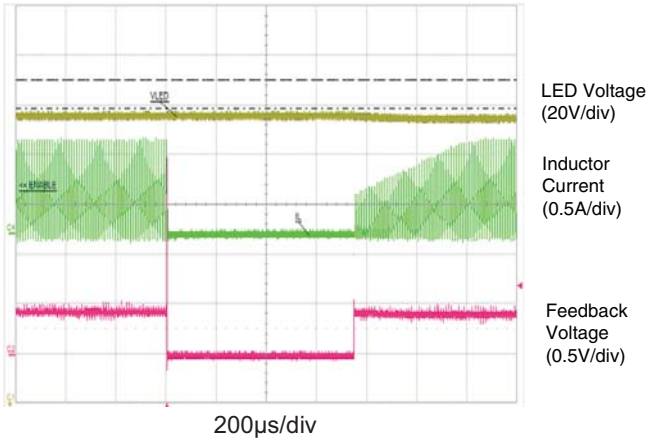


PVIN = 130 V, VOUT = 195 V, ILED = 0.2 A, DBRT Duty Cycle = 100%

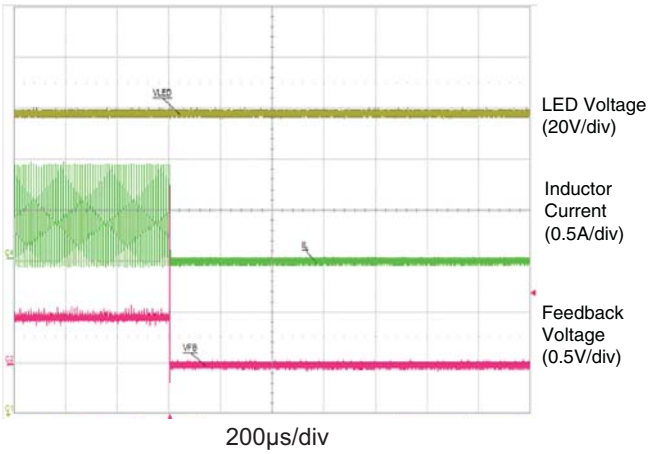


Additional Waveforms

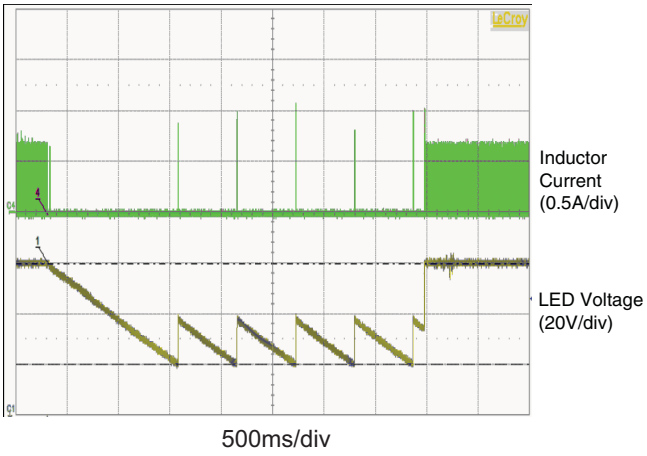
Non-latching LED Short Protection, Pin 6 AUTO Connected to 1nF



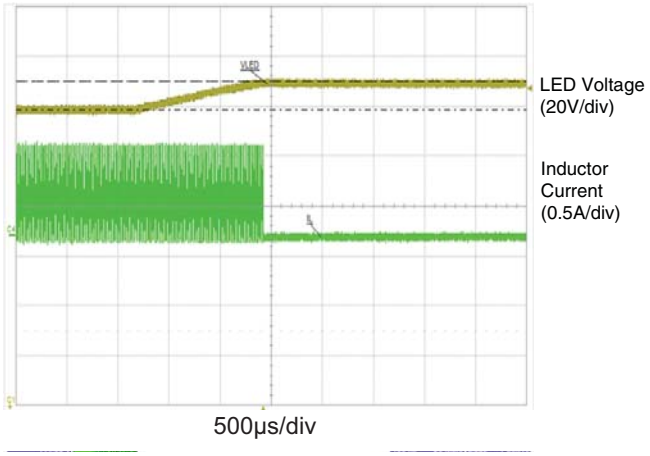
Latching LED Short Protection, Pin 6 AUTO Connected to GND



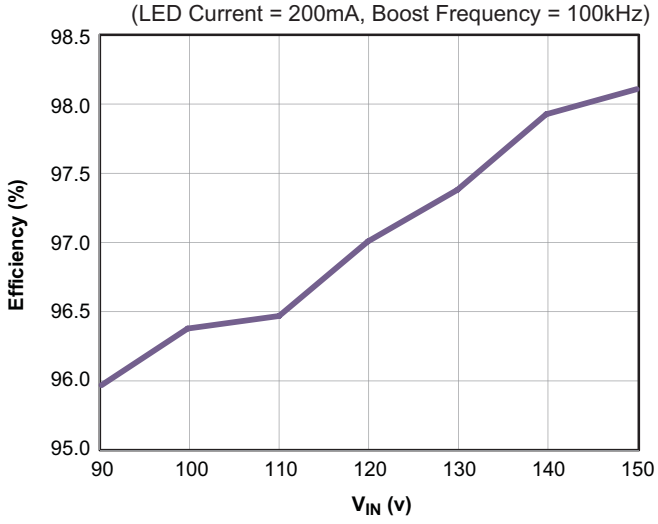
LED Short and Recovery



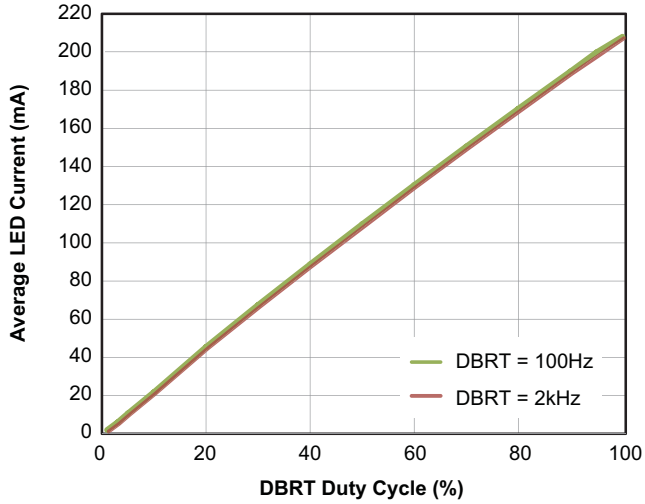
Non-latching OVP Protection



Efficiency vs. V_{IN} @ OUT = 195V
(LED Current = 200mA, Boost Frequency = 100kHz)



DBRT Control Linearity
(PVIN = 130V, VOUT = 195V)



Detailed Description

The AOZ1977 is a boost DC/DC controller designed to power a series of LEDs by regulating the current into the LED string. The LED current information is provided to the system through the sense resistor RFB at the bottom of the LED string, between FB pin and GND pin.

Protection Features

Over-Current Protection at Boost Switch

The current limit is a function of RS resistor value at CS pin and the voltage setting at ILIM pin. The voltage at ILIM is directly compared to the sense voltage at CS pin. When CS voltage reaches ILIM set voltage, current limit protection triggers and the boost switch will be turned off immediately until the next clock cycle. To make sure that current limit protection does not affect the normal operation, the current limit should be set at least 30 % higher than the inductor peak current. However, the voltage at ILIM must be less than 0.4 V. When CS voltage is higher than 0.4V, fault detection is active and that may affect normal operation. ILIM voltage is generated by connecting a resistor divider (RL1 and RL2 in the Typical Application diagram on page 1) from 1.2 V VREF pin to ILIM and GND pins. To minimize power consumption, it is recommended that the total resistance for the divider is approximately 20 kΩ.

For example,

- If peak current is 0.55 A.
- 30% higher is 0.72 A.
- CS voltage is 0.72 V x 0.55 Ω = 0.4 V.

Over-Voltage Protection at Output

Over-voltage protection is monitoring the LED output voltage through a resistor divider (Rov1 and Rov2 on page 1) from VOUT to OVP and GND pins. When the voltage at this pin is higher than 1 V, the controller will stop switching immediately until the voltage at this pin is below 0.8 V.

LED Short Protection

When FB voltage is higher than 1 V when LED current control switch is ON, the system will consider some LEDs are shorted instantaneously. Under this condition, the controller will enter the fault state.

LED Open Protection

When all LEDs are open, the system will respond by boosting the output voltage. Once the output voltage reaches the OVP threshold, OVP protection will trigger.

Latch Off or Auto Restart Mode

AOZ1977 can select either auto restart mode or latch-off mode under fault condition. Typical fault conditions are excessive current at boost switch, or LED short. For latch-off mode, the AUTO pin can be connected directly to ground. For auto restart mode, the AUTO pin should connect a capacitor to ground. The auto restart period will be determined by the following equation:

$$T_{AUTORESTART} = \frac{C(AUTO)}{1.25uA}$$

Thermal Protection

An internal temperature sensor monitors the junction temperature. It shuts down the internal control circuit and all drivers if the junction temperature exceeds 145 ºC.

Application Information

Inductor Selection

Inductor choice will be affected by many parameters, including duty cycle based on input/output setting, switching frequency, full scale LED current level, and mode of operations. The boost controller can operate under discontinuous mode, continuous mode, or critical conduction mode. For high voltage boost LED driver applications, it is recommended to use critical conduction mode for good stability and best efficiency.

Inductor Current in Critical Conduction Mode

In critical conduction mode:

$$ILpeak = di = 2 \times Iin$$

The duty cycle for the boost DC/DC system is defined as:

$$DutyCycle = D = \frac{Vout - Vin}{Vin}$$

To determine the ON time for the boost switch:

$$ONtime = dt = \frac{D}{Fsw}$$

For the application with VIN = 130 V, VOUT = 180 V, LED current = 200mA:

$$Iin = \frac{180V \times 0.2A}{130V} = 0.277A$$

$$di = 2 \times 0.227A = 0.555A$$

$$D = \frac{180V - 130V}{180V} = 0.28$$

$$dt = \frac{0.28}{100kHz} = 0.28us$$

The inductor value is determined by:

$$L = \frac{dt \times Vin}{di} = \frac{2.8us \times 130V}{0.555A} = 656uH$$

After the inductor value is calculated, we need to consider the DCR resistance and the Isat saturation current of the inductor. Inductor DCR is inversely proportional to the Isat. It is recommended to select an inductor for which the Isat value should be at least 50 % higher than the ILpeak value. To minimize the EMI effect, it is always preferable to use shielded type inductors.

Diode Selection

It is recommended to use fast recovery diode for D1. For most applications, Schottky diodes with correct current and voltage ratings are suitable. The diode current rating should be at least higher than the full scale LED current. The diode voltage rating should be higher than the OVP level of VOUT voltage.

Output Capacitors

The amount and type of capacitor used is mainly determined by the design output ripple requirement, and mainly by the output ripple current which is usually higher for boost converters and equals:

$$Iripple = \frac{\sqrt{Vout - Vin}}{Vin}$$

When selecting output capacitors, it is more important to check the effective ESR of the capacitor than the actual capacitance value. For example, a 10 μF capacitor with 0.02 Ω ESR will handle higher ripple current but produce less output ripple than a 33 μF capacitor with 0.04 Ω ESR. It is recommended to use low ESR MLCC ceramic capacitors. For high voltage cost effective application, multiple Electrolytic capacitors in parallel will reduce the total effective ESR.

Input Capacitors

The input capacitors for boost converters do not require low ESR due to the fact that the input current is continuous. Also, they do not contain large peak current as compared to the output capacitors.

The ripple current at the input capacitor is:

$$Iin\_ripple = \frac{0.3 \times Vin \times (Vout - Vin)}{Fsw \times L \times Vout}$$

where Fsw is the switching frequency, 100 kHz in this example.

Electrolytic capacitors should work well with the appropriate voltage and ripple current rating, it is not recommended to use Tantalum capacitors because Boost converters do exhibit high surge currents during startup which can cause tantalum capacitors to fail.

Current Sense Resistors

There are two current sense resistors in this application, an LED current sense resistor RFB and a Boost switch current sense resistor RS.

RFB LED current sense resistor is set by:

$$RFB = \frac{ISET\ Voltage}{LED\ Current} = \frac{0.5V}{0.2A} = 2.5\Omega$$

LED current is a function of ISET voltage and RFB resistance. ISET voltage is generated by connecting a resistor divider (Rr1 and Rr2 on page 1) from 1.2 V VREF pin to ISET and GND pins. To minimize power consumption, it is recommended that the total resistance for the divider is approximately 20 kΩ.

RS boost switch current sense resistor is set by:

$$RS = \frac{0.3V}{LEDInductor\ Peak\ Current} = \frac{0.3V}{0.55A} = 0.55\Omega$$

For typical application, it is recommend to set the voltage at CS to approximately 0.3 V when inductor current reaches the peak.

Boost Feedback Loop Compensation

The AOZ1977 employs peak current mode control for easy use and fast transient response. Peak current mode control eliminates the double pole effect of the output L&C filter. It greatly simplifies the compensation loop design.

With peak current mode control, the boost power stage can be simplified to be a one-pole, one left plane zero and one right half plane (RHP) system in frequency domain. The pole is the dominant pole and can be calculated by:

$$f_{P1} = \frac{1}{2\pi \times C_O \times R_L}$$

The zero is a ESR zero due to the output capacitor and its ESR. It is can be calculated by:

$$f_{Z1} = \frac{1}{2\pi \times C_O \times ESR_{CO}}$$

where;

C_O is the output filter capacitor,

R_L is load resistor value, and

ESR_{CO} is the equivalent series resistance of output capacitor.

The RHP zero has the effect of a zero in the gain causing an imposed +20 dB/decade on the roll off, but has the effect of a pole in the phase, subtracting 90° in the phase. The RHP zero can be calculated by:

$$f_{Z2} = \frac{V_{IN}^2}{2\pi \times L \times I_O \times V_O}$$

The RHP zero obviously can cause the instable issue if the bandwidth is higher. It is recommended to design the bandwidth to lower than the one half frequency of RHP zero.

The compensation design is actually to shape the converter close loop transfer function to get desired gain and phase. Several different types of compensation network can be used for AOZ1977. For most cases, a series capacitor and resistor network connected to the COMP pin sets the pole-zero and is adequate for a stable high-bandwidth control loop.

In the AOZ1977, FB pin and COMP pin are the inverting input and the output of internal transconductance error amplifier. A series R and C compensation network connected to COMP provides one pole and one zero. The pole is:

$$f_{P2} = \frac{G_{EA}}{2\pi \times C_C \times G_{VEA}}$$

where;

G_{EA} is the error amplifier transconductance, which is 200×10^{-6} A/V,

G_{VEA} is the error amplifier voltage gain, which is 340 V/V, and

C_C is the compensation capacitor.

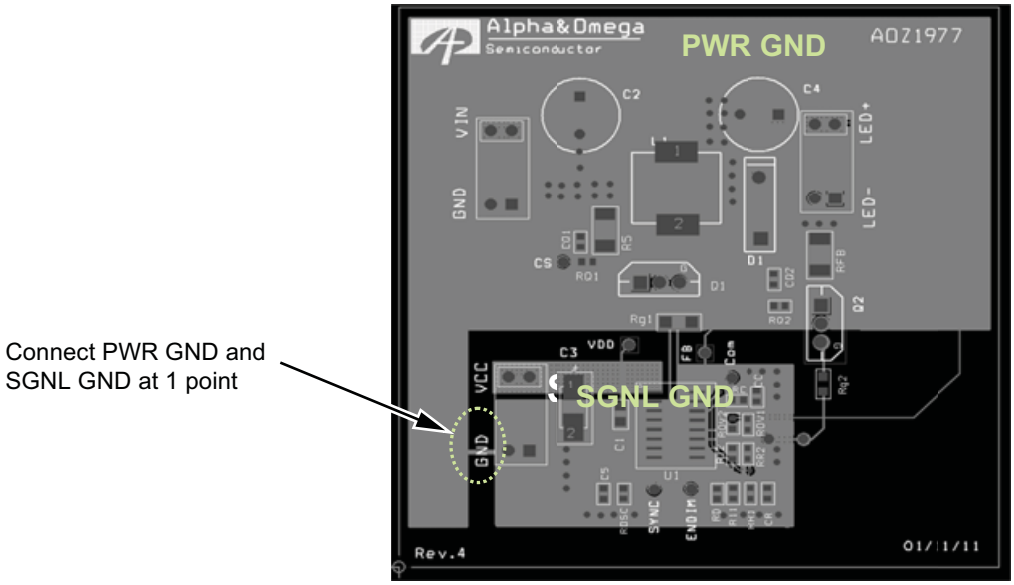
The zero given by the external compensation network, capacitor C_C and resistor R_C is located at:

$$f_{Z2} = \frac{1}{2\pi \times C_C \times R_C}$$

Choosing the suitable C_C and R_C by trading-off stability and bandwidth.

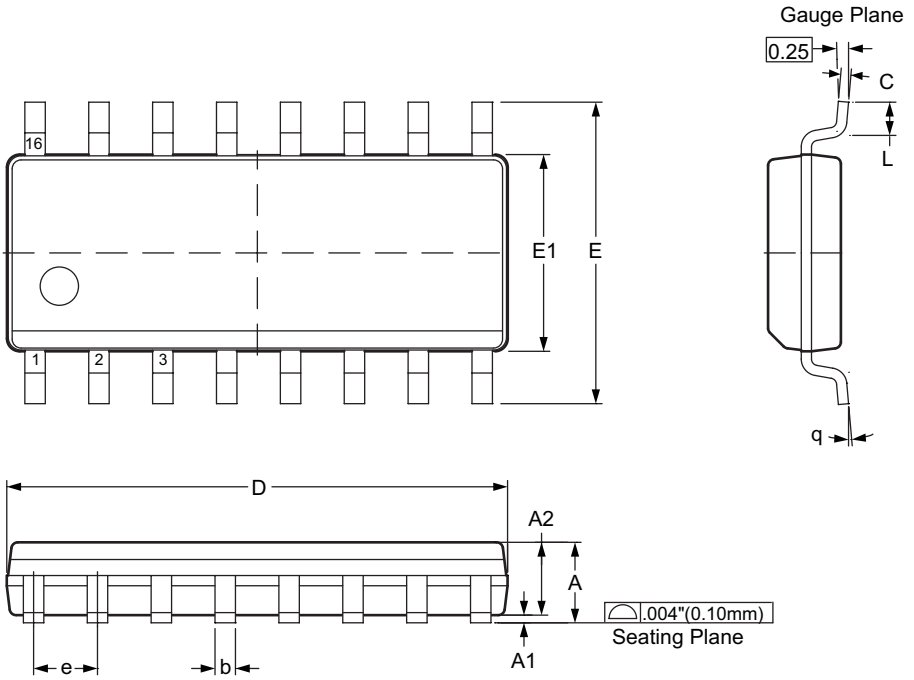
PCB Layout Consideration

Correct layout practices are essential for a working design that will meet expectations. It is recommended to use a two-layer board for the design. However, a single layer board would be sufficient if basic layout rules are followed. In any SMPS layout, external components should be grouped into Power or IC control. From typical application circuit, there are two GND symbols. The striped one is for Power GND and the solid one is for Signal/Control GND. Both symbols are connected to a single point connection on the layout, All Power connections should be as short and wide as possible in order to reduce undesired parasitic inductance. The output capacitors should be physically placed in the current path between the SMPS and the load. Input capacitors should be placed as close as possible to the input side of the inductor. To prevent interference and system noise, it is critical that the switch node connection for boost switch, inductor, and output diode must be as short and close as possible. A GND copper layer covers the top layer to help shield the noise. For two-layer board, it is essential that the GND plane under this switching node should be filled and uninterrupted.

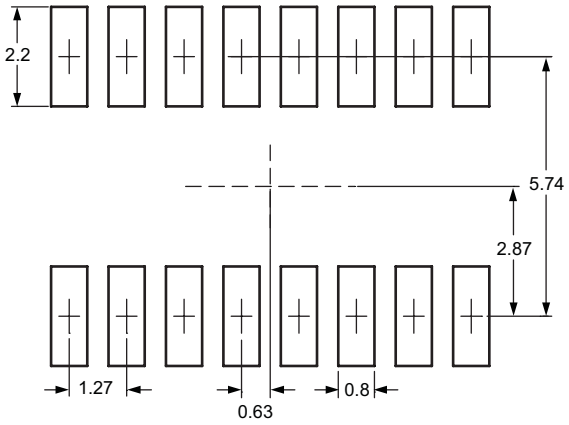


Single Point Connection Connecting PWR GND and Signal GND

Package Dimensions, SOIC, 16L



RECOMMENDED LAND PATTERN



UNIT: mm

Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	1.35	1.60	1.75
A1	0.10	—	0.25
A2	—	1.45	—
b	0.33	—	0.51
C	0.19	—	0.25
D	9.80	—	10.00
E1	3.80	3.90	4.00
e	1.27 TYP		
E	5.80	6.00	6.20
L	0.40	—	1.27
θ	0°	—	8°

Dimensions in inches

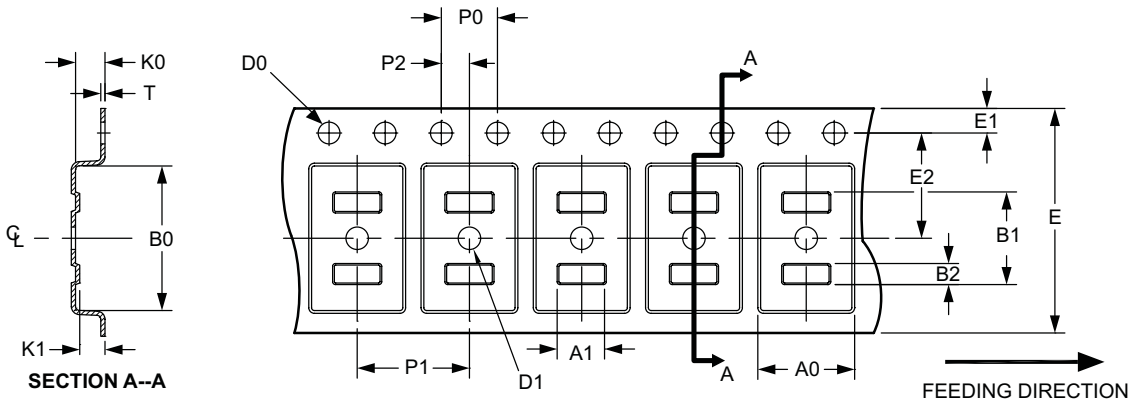
Symbols	Min.	Nom.	Max.
A	0.053	0.063	0.069
A1	0.004	—	0.010
A2	—	0.057	—
b	0.013	—	0.020
C	0.007	—	0.010
D	0.386	—	0.394
E1	0.150	0.154	0.157
e	0.050 TYP		
E	0.228	0.236	0.244
L	0.016	—	0.050
θ	0°	—	8°

Notes:

1. All dimensions are in millimeters.
2. Dimensions are inclusive of plating
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 6 mils.
2. Dimension L is measured in gauge plane.
3. Tolerance is 0.10mm unless otherwise specified.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

Tape and Reel Dimensions, SOIC, 16L

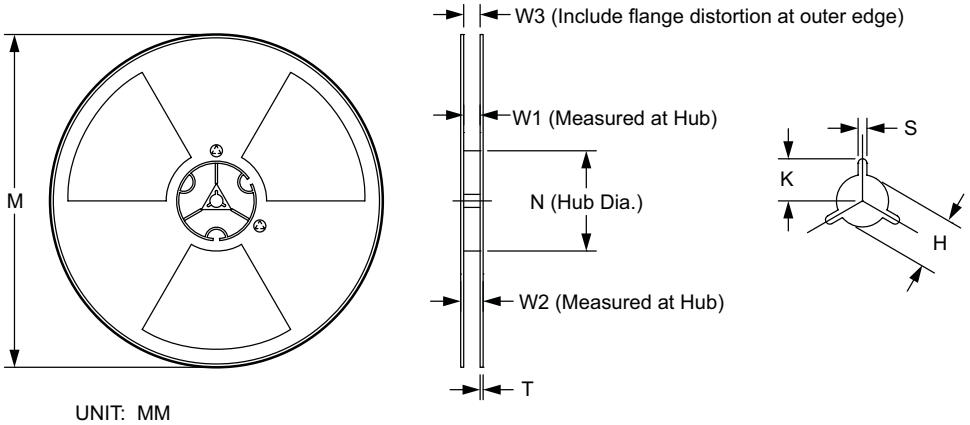
Carrier Tape



UNIT: MM

Package	A0	B0	K0	K1	D0	D1	E	E1	E2	P0	P1	P2	T	B1	B2	A1
SO16 (16 mm)	6.50 ±0.1	10.30 ±0.1	2.30 ±0.1	1.80 ±0.1	1.55 ±0.05	1.6 ±0.1	16.00 ±0.3	1.75 ±0.1	7.50 ±0.1	4.0 ±0.1	8.00 ±0.1	2.0 ±0.1	0.3 ±0.05	REF. 6.6	REF. 1.5	REF. 3.5

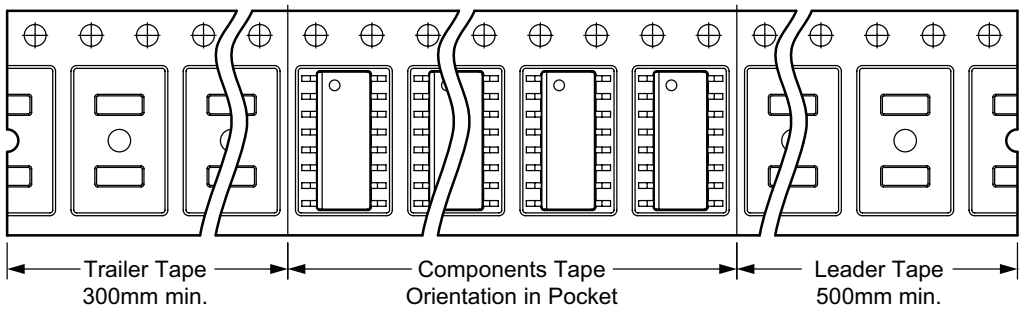
Reel



UNIT: MM

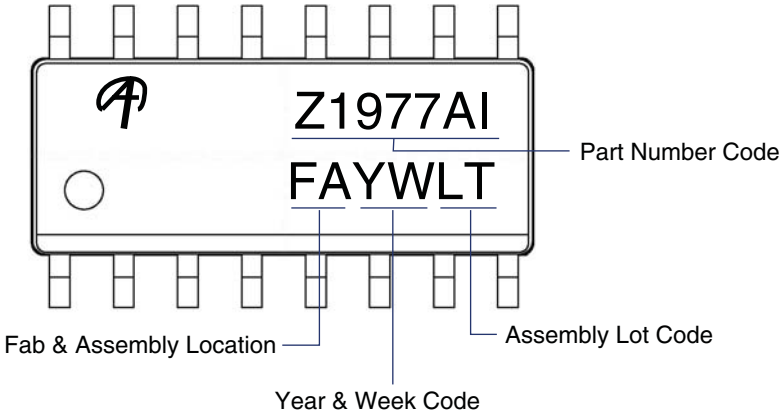
Tape Size	M	N	T	W1	W2	W3	S	K	H
16mm	Ø332 MAX.	Ø100.0 ±2.0	2.0 ±0.5	16.4 +2.0 -0	22.4 MAX.	15.9~19.4	2.2 TYP.	10.1 MIN.	Ø13.0 ±0.2

Leader/Trailer and Orientation



Part Marking

AOZ1977AI
(SOIC-16)



This datasheet contains preliminary data; supplementary data may be published at a later date.
Alpha & Omega Semiconductor reserves the right to make changes at any time without notice.