28V Programmable Current-Limited Load Switch

Preliminary DATASHEET

(Specifications subject to change)

General Description

The AOZ1360 is a member of Alpha and Omega Semiconductor's high-side load switch family intended for applications that require circuit protection. The device operates from voltages between 5.5V and 28V, and can handle a continuous current up to 3A. The internal current limiting circuit protects the input supply voltage from large load current. The current limit can be set with an external resistor. The AOZ1360 provides thermal protection function that limits excessive power dissipation. The device employs internal soft-start circuitry to control inrush current due to highly capacitive loads associated with hot-plug events. It features low quiescent current of 220µA and the supply current reduces to less than 1µA in shutdown.

The AOZ1360 is available in the SO-8 & 4x4DFN-10 package which can operate over -40°C to +85°C temperature range.

Features

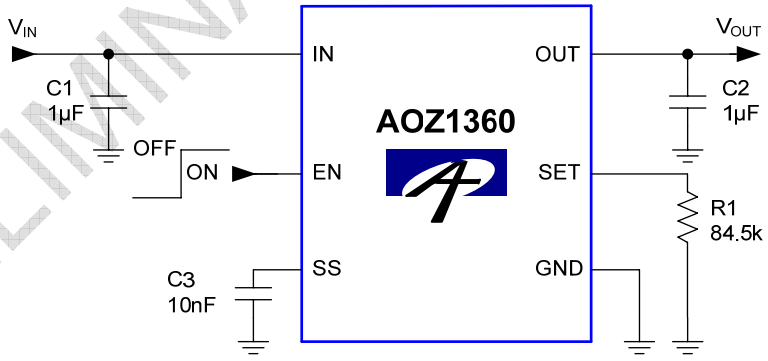
- 35mΩ maximum on resistance
- 2A minimum continuous current.
- Programmable current limit
- 5.5V to 28V operating input voltage
- Low quiescent current
- Under-voltage lockout
- Thermal shutdown protection
- 2.5kV ESD rating
- Available in SO-8 and 4mm x4mm DFN-10 package

Applications

- Notebook PCs
- Hot swap supplies

RoHS Compliant

Typical Application Circuit



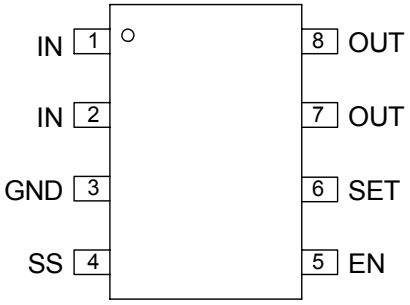
Ordering Information

Part Number	Package	Temperature Range	Environmental
AOZ1360AI	SO-8	-40°C to +85°C	RoHS
AOZ1360DI	DFN4x4 10L	-40°C to +85°C	RoHS

All AOS products are offered in packages with Pb-free plating and compliant to RoHS standards.
Parts marked as Green Products (with "L" suffix) use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/web/quality/rohs_compliant.jsp for additional information.

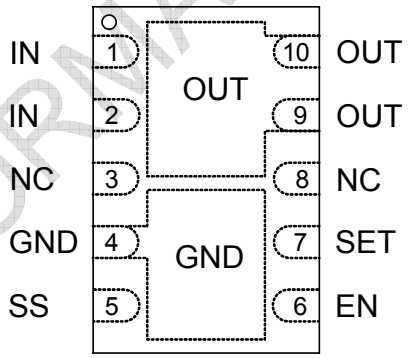
Pin Configuration

TOP VIEW



SO-8

TOP VIEW



DFN4X4 10L

Note: Connect all IN pins externally.

Pin Description

SO-8 Pin Number	DFN4x4 10L Pin Number	Pin Name	Pin Function
1,2	1,2	IN	P-channel MOSFET source. Connect a 1uF capacitor from IN to GND.
3	4	GND	Ground.
4	5	SS	Soft-Start Pin. Connect a capacitor from SS to GND to set the soft-start time. Connect SS to IN to set to the default soft-start time of 100us.
5	6	EN	Enable Input. Two options are available: active high and active low. See Ordering Information for details.
6	7	SET	Current Limit Set Pin. Connect a resistor from SET to GND to set the switch current limit.
	3,8	NC	No Connect
7,8	9,10	OUT	P-channel MOSFET Drain. Connect a 0.1uF capacitor from OUT to GND.

Absolute Maximum Ratings[1]

IN to GND .....-0.3V to +30V
EN, SET, OUT to GND .....-0.3V to V_{IN} + 0.3V
SS, SET .....-0.3V to +6V
Maximum Continuous Current..... 3A
Maximum Junction Temperature (T_J).....+150°C
ESD Rating (HBM) 2.5kV

Operating Ratings

Thermal Resistance (SO-8).....82°C/W

Thermal Resistance (DFN4X4).....63°C/W

Electrical Characteristics

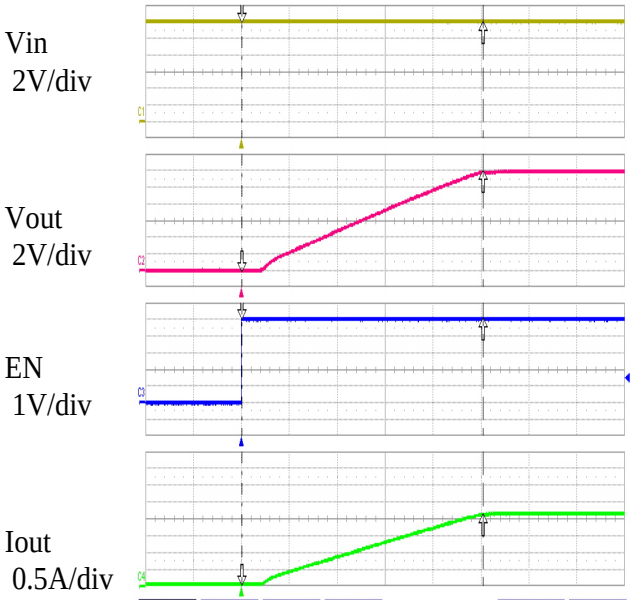
V_{IN} = 12V, T_A = -40°C to +85°C unless otherwise stated. Typical values are at 25°C

Parameter	Symbol	Conditions	MIN	TYP	MAX	UNITS
Input Supply Voltage	V_{IN}		5.5		28	V
Undervoltage Lockout Threshold	V_{UVLO}	IN rising		4.9	5.4	V
Undervoltage Lockout Hysteresis	V_{UVHYS}			400		mV
Input Quiescent Current	I_{IN_ON}	EN = IN for -00, EN = GND for -01, no load		220	400	µA
Input Shutdown Current	I_{IN_OFF}	EN = GND for -00, EN = IN for -01, no load			1	µA
Output Leakage Current	I_{LEAK}	EN = GND for -00, EN = IN for -01, no load			1	µA
Switch On Resistance	$R_{DS(ON)}$	AOZ1360AI V_{IN} = 12V		22	35	mΩ
Switch On Resistance	$R_{DS(ON)}$	AOZ1360AI V_{IN} = 5.5V		33	43	mΩ
Current Limit	I_{LIM}	R_{SET} = 84.5kΩ (SO8) R_{SET} = XXX kΩ (DFN)	2	2.7	3.4	A
Enable Input Low Voltage	V_{EN_H}				0.8	V
Enable Input High Voltage	V_{EN_L}		2.0			V
Enable Input Hysteresis	V_{EN_HYS}			100		mV
Enable Input Bias Current	I_{EN_BIAS}				1	µA
Turn-On Delay Time EN_50% to OUT_10%	**Td_on**	**R_L=120Ω, C_L = 1µF, SS = Floated**		**220[2]**		**µs**
Turn-On Rise Time **OUT_10% to 90%**	t_{ON}	**R_L=120Ω, C_L = 1µF, SS = Floated**		**280**		**µs**
		R_L=120Ω, C_L = 1µF, **C_{SS} = 1nF**		**360**		µs
Turn-Off Fall Time	t_{OFF}	**R_L=120Ω,** C_L = 1µF, **SS = Floated**		**280**		µs
Thermal Shutdown Threshold	T_{SD}			130		°C
Thermal Shutdown Hysteresis	T_{SD_HYS}			30		°C

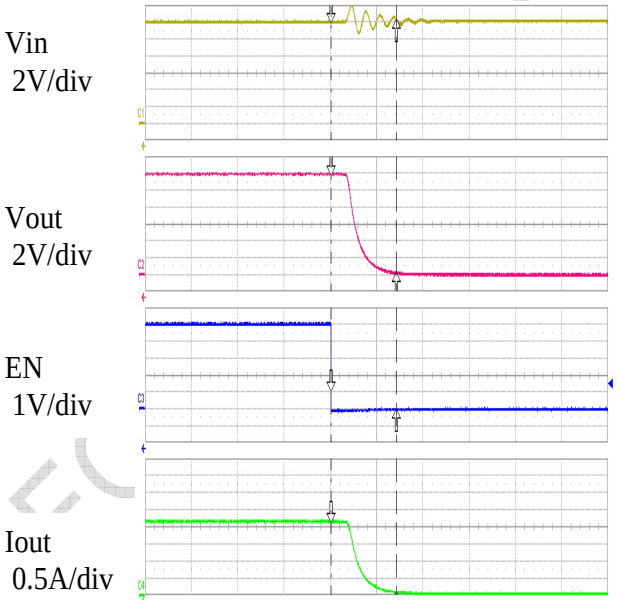
(1) Stresses beyond the Absolute Maximum Ratings may cause permanent damage to the device.
(2) Depends on the gate loading of the discrete PMOS, to be confirmed by silicon data.

Typical Operating Characteristics
Functional Characteristics

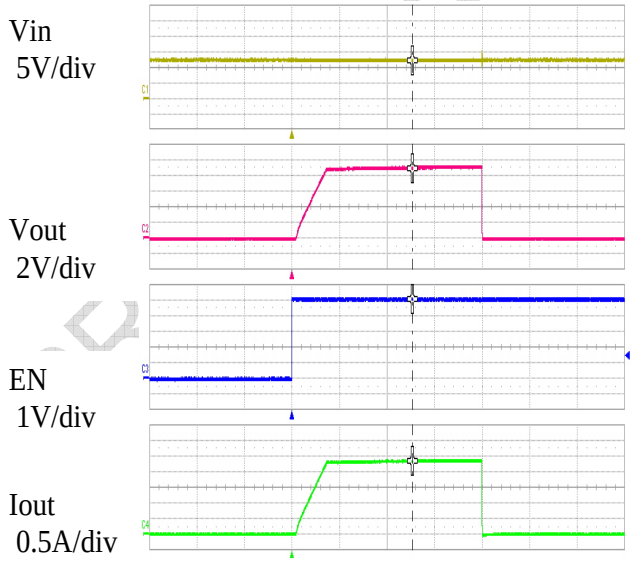
Turn-On
(Vin = 12V, R = 5.6Ω)



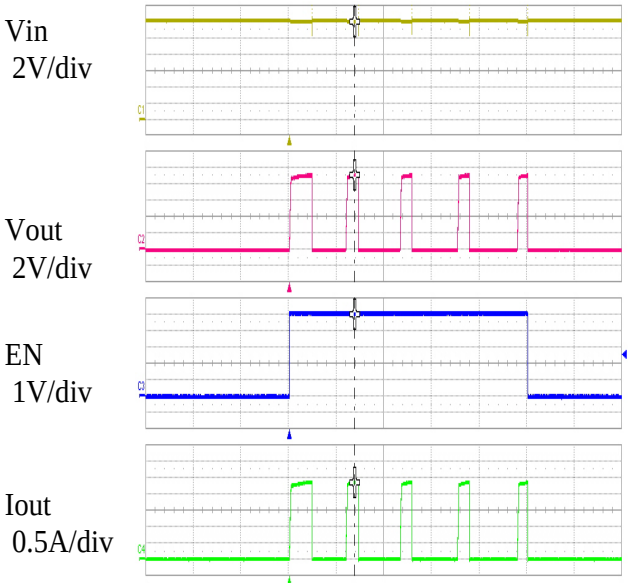
Turn-Off
(Vin = 12V, R = 5.6Ω)



Current Limit
(Vin = 12V, R = 3.6Ω)



Over Temperature
(Vin = 12V, R = 3.6Ω)



Timing Diagram

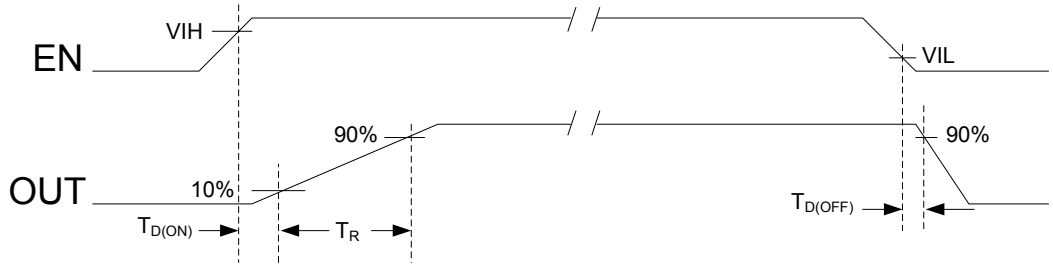


Figure 1 AOZ1360 Timing Diagram

Functional Block Diagram

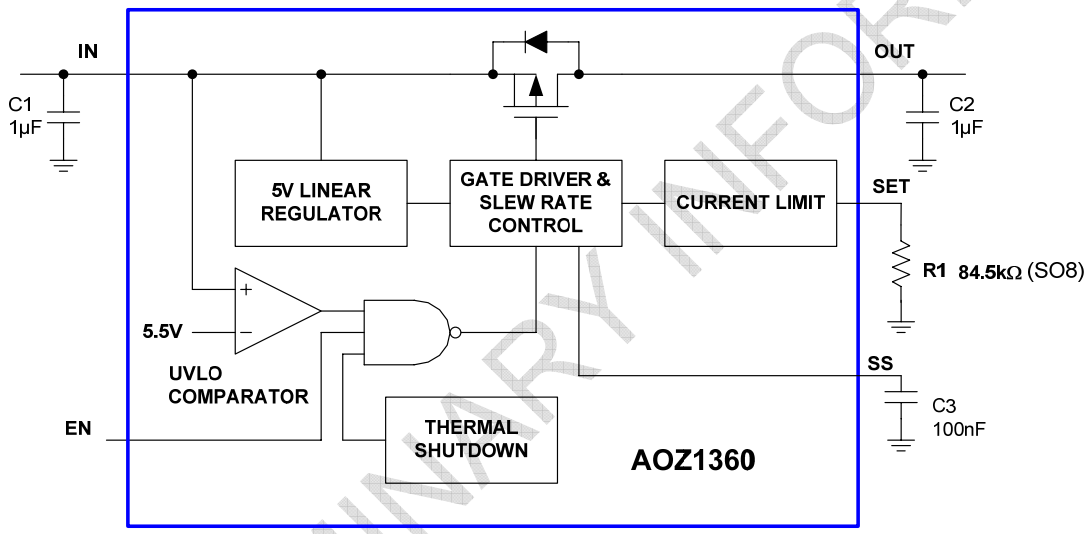


Figure 2 Functional Block Diagram

Detailed Description

Introduction

The AOZ1360 is a 35mΩ P-channel high-side load switch with adjustable soft-start slew-rate control, programmable current limit and thermal shutdown. It operates with an input voltage range from 5.5V to 28V and can handle a continuous current of 2A.

Enable

The Enable pin is the ON/OFF control for the output switch. It's an active-high input. The EN pin is active after V_{IN} is above the UVLO threshold of 4.9 V. Conversely, the Enable will be de-activated if the V_{IN} falls below the UVLO of 2.0V. The EN pin must be driven to a logic high or logic low state to guarantee operation. While disabled, the AOZ1360 only draws about 1uA supply current. The EN is a high impedance input with an ESD protection diode to ground and should not be forced below ground. This input level is compatible with most microcontroller outputs and other logic families.

Under-Voltage Lockout (UVLO)

The under-voltage lockout (UVLO) circuit of AOZ1300 monitors the input voltage and prevents the output MOSFET from turning on until VIN exceeds 4.9V.

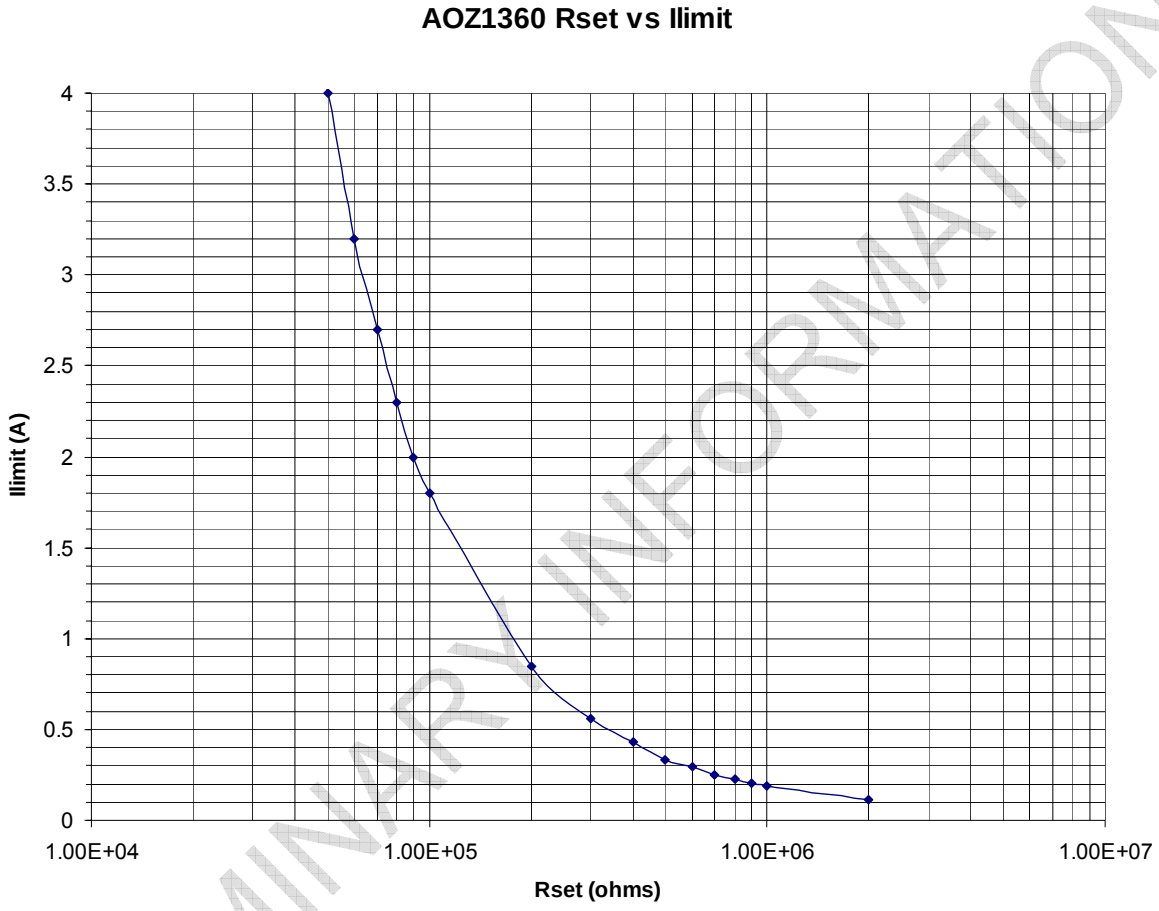
Adjustable Soft-Start Slew-Rate Control

When the EN pin is asserted high, the slew rate control circuitry applies voltage on the gate of the PMOS switch in a manner such that the output voltage and current is ramped up linearly until it reaches the steady-state load current level. The slew rate can be adjusted by an external capacitor connected to the SS pin to ground. The slew rate rise time, Ton, can be set using the following equation:

$$Ton = \frac{C_{SS} * V_{IN}}{30\mu A}$$

Programmable current Limit

The current limit is programmed by an external resistor connected to the SET pin to ground. This sets a reference voltage to the current limit error amplifier that compares it to a sensed voltage that is generated by passing a small portion of the load current through an internal amplifier. When the sensed load current exceeds the set current limit, the load current is then clamped at the set limit and the Vout drops to whatever voltage necessary to clamp the load current. The AOZ1360 will stay in this condition until the load current no longer exceeds the current limit or if the thermal shutdown protection is engaged. To set the current limit use the below graph



Thermal-Shutdown Protection

During current limit or short circuit conditions the PMOS resistance is increased to clamp the load current. This increases the power dissipation in the chip causing the die temperature to rise. When the die temperature reaches 130°C the thermal shutdown circuitry will shutdown the device. There is a 30°C hysterisys after which the device will turn back on and go thru soft start. The thermal shutdown will cycle repeatedly until the short circuit condition disappears or the enable pin is pulled LOW by an external monitor.

Applications Information

Input Capacitor Selection

Use a 1uF or larger capacitor for input bypassing. This will limit the input voltage drop during output transient conditions. 1uF capacitor should be adequate for most applications; however, higher capacitor values will further reduce the voltage drop. Place the bypass capacitor as close to the IN pins as feasibly possible.

Output Capacitor Selection

Use a 0.1uF or larger capacitor between the OUT and GND pins. The capacitance does not affect the turn on slew rate; however, a larger capacitor will make the initial turn on transient smoother.

Power Dissipation Calculation

Calculate the power dissipation for normal load condition using the following equation:

$P_D = R_{ON} \times (I_{OUT})^2$

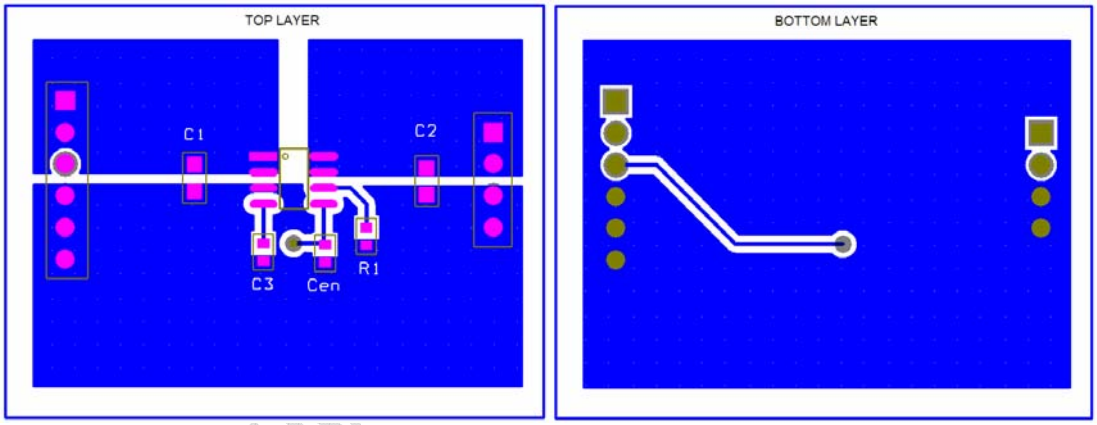
The worst case power dissipation occurs when the load current hits the current limit due to over-current or short circuit faults. The power dissipation under these conditions can be calculated using the following equation:

$P_D = (V_{IN} - V_{OUT}) \times I_{LIMIT}$

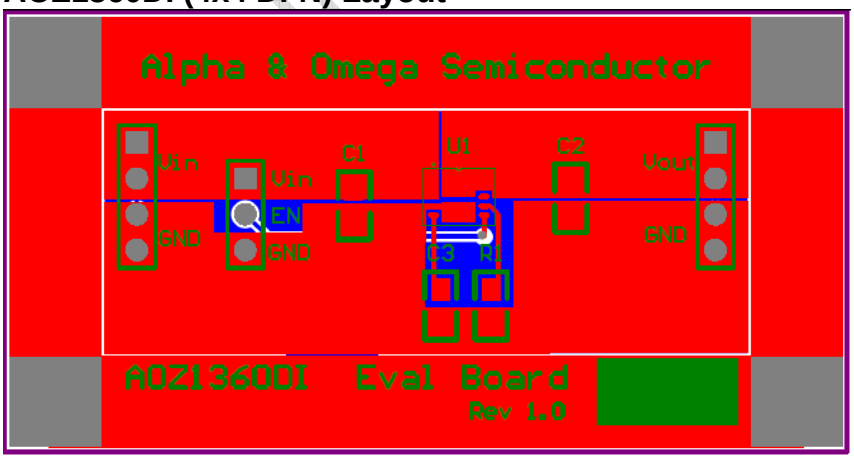
Layout Guidelines

Good PCB layout is important for improving the thermal and overall performance of AOZ1360. To optimize the switch response time to output short-circuit conditions keep all traces as short as possible to reduce the effect of unwanted parasitic inductance. Place the input and output bypass capacitors as close as possible to the IN and OUT pins. The input and output PCB traces should be as wide as possible for the given PCB space. Use a ground plane to enhance the power dissipation capability of the device.

AOZ1360AI (SO-8) Layout

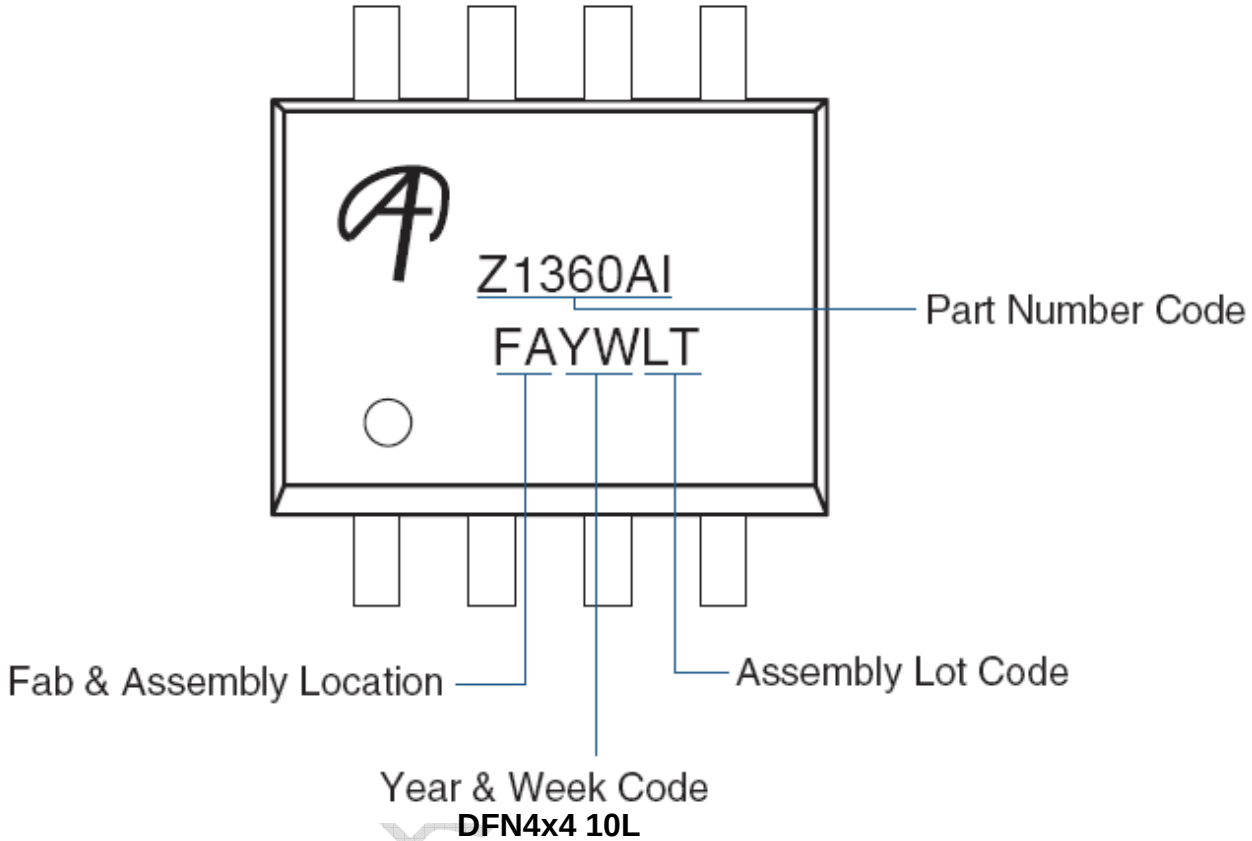


AOZ1360DI (4x4 DFN) Layout

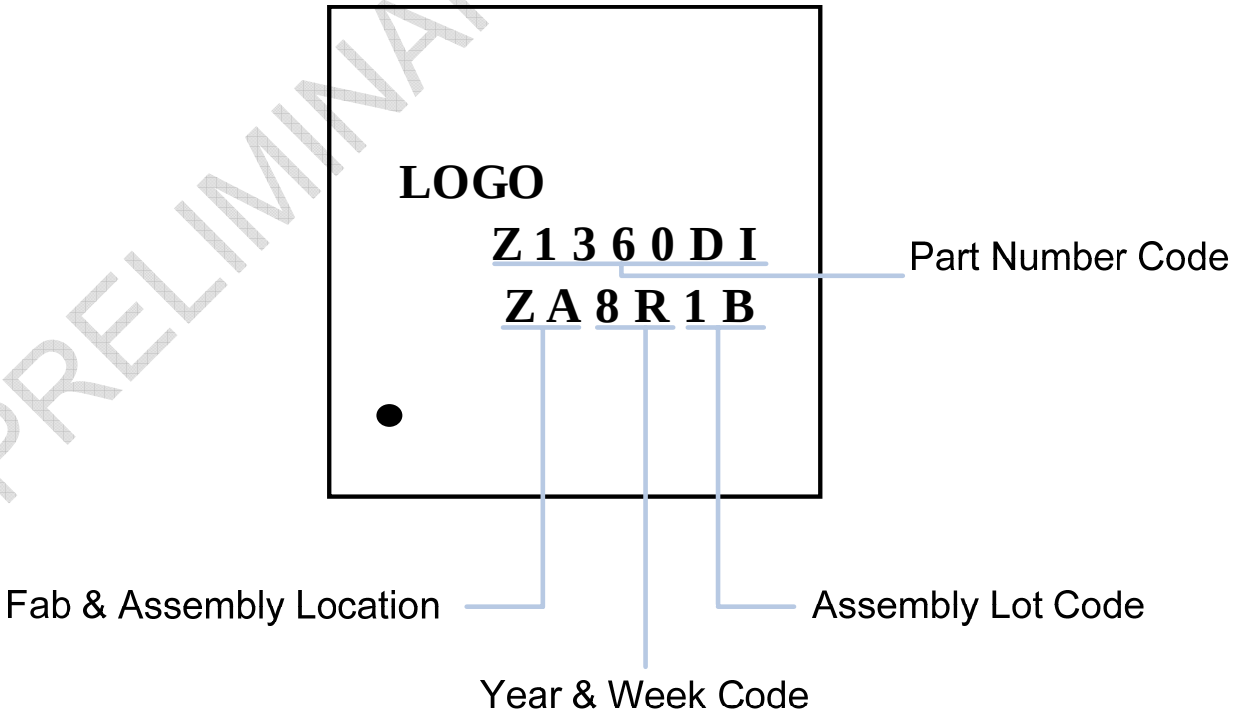


AOZ1360 Package Marking

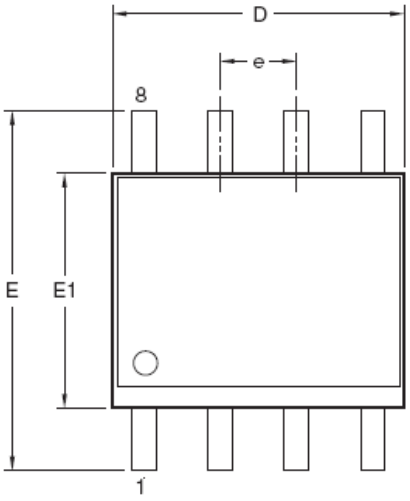
SO-8

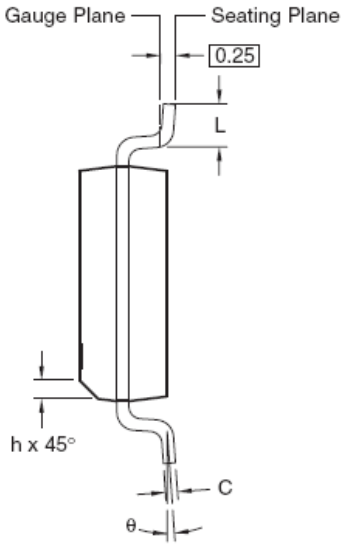


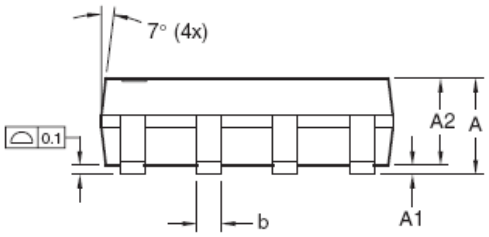
DFN4x4 10L

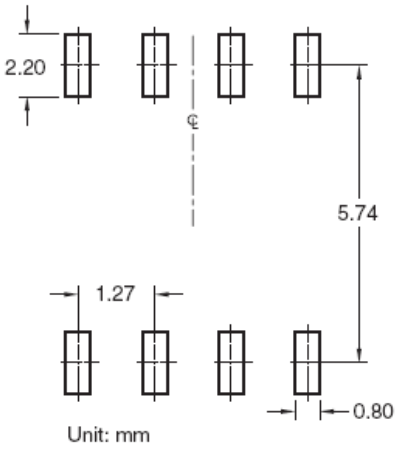


Package Dimensions, SO-8L









Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	1.35	1.65	1.75
A1	0.10	—	0.25
A2	1.25	1.50	1.65
b	0.31	—	0.51
c	0.17	—	0.25
D	4.80	4.90	5.00
E1	3.80	3.90	4.00
e	1.27 BSC		
E	5.80	6.00	6.20
h	0.25	—	0.50
L	0.40	—	1.27
θ	0°	—	8°

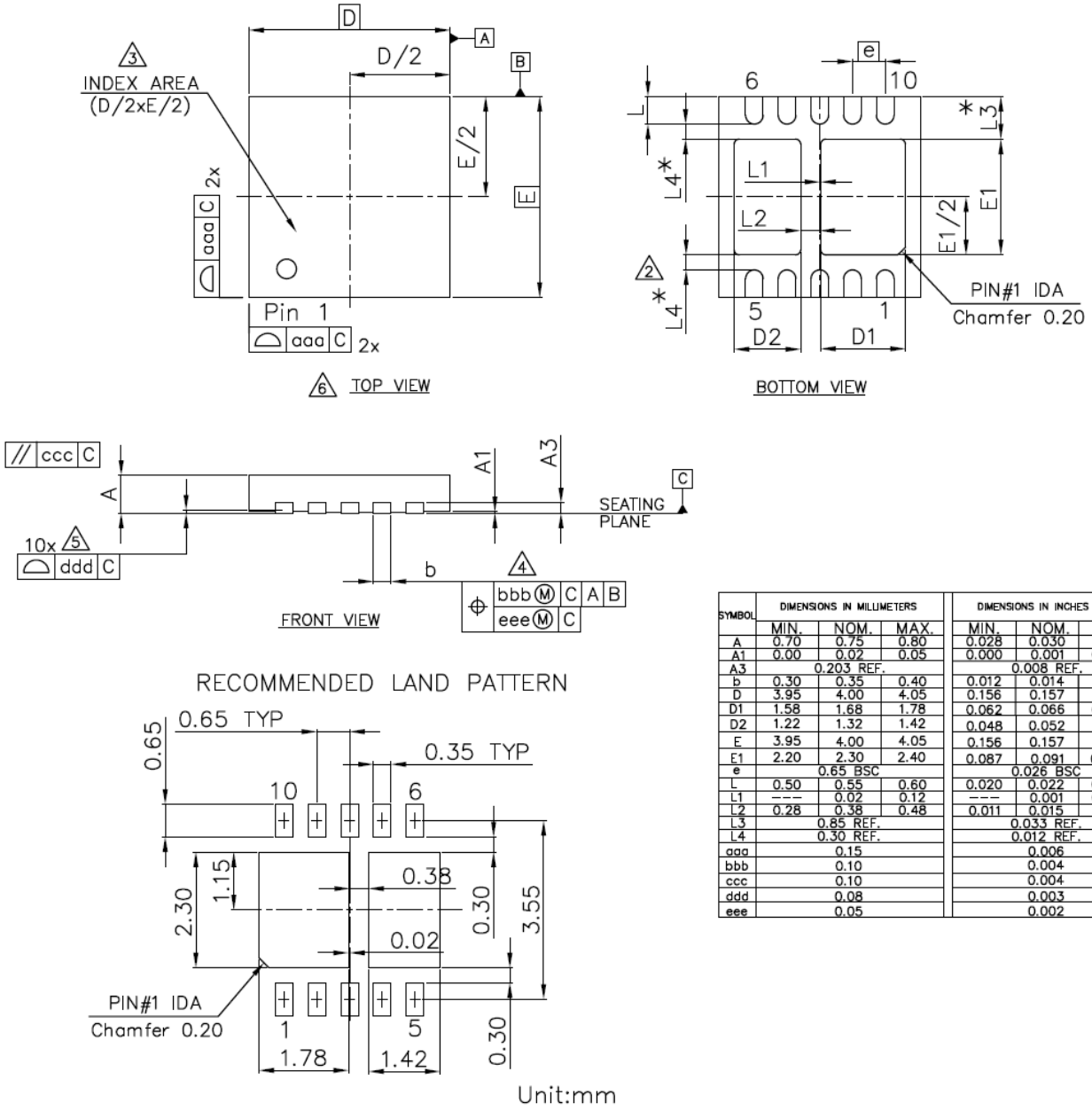
Dimensions in inches

Symbols	Min.	Nom.	Max.
A	0.053	0.065	0.069
A1	0.004	—	0.010
A2	0.049	0.059	0.065
b	0.012	—	0.020
c	0.007	—	0.010
D	0.189	0.193	0.197
E1	0.150	0.154	0.157
e	0.050 BSC		
E	0.228	0.236	0.244
h	0.010	—	0.020
L	0.016	—	0.050
θ	0°	—	8°

Notes:

1. All dimensions are in millimeters.
2. Dimensions are inclusive of plating
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 6 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

Package Dimensions, DFN4X4



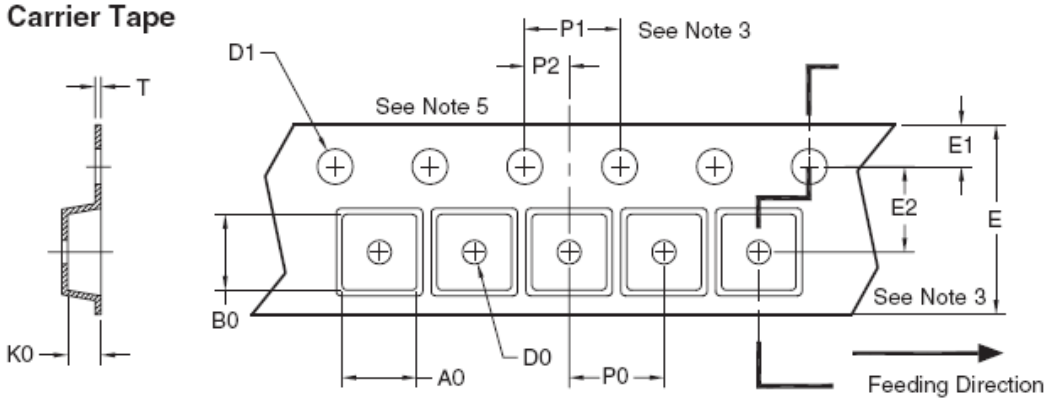
SYMBOL	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3		0.203 REF.			0.008 REF.	
b	0.30	0.35	0.40	0.012	0.014	0.016
D	3.95	4.00	4.05	0.156	0.157	0.159
D1	1.58	1.68	1.78	0.062	0.066	0.070
D2	1.22	1.32	1.42	0.048	0.052	0.056
E	3.95	4.00	4.05	0.156	0.157	0.159
E1	2.20	2.30	2.40	0.087	0.091	0.094
e		0.65 BSC			0.026 BSC	
L	0.50	0.55	0.60	0.020	0.022	0.024
L1	---	0.02	0.12	---	0.001	0.005
L2	0.28	0.38	0.48	0.011	0.015	0.019
L3		0.85 REF.			0.033 REF.	
L4		0.30 REF.			0.012 REF.	
aaa		0.15			0.006	
bbb		0.10			0.004	
ccc		0.10			0.004	
ddd		0.08			0.003	
eee		0.05			0.002	

Note:

1. All dimensions are in millimeters.
2. The dimensions with * are just for reference.
3. The location of the terminal #1 identifier and terminal numbering convention conforms to JEDEC publication 95 SPP-002.
4. Dimension b appliers to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured in that radius area.
5. Coplanarity applies to the terminals and all other bottom surface metallization.
6. Drawing shown are for illustration only.

Tape and Reel Dimensions

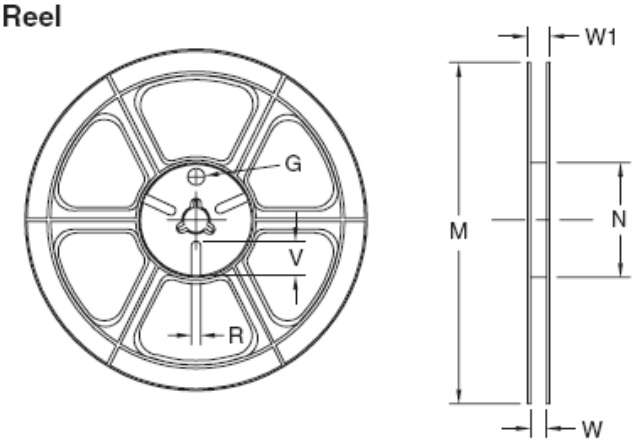
SO-8 Carrier Tape



Unit: mm

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
SO-8 (12mm)	6.40 ±0.10	5.20 ±0.10	2.10 ±0.10	1.60 ±0.10	1.50 ±0.10	12.00 ±0.10	1.75 ±0.10	5.50 ±0.10	8.00 ±0.10	4.00 ±0.10	2.00 ±0.10	0.25 ±0.10

SO-8 Reel



Tape Size	Reel Size	M	N	W	W1	H	K	S	G	R	V
12mm	ø330	ø330.00 ±0.50	ø97.00 ±0.10	13.00 ±0.30	17.40 ±1.00	ø13.00 +0.50/-0.20	10.60	2.00 ±0.50	—	—	—

SO-8 Tape

Leader/Trailer & Orientation