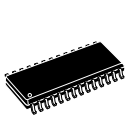
# L9733

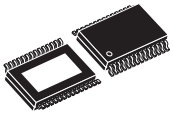
## Octal self configuring low/high side driver

## Features

- Eight independently self configuring low/high drivers
- Supply voltage from 4.5V to 5.5V
- $R_{ON(max)}$=0.7Ω @ $T_j$ = 25°C, $R_{ON(max)}$=1.2Ω @$T_j$ = 125°C
- Minimum current limit of each output 1A
- Output voltage clamping min. 40V in low side configuration
- Output voltage clamping max. -14V in high side configuration
- SPI interface for outputs control and for diagnosis data communication
- Additional PWM inputs for 3 outputs
- Independent thermal shutdown for all outputs Open load, Short to GND, short to Vb, Overcurrent diagnostics in latched or unlatched mode for each channel
- Internal charge pump without need of external capacitor
- Controlled SR for reduced EMC



**SO-28**



**PowerSSO-28**

## Description

The L9733 IC is a highly flexible monolithic, medium current, output driver that incorporates 8 outputs that can be used as either internal low or high side drives in any combination.

Outputs 1-8 are self-configuring as high or low side drives. Self-configuration allows a user to connect a high or low side load to any of these outputs and the L9733 will drive them correctly as well as provide proper fault mode operation with no other needed inputs. In addition, Outputs 6, 7 and 8 can be PWM controlled via a external pins (IN6-8).

This device is capable of switching variable load currents over the ambient range of -40°C to +125°C. The outputs are MOSFET drivers to minimize Vdd current requirements. For low side configured outputs an internal zener clamp from the drain to gate with a breakdown of 50V minimum will provide fast turn off of inductive loads. When a high side configured output is commanded OFF after having been commanded ON, the source voltage will go to (VGND - 15V).

An 16 bit SPI input is used to command the 8 output drivers either "On" or "Off", reducing the I/O port requirement of the microcontroller. Multiple L9733 can be daisy-chained. In addition the SPI output indicates latched fault conditions that may have occurred.

**Table 1. Device summary**

| Order code | Package | Packing |
|---|---|---|
| L9733 | SO-28 | Tube |
| L9733XP | PowerSSO-28 (Exposed pad) | Tube |

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# 1 Pin description

**Figure 1. Pin connection (top view)**

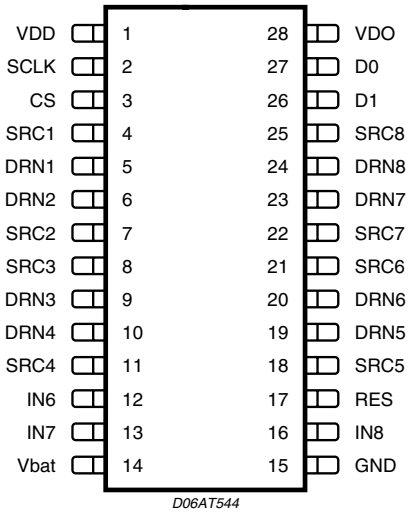



**Table 2. Pin description**

| N° | Pin | Function |
|---|---|---|
| 1 | VDD | 5 Volt supply input |
| 2 | SCLK | SPI serial clock input |
| 3 | CS | SPI chip select (active low) |
| 4 | SRC1 | Source pin of configurable driver #1 (0.7 Ω $Rds_{on}$ @+25°) |
| 5 | DRN1 | Drain pin of configurable driver #1(0.7 Ω $Rds_{on}$ @+25°) |
| 6 | DRN2 | Drain pin of configurable driver #2 (0.7 Ω $Rds_{on}$ @+25°) |
| 7 | SRC2 | Source pin of configurable driver #2 (0.7 Ω $Rds_{on}$ @+25°) |
| 8 | SRC3 | Source pin of configurable driver #3 (0.7 Ω $Rds_{on}$ @+25°) |
| 9 | DRN3 | Drain pin of configurable driver #3 (0.7 Ω $Rds_{on}$ @+25°) |
| 10 | DRN4 | Drain pin of configurable driver #4 (0.7 Ω $Rds_{on}$ @+25°) |
| 11 | SRC4 | Source pin of configurable driver #4 (0.7 Ω $Rds_{on}$ @+25°) |
| 12 | IN6 | Discrete input used to PWM output driver #6 |
| 13 | IN7 | Discrete input used to PWM output driver #7 |
| 14 | Vbat | Battery supply voltage |
| 15 | GND | Analog ground |
| 16 | IN8 | Discrete input used to PWM output driver #8 |
| 17 | RES | Reset input (active low) |
| 18 | SRC5 | Source pin of configurable driver #5 (0.7 Ω $Rds_{on}$ @+25°) |

**Table 2. Pin description (continued)**

| N° | Pin | Function |
|---|---|---|
| 19 | DRN5 | Drain pin of configurable driver #5 (0.7 Ω $Rds_{on}$ @+25°) |
| 20 | DRN6 | Drain pin of configurable driver #6 (0.7 Ω $Rds_{on}$ @+25°) |
| 21 | SRC6 | Source pin of configurable driver #6 (0.7 Ω $Rds_{on}$ @+25°) |
| 22 | SRC7 | Source pin of configurable driver #7 (0.7 Ω $Rds_{on}$ @+25°) |
| 23 | DRN7 | Drain pin of low side driver #7 (0.7 Ω $Rds_{on}$ @+25°) |
| 24 | DRN8 | Drain pin of low side driver #8 (0.7 Ω $Rds_{on}$ @+25°) |
| 25 | SRC8 | Source pin of configurable driver #8 (0.7 Ω $Rds_{on}$ @+25°) |
| 26 | DI | SPI data in |
| 27 | DO | SPI data out |
| 28 | VDO | Microcontroller logic interface voltage |

# 2 Operating conditions

## 2.1 Maximum ratings

This part may not operate if taken outside the maximum ratings. Once the condition is returned to within the specified maximum rating or the power is recycled, the part will recover with no damage or degradation.

**Table 3. Maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{dd}$ | Supply voltage | 4.5 to 5.5 | V |
| $V_{bat}$ | Battery supply voltage | 4.5 to 18 | V |
| $T_j$ | Thermal junction temperature range | -40 to 150 | °C |
| | Snubbing voltage of DRN1-8 | min 50 | VDC |
| $I_O$ | Output current 1-8 | max 800 | mA |

## 2.2 Absolute maximum ratings

This part may be irreparably damaged if taken outside the specified Absolute Maximum Ratings. Operation outside the Absolute Maximum Ratings may also cause a decrease in reliability.

**Table 4. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply voltage | -0.3 to 7 | V |
| $V_{bat}$ | Supply voltage | -0.3 to 40 | V |
| | CS,DI,DO,SCLK,EN,IN6,IN7,IN8,VDO | -0.3 to 7.0 | V |
| | SRC 1-8 | -24 to 40 | VDC |
| | DRN1-8 | -0.3 to 60 | VDC |
| $I_{OL}$ | Current limit of output 1-8 (-40°C) | 2.5 | A |
| $I_{OP}$ | Over current protection at output 1-8 (-40°C) | 3 | A |
| | Maximum clamping energy | 20 | mj |
| ESD | Human Body Model - All pins | ±2 (1) | kV |
| | Human Body Model - Driver outputs | ±4 (1) | kV |

1. Device is only protected vs. GND.

## 2.3 Thermal data

**Table 5. Thermal data**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{amb}$ | Operating ambient temperature | -40 | | 125 | °C |
| $T_{stg}$ | Storage temperature | -50 | | 150 | °C |
| $T_j$ | Maximum operating junction temperature | | | 150 | °C |
| $R_{th}$ | Thermal shut-down temperature | 151 | 175 | 200 | °C |
| $R_{th\text{-}hys}$ | Thermal shut-down temperature hysteresis | 7 | 10 | 25 | °C |
| $R_{Th\ j\text{-}amb}$ | Thermal resistance junction to ambient for SO28 (1)<br>for PowerSSO28 (2) | | | 55<br>24 | °C/W<br>°C/W |
| $R_{Th\ j\text{-}case}$ | Thermal resistance junction to case (PowerSSO28) | | | 3 | °C/W |
| $R_{Th\ j\text{-}pins}$ | Thermal resistance junction to pins (SO28) | | | 20 | °C/W |

1. With 6cm$^2$ on board heat sink area.
2. With 2s2p PCB thermally enhanced.

# 3 Electrical performance characteristics

These are the electrical capabilities this part was designed to meet. It is required that every part meet these characteristics.

## 3.1 DC characteristics:

$T_{amb}$ = -40 to 125°C, $V_{dd}$ = 4.5 to 5.5 Vdc, $V_{bat}$ = 4.5 to 18Vdc (high side configuration), unless otherwise specified.

**Table 6. DC characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $IN6v_{ih}$ | IN6 input voltage | | | | 0.7vdo | V |
| $IN6v_{il}$ | | | 0.3vdo | | | V |
| $I_{IN6il}$ | IN6 input current | In6 = 0 VDC | | | \|10\| | µA |
| $I_{IN6ih}$ | | In6 = VDO | 10 | | 100 | µA |
| $IN7v_{ih}$ | IN7 input voltage | | | | 0.7vdo | V |
| IN7vil | | | 0.3vdo | | | V |
| $I_{IN7il}$ | IN7 input current | In7 = 0 VDC | | | \|10\| | µA |
| $I_{IN7ih}$ | | In7 = VDO | 10 | | 100 | µA |
| $IN8v_{ih}$ | IN8 input voltage | | | | 0.7vdo | V |
| $IN8v_{il}$ | | | 0.3vdo | | | V |
| $I_{IN8il}$ | IN8 input current | In8 = 0 VDC | | | \|10\| | µA |
| $I_{IN8ih}$ | | In8 = VDO | 10 | | 100 | µA |
| $CS_{ih}$ | CS input voltage | | | | 0.7vdo | V |
| $CS_{il}$ | | | 0.3vdo | | | V |
| $I_{CSih}$ | CS input current | CS = VDO | | | \|10\| | µA |
| $I_{CSil}$ | | CS = 0 VDC | 10 | | 100 | µA |
| $SCLK_{ih}$ | SCLK input voltage | | | | 0.7vdo | V |
| $SCLK_{il}$ | | | 0.3vdo | | | V |
| $I_{SCLKih}$ | SCLK input current | SCLK = VDO | | | \|10\| | µA |
| $I_{SCLKil}$ | | SCLK = 0 VDC | 10 | | 100 | µA |
| $DI_{ih}$ | DI input voltage | | | | 0.7vdo | V |
| $DI_{il}$ | | | 0.3vdo | | | V |
| $I_{DIih}$ | DI input current | DI = VDO | | | \|10\| | µA |
| $I_{DIil}$ | | DI = 0 VDC | 10 | | 100 | µA |
| $DO_{ol}$ | DO output voltages | $I_{DO}$ = 2.5 mA | | | 0.4 | V |
| $DO_{oh}$ | | $I_{DO}$ = -2.5 mA | vdo-0.6 | | | V |

**Table 6. DC characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{DOzol}$ | DO Tri-state currents | DO = 0 VDC | | | \|10\| | µA |
| $I_{DOzoh}$ | | DO = VDO | | | \|10\| | µA |
| $RES_{ih}$ | RES input voltage | | | | 0.7vdo | V |
| $RES_{il}$ | | | 0.3vdo | | | V |
| $I_{RESil}$ | RES input current | RES = 0 VDC | 10 | | 100 | µA |
| $I_{RESih}$ | | RES = VDO | | | \|10\| | µA |
| $I_{slp}$ | Vbat sleep current | VDD = SRC1-8 = 0VDC<br>DRN1-DRN8=18VDC, Vb. Sum currents ($T_{amb}$ > 0°C)<br>($T_{amb}$ @ -40°C) | | | <br>10<br>3 | <br>µA<br>µA |
| $I_{vbat}$ | Vbat current | VDD=5V<br>All Outputs Commanded On | | | 15 | mA |
| $I_{VDD}$ | Max. VDD current | All Outputs Commanded On | | | 8.5 | mA |
| $I_{VDD}$ | Min. VDD current | All Outputs Commanded Off | 0.5 | | | mA |
| $I_{DRN1lk}$ - $I_{DRN8lk}$ | DRN1 - DRN8<br>Leakage currents<br>(Low side) | VDD = 0 VDC: SRC1-8 = 0 VDC<br>DRN1- DRN8 = 16 VDC<br>DRN1- DRN8 = 40 VDC | | | <br>5<br>10 | <br>µA<br>µA |
| $I_{SRC1lk}$ - $I_{SRC8lk.}$ | SRC1 – SRC8<br>Leakage currents<br>(High side) | VDD = 0 VDC: SRC1-8 = 0 VDC<br>DRN1- 8 = 16 V<br>DRN1- 8 = 40 VDC | | | <br>-5<br>-10 | <br>µA<br>µA |
| $I_{Drn1-8sink}$ | DRN1 – DRN8 Sink current<br>(Low side) | SRC1-8 = GND DI = AC00h<br>$R_{load} \leq 11K\Omega$<br>$R_{load} \leq 200K\Omega$ | <br>10<br>120 | | <br>100<br>280 | <br>µA<br>µA |
| $R_{DRN1-8}$ | Open load detection resistance | VBAT>=9V | 11 | | 200 | KΩ |
| $I_{Drn1-8source}$ | Source current | DRN1-DRN8 = GND | -10 | | -100 | µA |
| $I_{src1-8sink}$ | SRC1 – SRC8<br>Sink/source current<br>(High side) | DRN1- 8 = Vb, DI = AC00h<br>SCR1- 8 = Vb | <br>10 | | <br>100 | <br>µA |
| $I_{src1-8source}$ | | SCR1- 8 = GND | -18 | | -100 | µA |
| $V_{Drn1-8open}$ | DRN1 – DRN8<br>Open load voltage<br>(Low side) | SRC1- 8 = GND, DI = AC00h<br>DRN1- DRN8 = Open<br>VDD=4.9 to 5.1 VDC | 2.7 | | 3.1 | V |
| | | SRC1- 8 = GND, DI = AC00h<br>DRN1- DRN8 = Open<br>VDD = 4.5 to 5.5V | 2.5 | | 3.5 | V |
| $V_{src1-8open}$ | SRC1 – SRC8 open load voltage (High side)<br>DRN1 - DRN8 | DRN1-8 = Vb, DI = AC00h<br>SCR1-8 = open | 2.0 | | 2.8 | V |

**Table 6. DC characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{DRN1limit}$ - $I_{DRN8limit}$ | DRN1 - DRN8 Current limits (Low side) | DI = ACFFh, DI = AAFFh<br>SRC1 – SRC8 = 0 VDC<br>DRN1 - DRN8 = 4.5 - 16 VDC<br>($T_{amb}$ > 0°C)<br>($T_{amb}$ @ -40°C) | <br><br><br>1<br>1 | | <br><br><br>2.2<br>2.5 | <br><br><br>A<br>A |
| $I_{DRN1OVC}$- $I_{DRN8OVC}$ | DRN1 - DRN8 Overcurrent threshold (Low side) | DI = AC00h, DI = AA00h SRC1 – SRC8 = 0 VDC<br>DRN1 - DRN8 = 4.5 - 16 VDC<br>($T_{amb}$ > 0°C)<br>($T_{amb}$ - 40°C) | <br><br>1<br>1 | | <br><br>2.7<br>3 | <br><br>A<br>A |
| $I_{SRC1limit}$- $I_{SRC8limit}$ | SRC1 – SRC8 Current limits (High side) | DI = ACFFh, DI = AAFFh<br>DRN1 - DRN8 = Vb<br>SRC1 – SRC8 = GND<br>($T_{amb}$ > 0°C)<br>($T_{amb}$ - 40°C) | <br><br><br>1<br>1 | | <br><br><br>2.2<br>2.5 | <br><br><br>A<br>A |
| $I_{SRC1OVC}$- $I_{SRC8OVC}$ | Overcurrent threshold (High side) | DRN1 - DRN8 = Vbat<br>SRC1 – SRC8 = GND<br>($T_{amb}$ > 0°C)<br>($T_{amb}$ - 40°C) | <br><br>1<br>1 | | <br><br>2.7<br>3 | <br><br>A<br>A |
| $DRN1_{Cl+}$ - $DRN8_{Cl}$+ | DRN1 - DRN8 Clamp voltages (Low side) | DI = AC00h<br>SRC1-8 = GND, $I_{DRN1-8}$ = 350 mA | 50 | | 60 | V |
| $SRC1_{Cl+}$- $SRC8_{Cl}$+ | SRC1 – SRC8 Clamp voltages (High side) | DI = AC00h<br>DRN1-8 = Vbat, $I_{SRC1-8}$ = -350 mA | -24 | | -14 | V |
| $V_{Drn1-8open}$ - $DRN1-8_{VthGND}$ | Short to GND threshold distance from open load voltage (Low side) | SRC1 – SRC8 = GND:<br>Decrease Drn1 - Drn8 until Faults are ”Set” | 0.3 | | 0.7 | V |
| $DRN1-8_{VthVbat}$- $V_{Drn1-8open}$ | DRN1 - DRN8 Short to Vbat threshold distance from open load voltage (Low side) | DI = AC00h<br>SRC1 – SRC8 = GND: Increase Drn1 - Drn8 until Faults are ”Not Set” | 0.3 | | 0.7 | V |
| $V_{Drn1-8open}$ - $SRC1-8_{VthGND}$ | SRC1 - SRC8 Short to GND threshold distance from open load voltage (High side) | DI = AC00h<br>Drn1 – Drn8 = Vb: Decrease SRC1 - SRC8 until Faults are ”Not Set” | 0.2 | | 0.6 | V |
| $SRC1-8_{VthVbat}$- $V_{Drn1-8open}$ | SRC1 – SRC8 Short to Vbat threshold distance from open load voltage (High side) | DI = AC00h<br>Drn1 – Drn8 = Vbat: Increase SCR1 - SCR8 until Faults are ” Set” | 0.2 | | 0.6 | V |
| $Rdson_{Drn1-8}$ | On resistance (Drn to SRC1-8) | @ +125°C @ $I_{DRN}$ = 350mA | | | 1.2 | Ω |
| | | @ +25o C @ IDRN = 350mA | | | 0.7 | Ω |
| | | @ -40°C @ $I_{DRN}$ = 350mA | | | 0.5 | Ω |

**Table 6. DC characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $Drn1\text{-}8_{ther}$ (1) | Thermal shutdown temperature | DI = ACFFh, $I_{Drn1\text{-}8}$ = 1 mA, SRC1 – SRC8 = GND, Increase temperature until Drn1 - Drn8 > 2 VDC, Verify DO Bits 0-15 are "Set" | 151 | | 200 | °C |
| $Drn1\text{-}8_{hyst}$ (1) | Hysteresis | Drn1 - Drn8 < 2 VDC | 5 | | 15 | °C |

1. Design Information, not tested.

## 3.2 AC characteristics:

$T_{amb}$= -40 to 125°C, $V_{dd}$ = 4.5 to 5.5 Vdc, $V_{bat}$ = 4.5 to 18Vdc, unless otherwise specified

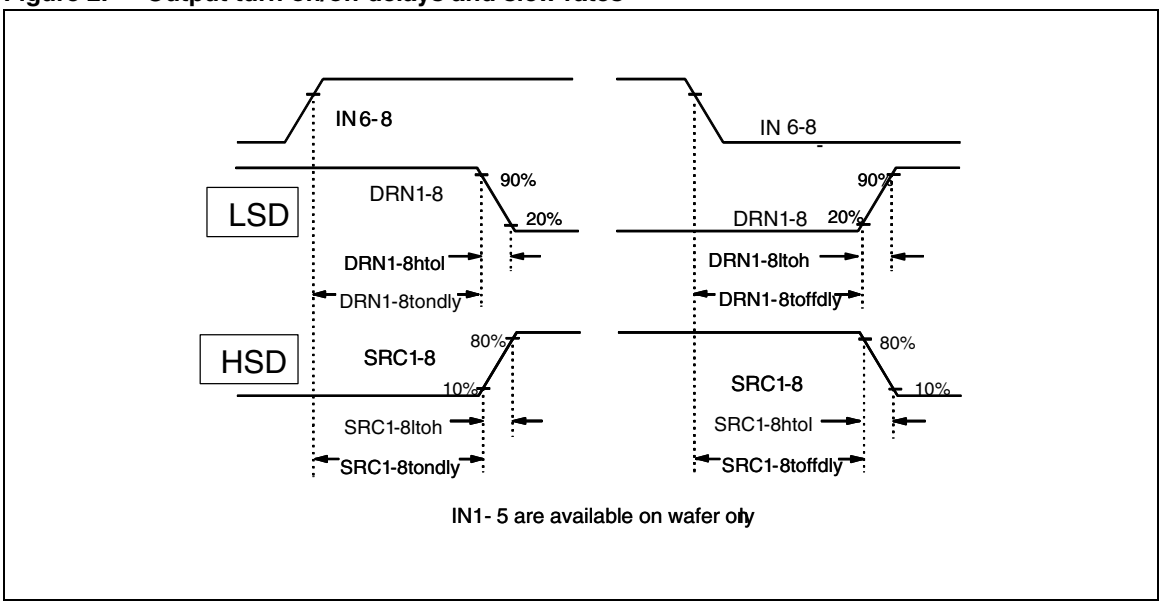
**Table 7. AC characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_{filtDRN1\text{-}8}$ | DRN1 - DRN8 Open load & short to GND filter time (Low Side) (Latch mode) | DI = AC00h, DI = A3FFh SRC1 – SRC8 = GND | 300 | | 900 | µs |
| $T_{filtSRC1\text{-}8}$ | SRC1 - SRC8 Open load & short to Vbat filter time (High side) (Latch mode) | DI = AC00h, DI = A3FFh DRN1 – DRN8 = Vb | 300 | | 900 | µs |
| $T_{delDRN1\text{-}8}$ | DRN1 - DRN8 Overcurrent switch off delay (Low side) | DI = ACFFh, DI = AA00h SRC1 – SRC8 = GND | 10 | | 75 | µs |
| $T_{delSRC1\text{-}8}$ | SRC1 - SRC8 Overcurrent switch off delay (High side) | DI = ACFFh, DI = AA00h DRN1 – DRN8 = Vb | 10 | | 75 | µs |
| $T_{res}$ | Restart time after overcurrent switch off time (Int) | DI = ACFFh, DI = AA00h | 120 | | 450 | ms |
| $Drn1\text{-}8_{htol}$ | Slew rate turn on | Outputs loaded as *Figure 4* See *Figure 2* | 0.65 | | 1.95 | V/µs |
| $Drn1\text{-}8_{ltoh}$ | Turn off (Low side) | See *Figure 2* | 0.5 | | 1.5 | V/µs |
| $SRC1\text{-}8_{htol}$ | Slew rate turn on | Outputs loaded as *Figure 4* See *Figure 2* | 0.65 | | 1.95 | V/µs |
| $SRC1\text{-}8_{ltoh}$ | Turn off (High side) | See *Figure 2* | 0.5 | | 1.5 | V/µs |

**Table 7. AC characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $Drn1\text{-}8_{tondly}$ | Delay time Turn on | Outputs loaded as *Figure 4* See *Figure 2* | 2 | | 20 | µs |
| $Drn1\text{-}8_{toffdly}$ | Turn off (Low side) | See *Figure 2* | 10 | | 100 | µs |
| $SRC1\text{-}8_{tondly}$ | Delay time Turn on | Outputs loaded as *Figure 4* See *Figure 2* | 2 | | 20 | µs |
| $SRC1\text{-}8_{toffdly}$ | Turn off (High side) | See *Figure 2* | 10 | | 100 | µs |
| $Drn1\text{-}8_{offon}$ | Delay delta | $Drn1\text{-}8_{toffdly}$ - $Drn1\text{-}8_{tondly}$ | 10 | | 60 | µs |
| $SRC1\text{-}8_{offon}$ | Delay delta | $SRC1\text{-}8_{toffdly}$ - $SRC1\text{-}8_{tondly}$ | 10 | | 60 | µs |

**Figure 2. Output turn on/off delays and slew rates**



## 3.3 SPI characteristics and timings

$T_{amb}$= -40 to 125°C, $V_{dd}$ = 4.5 to 5.5 Vdc, $V_{bat}$ = 4.5 to 18Vdc, unless otherwise specified

**Table 8. SPI characteristics and timings**

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $DINC_{in}$ | Input capacitance | | | | 20 | pF |
| $SCLK_{Cin}$ | | | | | 20 | pF |
| $DO_{rise}$ | Output data (do) rise time | 50 pF from DO to Ground See *Figure 5* | | | 70 | ns |
| $DO_{fall}$ | Output data (do) fall time | See *Figure 5* | Figure 5 | | 70 | ns |
| $DO_a$ | Access time | See *Figure 6* | | | 350 | ns |
| $DO_{sum}$ | Set up time | See *Figure 6* | 20 | | | ns |
| $DO_{hm}$ | Hold time | See *Figure 6* | 10 | | | ns |
| $DO_{dis}$ | Output data (DO) disable time | No Capacitor on DO, See *Figure 5* | | | 400 | ns |
| $tth_{Filt}$ | Filter time | All Fault bits are “Set” | 5 | | 20 | µs |
| SCLKwid | SCLK width | See *Figure 5*, @ $f_{SCLK}$ = 5.4MHz(1) | 185 | | | ns |
| SCLKlm | SCLK low time | See *Figure 5*, @ $f_{SCLK}$ = 5.4MHz(1) | 58 | | | ns |
| SCLKhm | SCLK high time | See *Figure 5*, @ $f_{SCLK}$ = 5.4MHz(1) | 58 | | | ns |
| SCLKrise | SCLK rise time | See *Figure 5*, @ $f_{SCLK}$ = 5.4MHz(1) | | | 21 | ns |
| SCLKfall | SCLK fall time | See *Figure 5*, @ $f_{SCLK}$ = 5.4MHz(1) | | | 21 | ns |
| CSrise | Channel select (CS) rise time | See *Figure 5* (1) | | | 100 | ns |
| CSfall | Channel select (CS) fall time | See *Figure 5* (1) | | | 100 | ns |
| CSlead | Channel select (CS) lead time | See *Figure 6* (1) | 455 | | | ns |
| CSlag | Channel select (CS) lag time | See *Figure 6* (1) | 50 | | | ns |
| DIrise | Input data (DI) rise time | See *Figure 5*, @ $f_{SCLK}$ = 5.4MHz(1) | | | 30 | ns |
| DIfall | Input data (DI) fall time | See *Figure 5* @ $f_{SCLK}$ = 5.4MHz(1) | | | 30 | ns |
| DIsus | Input data (DI) set-up time | See *Figure 6*, @ $f_{SCLK}$ = 5.4MHz(1) | 15 | | | ns |
| DIhs | Input data (DI) hold time | See *Figure 6*, @ $f_{SCLK}$ = 5.4MHz(1) | 10 | | | ns |

1. Guaranteed by design.

**Figure 3. DO loading for disable time measurement**

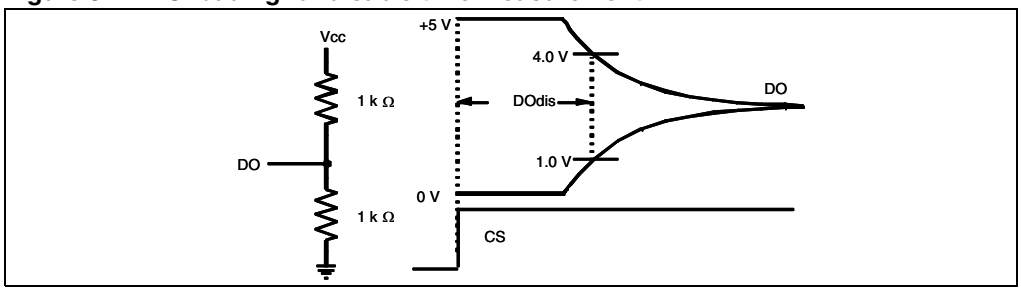



**Figure 4. Output loading for slew rate measurements**

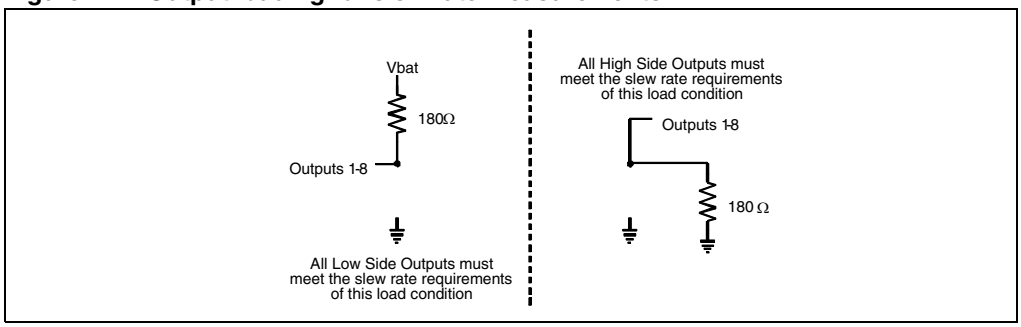



**Figure 5. SPI input/output timings**

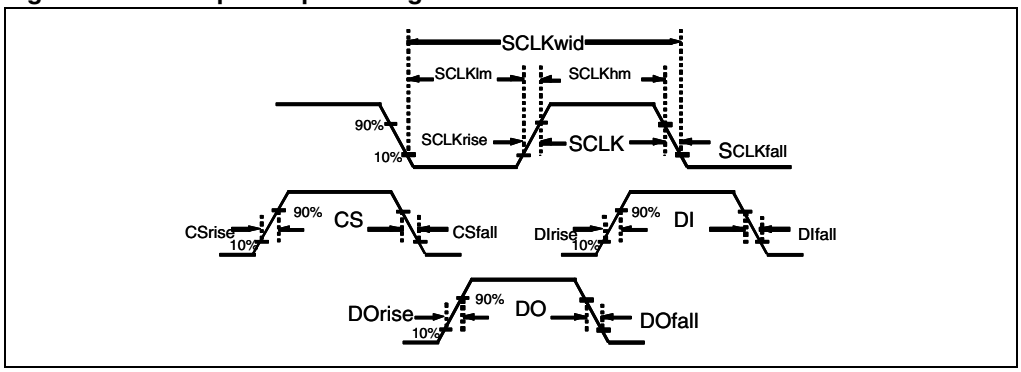
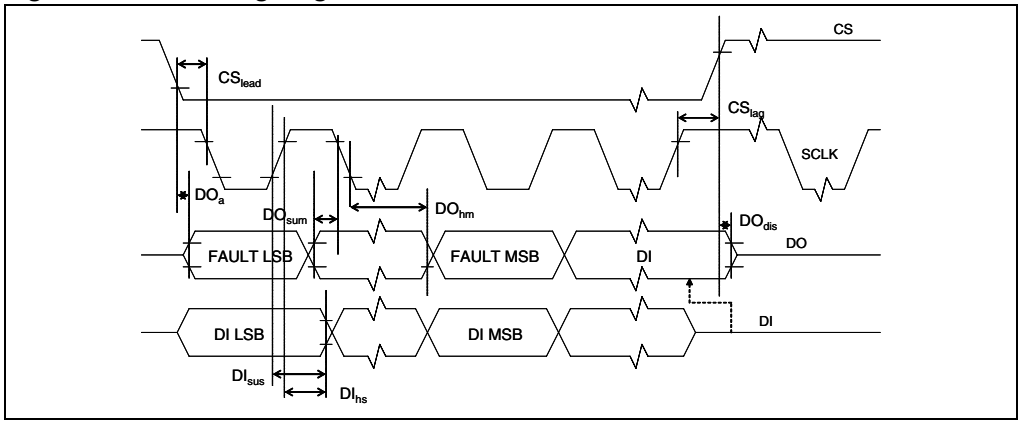



**Figure 6. SPI timing diagram**



# 4 Functional description

L9733 integrates 8 self-configuring outputs (OUT1-8) which are able to drive either incandescent lamps, inductive loads (non-pwm'd, in pwm is necessary an external diode to reduce flyback power dissipation), or resistive loads biased to Vbat (low side configuration) or to GND (high side configuration). These outputs can be enabled and disabled via the SPI bus. Each of these outputs has a short circuit protection (with 0.8-2.4 Amps threshold) selectable via SPI bus between a filtered switching OFF overcurrent protection or a linear current limitation (default condition after power ON is switching OFF protection enabled).

An over-temperature protection as described in *Section 2.1* is available for each outputs. When a high side configured output is commanded OFF after having been commanded ON, the source voltage will go to (VGND - 15V). This is due to the design of the circuitry and the transconductance of the MOSFET. When a low side configured output is commanded OFF after having been commanded ON, the output voltage will rise to the internal zener clamp voltage (50 VDC minimum) due to the flyback of the inductive load.

Outputs 1-8 are able to drive any combination of inductive loads or lamps at one time. Inductive loads for the L9733 can range from 35mH to a maximum of 325mH. The recommended worst-case solenoid loads (at -40°C) are calculated using a minimum resistance of 40Ω for each output. The maximum single pulse inductive load energy the L9733 outputs is able to be safely handle is 20mJ at -40°C to 125°C (Worst-case load of 325mH & 40Ω).

## 4.1 Configurations for outputs 1-8

The drain and source pins for each Output must be connected in one of the two following configurations (see *Figure 7*).

### 4.1.1 Low side drivers

When any combination of Outputs 1-8 are connected in a low side drive configuration the source of the applicable Output (Src1-8) shall be connected to ground. The drain of the applicable Output (Drn1-8) shall be connected to the low side of the load.

### 4.1.2 High side drivers

When any combination of Outputs 1-8 are connected in a high side drive configuration the Drain of the applicable Output (Drn1-8) shall be connected to Vbat. The source of the applicable Output (Src1-8) shall be connected to the high side of the load.

## 4.2 Outputs 1-5

These five outputs can be used as either high or low side drives. The room temperature Rdson of these outputs is 0.7Ω. A current limited (100µA max) voltage generator is connected to Src 1-5 for open load and short to GND detection when a low side configured output is commanded OFF. Another current limited (100µA max if VDrn 1-5 > 60%Vbat, 280µA max if VDrn 1-5 < 60%Vbat) voltage generator is connected to Drn 1-5 for open load and short to Vbat detection when a high side configured output is commanded OFF.
Drain pins of Outputs 1-5 (Drn1-5) are connected to the drains of the N channel MOSFET

transistors. Source pins of Outputs 1-5 (Src1-5) are connected to the sources of the N channel MOSFET transistors.

## 4.3 Outputs 6-8

These three self-configuring outputs can be used to drive either high or low side loads. In addition to being controlled by the SPI BUS these outputs can also be enabled and disabled via the IN6 & IN7& IN8 inputs. The IN6, IN7 and IN8 inputs are logically or'd with the SPI commands to allow either the IN6 & IN7 & IN8 inputs or the SPI commands to activate these outputs. The use of the IN6 & IN7 & IN8 pins for PWM control on these outputs should only be done with non-inductive loads if an external flyback diode is not present. The room temperature Rdson of these four outputs is 0.7Ω. A current limited (100µA max) voltage generator is connected to Src 6-8 for open load and short to GND detection when a low side configured output is commanded OFF. Another current limited (100µA max if VDrn 6-8 > 60%Vbat, 280µA max if VDrn 6-8 < 60%Vbat) voltage generator is connected to Drn 6-8 for open load and short to Vbat detection when a high side configured output is commanded OFF.
Drain pins of Outputs 6-8 (Drn6-8) are connected to the drains of the N channel MOSFET transistors. Source pins of Outputs 6-8 (Src6-8) are connected to the sources of the N channel MOSFET transistors.

## 4.4 Drn1-8 susceptibility to negative voltage transients

All outputs connected in the low side configuration must have a ceramic chip capacitor of 0.01µF to 0.1µF connected from drain to ground. This is needed to prevent potential problems with the device operation due to the presence of fast negative transient(s) on the drain(s) of the device. Adequate de-coupling capacitors from the Drain (VBAT) to ground shall be provided for high side configured outputs.

## 4.5 Supply pins

### 4.5.1 Main power input (Vdd)

An external +5.0 ±0.5 VDC supply provided from an external source is the primary power source to the L9733. This supply is used as the power source for all of its internal logic circuitry and other miscellaneous functions.

### 4.5.2 Battery supply (Vbat)

This input is the supply for the on board charge pump. This input shall be connected directly to battery. If this input is not connected to the same supply, without additional voltage drops, of the drains of any high side connected outputs, then the Rdson of that given output will be higher than the specified maximum.

### 4.5.3 Discrete inputs voltage supply (VDO)

This pin is used to supply the discrete input stages of L9733 and must be connected to the same voltage used to supply the peripherals of the processor interfaced to L9733.

## 4.6 Discrete inputs

### 4.6.1 Output 6-8 enable input (In6, In7, In8)

This input allows Output 6 (or Output 7, or Output 8) to be enabled via this external pin without the use of the SPI. The SPI command and the In6-7 input are logically or'd together. A logic "1" on this input (In6, In7 or In8) will enable this output no matter what the status of the SPI command register. A logic "0" on this input will disable this output if the SPI command register is not commanding this output on. This pins (In6, In7 or In8) can be left "open" if the internal output device is being controlled only via the SPI. This input has a nominal 100kΩ resistor connected from this pin to ground, which will pull this pin to ground if an open circuit condition occur. This input is ideally suited for non-inductive loads that are pulse width modulated (PWM'd). This allows PWM control without the use of the SPI inputs.

### 4.6.2 Reset input (RES)

When this input goes low it resets all the internal registers and switches off all the output stages. This input has a nominal 100 kΩ resistor connected from this pin to VDD, which will pull this pin to VDD if an open circuit condition occur.

# 5 Serial peripheral interface (SPI)

The L9733 has a serial peripheral interface consisting of Serial Clock (SCLK), Data Out (DO), Data In (DI), and Chip Select (CS). All outputs will be controlled via the SPI. The input pins CS, SCLK, and DI, thanks to VDO pin, have level input voltages allowing proper operation from microcontrollers that are using 5.0 or 3.3 volts for their Vdd supply. The design of the L9733 allows a "daisy-chaining" of multiple L9733's to further reduce the need for controller pins.

## 5.1 Serial data output (DO)

This output pin is in a tri-state condition when CS is a logic '1'. When CS is a logic '0', this pin transmits 16 bits of data from the fault register to the digital controller. After the first 16 bits of DO fault data are transmitted (after a CS transition from a logic '1' to a logic '0'), then the DO output sequentially transmits the digital data that was just received (16 SCLK cycles earlier) on the DI pin. The DO output continues to transmit the 16 SCLK delayed bit data from the DI input until CS eventually transitions from a logic '0' to a logic '1'. DO data changes state 10 nsec or later, after the falling edge of SCLK. The LSB is the first bit of the byte transmitted on DO and the MSB is the last bit of the byte transmitted on DO, once CS transitions from a logic '1' to a logic '0'.

## 5.2 Serial data input (DI)

This input takes data from the digital controller while CS is low. The L9733 accepts an 16 bit byte to command the outputs on or off. The L9733 also serially wraps around the DI input bits to the DO output after the DO output transmits its 16 fault flag bits. The LSB is the first bit of each byte received on DI and the MSB is the last bit of each byte received on DI, once CS transitions from a logic '1' to a logic '0'. The last 4 bits (b15-b12) of the first 16 bit byte are used as key-word. The 4 bits (b11-b8) of the first 16 bits byte are used to select writing mode between OUT8-1 status and diagnosis operating mode . The DI input has a nominal 100 kΩ resistor connected from this pin to the VDO pin, which pulls this pin to VDO if an open circuit condition occurs.

## 5.3 Chip select (CS)

This is the chip select input pin. On the falling edge of CS, the DO pin is released from tri-state mode. While CS is low, register data are shifted in and shifted out the DI pin and DO pin, respectively, on each subsequent SCLK. On the rising edge of CS, the DO pin is tri-stated and the fault register is "Cleared" if a valid DI byte has been received. A valid DI byte is defined as such:

- a multiple of 16 bits was received.
- a valid key-word was received

The fault data is not cleared unless all of the 2 previous conditions have been met. The CS input has a nominal 100kΩ resistor connected from this pin to the VDO pin, which pulls this pin to VDO if an open circuit condition occurs.

## 5.4 Serial clock (SCLK)

This is the clock signal input for synchronization of serial data transfer. DI data is shifted into the DI input on the rising edge of SCLK and DO data changes on the falling edge of SCLK. The SCLK input has a nominal 100kΩ resistor connected from this pin to the VDO pin, which pulls this pin to VDO if an open circuit condition occurs.

## 5.5 Initial input command register & fault register SPI cycle

After initial application of Vdd to the L9733, the input command register and the fault register are "Cleared" by the POR circuitry and that means that the default condition for the output status is Off, the default diagnostic mode is No Latch and the switching OFF overcurrent protection is enable. During the initial SPI cycle, and all subsequent cycles, valid fault data will be clocked out of DO (fault bits).

## 5.6 Input command register

An input byte (16 bits) is routed to the Command Register. The content of this Command Register is given in table 9. Additional DI data will continue to be wrapped around to the DO pin. If CS should happen to go high before complete reception of the current byte, this just transmitted byte shall be ignored (invalid).

**Table 9. Bit command register definition**

| Key word | | | | Writing mode: output | | | | Output status | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **MSB** | | | | | | | | | | | | | | | **LSB** |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | OUT 8 | OUT 7 | OUT 6 | OUT 5 | OUT 4 | OUT 3 | OUT 2 | OUT 1 |
| b15 | b14 | b13 | b12 | b11 | b10 | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |

| Key word | | | | Writing mode: diag | | | | Driver diag mode | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **MSB** | | | | | | | | | | | | | | | **LSB** |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | Diag 8 | Diag 7 | Diag 6 | Diag 5 | Diag 4 | Diag 3 | Diag 2 | Diag 1 |
| b15 | b14 | b13 | b12 | b11 | b10 | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |

| Key word | | | | Writing mode: protect | | | | Driver overcurrent protection | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **MSB** | | | | | | | | | | | | | | | **LSB** |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | Ilim 8 | Ilim 7 | Ilim 6 | Ilim 5 | Ilim 4 | Ilim 3 | Ilim 2 | Ilim 1 |
| b15 | b14 | b13 | b12 | b11 | b10 | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |

**Table 10. Command register logic definition**

| Bit | State | Status | Writing mode |
|---|---|---|---|
| b0-b7 | 0 | OUT1 - OUT8 are Commanded Off | Output |
| b0-b7 | 1 | OUT1 - OUT8 are Commanded On | Output |
| b0-b7 | 0 | OUT1 - OUT8 Diagnostic is No Latch Mode | Diag |
| b0-b7 | 1 | OUT1 - OUT8 Diagnostic is Latch Mode | Diag |
| b0-b7 | 0 | OUT1 - OUT8 Switching OFF Overcurrent Protection | Protection |
| b0-b7 | 1 | OUT1 - OUT8 Linear Overcurrent Protection | Protection |

# 6 Other L9733 features

## 6.1 Charge pump usage

In order to provide low Rdson values when connected in a high side configuration, a charge pump to drive the internal gate voltage(s) above Vbat is implemented. The charge pump used on the L9733 doesn't need external capacitor. The L9733 uses a common charge pump and oscillator for all the 8 configurable output channels. The charge pump uses the Vbat supply connected directly to the Vb pin. The normal range of the Vbat voltage is 10 to 18V18V. However, the L9733 is functional with Vbat voltages as low as 4.5V DC with eventually a degradation of Rdson.

The frequency range of this charge pump is from 3.6 to 7.6 MHz. The frequency is above 1.8MHz in order to be above the AM radio band and below 8.0MHz so that harmonics do not get within the FM radio band.

## 6.2 Waveshaping

Both the turn on and the turn off slew rates on all outputs (OUT1-8) are limited to between 10µs and 100µs for both rise and fall times (10 to 90%, and vice versa), to reduce conducted EMC energy in the vehicle's wiring harness. The characteristics of the turn-on and turn-off voltage is linear, with no discontinuities, during the output driver state transition.

## 6.3 POR register initialization

When the L9733 wakes up, the Vdd supply to the L9733 is allowed from 0 to 5 VDC in 0.3 to 3ms. The L9733 has a POR circuit, which monitors the Vdd voltage. When the Vdd voltage reaches an internal threshold, and remains above this trip level for at least 5 to 20µs, the Command and Fault registers are "cleared". Before Vdd reaches this trip level, none of the eight outputs are allowed to momentarily glitch on.

## 6.4 Thermal shutdown

Each of the eight outputs has independent thermal protection circuitry that disables each output driver once the local N-Channel MOSFET's device temperature reaches between +151 and +200°C. A filter is present to validate the thermal fault (5µs to 20µs). There is a 5 to 15°C hysteresis between the enable and disable temperature levels. The faulted channel will periodically turn off and on until the fault condition is cleared, the ambient temperature is decreased sufficiently or the output is commanded off. If a thermal shutdown, of one or more output drivers, is active during the falling edge of the chip select (CS) signal all the bits of the Fault Register are "setted" to "1" (thermal shutdown is not latched and could be read only in the moment it is present). The thermal fault is cleared on the rising edge of Chip Select if a valid DI byte was received.

*Note: Due to the design of the L9733 each output's thermal limit "may not" be truly independent to the extent that if one output is shorted, it may impact the operation of other outputs (due to lateral heating in the die).*

# 7 Fault operation

The fault diagnostic capability consists of one internal 16 bits shift register and 2 bits are used for each output. The diagnostic information are: no fault present, overcurrent, open load and short circuit.

All of the faults will be cleared on the rising edge of Chip Select if a valid DI byte was received

**Table 11. Fault register definition**

| OUT 8 | | OUT 7 | | OUT6 | | OUT5 | | OUT4 | | OUT3 | | OUT2 | | OUT1 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MSB | | | | | | | | | | | | | | | LSB |
| D1 | D0 | D1 | D0 | D1 | D0 | D1 | D0 | D1 | D0 | D1 | D0 | D1 | D0 | D1 | D0 |
| b15 | b14 | b13 | b12 | b11 | b10 | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |

**Table 12. Fault logic definition**

| D1 | D0 | Fault status |
|---|---|---|
| 0 | 0 | No fault is present |
| 0 | 1 | Open load |
| 1 | 0 | Short circuit to GND (low side) or Short circuit to Vbat (high side) |
| 1 | 1 | Overcurrent |

If all the bits b0-b15 of the fault register have value '1' it means that a thermal fault, at least on one of the eight independent Outputs, occurred.

## 7.1 Low side configured output fault operation

The diagnostic circuitry verifies for the low side configured output the following condition: Normal operation, open load, short circuit to GND and overcurrent (only if the switching OFF protection, selectable for each channel via SPI bus, is active).

The diagnostic circuitry operates in two different modes, selected for each channel by SPI: no latch mode and latch mode. The fault priority is overcurrent and then open load or short circuit to GND, this means that if an overcurrent occurs the fault register is always overwritten and following open load or short to GND faults that happen before that the register is cleared will be ignored.

### 7.1.1 No latch mode

This diagnostic operating mode doesn't latch open load and short to GND faults.

1. **Open load**
   The diagnostic of open load is detected only in OFF condition sensing the Drn1-8 output voltage. This fault is detected on the falling edge of the CS input if the power drain voltage is inside the voltage range limited by the two thresholds **Vth_Vbat** and

**Vth_GND**. An internal current limited voltage regulator fixes the drain voltage inside the described range when no load is connected.

2. **Short circuit to GND**
   The diagnostic of short circuit to GND is detected only in OFF condition sensing the Drn1-8 output voltage. This fault is detected on the falling edge of the CS input if the power drain voltage is lower than the **Vth_GND** threshold.
3. **Overcurrent**
   The diagnostic of overcurrent is detected only in ON condition, if the switching OFF protection of the channel is enabled (default), sensing the current level of the output power transistor. If the output current has been above the short threshold **Iovc** for the filtering time **Tdel** the output power is switched off and at the same time an overcurrent fault is written in the fault register.
   There are three possibilities to restart one output after the fault has occurred:
   - Automatically after a time **Tres**
   - On the rising edge of CS if two valid DI byte has been received and first the Output Status in the command register is written with logic '0' and then with a logic “1” in the following SPI cycle
   - On the rising edge (low to high transition) at the corresponding parallel input pin (only for Outputs 6-8).
   - If the switching OFF protection is not active the On phase overcurrent protection is a linear current limitation and no diagnosis is available.

The use of the IN6-8 pins for PWM control on the outputs 6-8 could generates bad diagnostic behavior when the falling edge of CS happens a short time after the falling edge of IN6-8 during the power MOS transient. Software filtering may be needed to ignore fault signals during Drn6-8 transient after falling edge of IN6-8.

### 7.1.2 Latch mode

This diagnostic operating mode latches all faults when they happen.

1. **Open load**
   The diagnostic of open load is detected only in OFF condition sensing the Drn1-8 output voltage. This fault is detected if the power drain voltage is inside the voltage range limited by the two thresholds Vth_Vbat and Vth_GND for the filtering time **Tfilt**. An internal current limited voltage regulator fixes the drain voltage inside the described range when no load is connected.
2. **Short circuit to GND**
   The diagnostic of short circuit to GND is detected only in OFF condition sensing the Drn1-8 output voltage. This fault is detected if the power drain voltage is lower than the Vth_GND threshold for the filtering time Tfilt.
3. **Overcurrent**
   The diagnostic of overcurrent is detected only in ON condition, if the switching OFF protection of the channel is enabled (default), sensing the current level of the output power transistor. If the output current has been above the short threshold Iovc for the filtering time Tdel the output power is switched off and at the same time an overcurrent fault is written in the fault register. If the switching OFF protection is not active the On

phase overcurrent protection is a linear current limitation and no diagnosis is available. There are three possibilities to restart one output after the fault has occurred:

– Automatically after a time **Tres**
– On the rising edge of CS if two valid DI byte has been received and first the Output Status in the command register is written with logic '0' and then with a logic “1” in the following SPI cycle
– On the rising edge (low to high transition) at the corresponding parallel input pin (only for Outputs 6-8).
If the power MOS transient, after a switching-off command, is longer than Tdel filtering time, a bad diagnostic behavior happens and software filtering may be needed.

## 7.2 High side configured output fault operation

The diagnostic circuitry verifies for the high side configured output the following condition: Normal operation, open load, short circuit to Vbat and overcurrent (only if the switching OFF protection, selectable for each channel via SPI bus, is active).

The diagnostic circuitry operates in two different modes, selected for each channel by SPI: no latch mode and latch mode. The fault priority is overcurrent and then open load or short circuit to Vb, this means that if an overcurrent occurs the fault register is always overwritten and following open load or short to Vbat faults that happen before that the register is cleared will be ignored.

### 7.2.1 No latch mode

This diagnostic operating mode doesn't latch open load and short to Vbat faults.

1. **Open load**
The diagnostic of open load is detected only in OFF condition sensing the Src1-8 output voltage. This fault is detected on the falling edge of the CS input if the power drain voltage is inside the voltage range limited by the two thresholds Vth_Vbat and Vth_GND. An internal current limited voltage regulator fixes the drain voltage inside the described range when no load is connected.
2. **Short Circuit to Vb**
The diagnostic of short circuit to Vbat is detected only in OFF condition sensing the Src1-8 output voltage. This fault is detected on the falling edge of the CS input if the power drain voltage is higher than the **Vth_Vbat** threshold.
3. **Overcurrent**
The diagnostic of overcurrent is detected only in ON condition, if the switching OFF protection of the channel is enabled (default), sensing the current level of the output power transistor. If the output current has been above the short threshold Iovc for the filtering time Tdel the output power is switched off and at the same time an overcurrent

fault is written in the fault register.
There are three possibilities to restart one output after the fault has occurred:

– Automatically after a time **Tres**
– On the rising edge of CS if two valid DI byte has been received and first the Output Status in the command register is written with logic '0' and then with a logic “1” in the following SPI cycle
– On the rising edge (low to high transition) at the corresponding parallel input pin (only for Outputs 6-8).
– If the switching OFF protection is not active the On phase overcurrent protection is a linear current limitation and no diagnosis is available.
The use of the IN6-8 pins for PWM control on the outputs 6-8 could generates bad diagnostic behavior when the falling edge of CS happens a short time after the falling edge of IN6-8 during the power MOS transient. Software filtering may be needed to ignore fault signals during Drn6-8 transient after falling edge of IN6-8.

### 7.2.2 Latch mode

This diagnostic operating mode latches all faults when they happen.

1. **Open load**
The diagnostic of open load is detected only in OFF condition sensing the Src1-8 output voltage. This fault is detected if the power drain voltage is inside the voltage range limited by the two thresholds **Vth_Vbat** and **Vth_GND** for the filtering time **Tfilt**. An internal current limited voltage regulator fixes the drain voltage inside the described range when no load is connected.
2. **Short Circuit to Vb**
The diagnostic of short circuit to Vbat is detected only in OFF condition sensing the Src1-8 output voltage. This fault is detected if the power drain voltage is higher than the **Vth_Vbat** threshold for the filtering time **Tfilt**.
3. **Overcurrent**
The diagnostic of overcurrent is detected only in ON condition, if the switching OFF protection of the channel is enabled (default), sensing the current level of the output power transistor. If the output current has been above the short threshold **Iovc** for the filtering time **Tdel** the output power is switched off and at the same time an overcurrent fault is written in the fault register.

There are three possibilities to restart one output after the fault has occurred:

– Automatically after a time **Tres**
– On the rising edge of CS if two valid DI byte has been received and first the Output Status in the command register is written with logic '0' and then with a logic “1” in the following SPI cycle
– On the rising edge (low to high transition) at the corresponding parallel input pin (only for Outputs 6-8).
If the switching OFF protection is not active the On phase overcurrent protection is a linear current limitation and no diagnosis is available.

If the power MOS transient, after a switching-off command, is longer than **Tdel** filtering time, a bad diagnostic behavior happens and software filtering may be needed.

**Figure 7. L9733 application schematic**

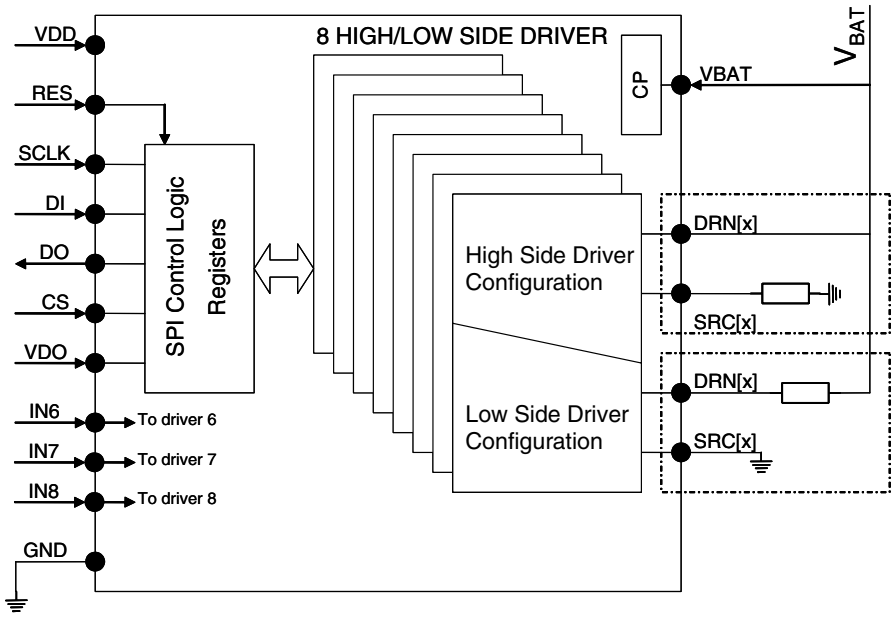
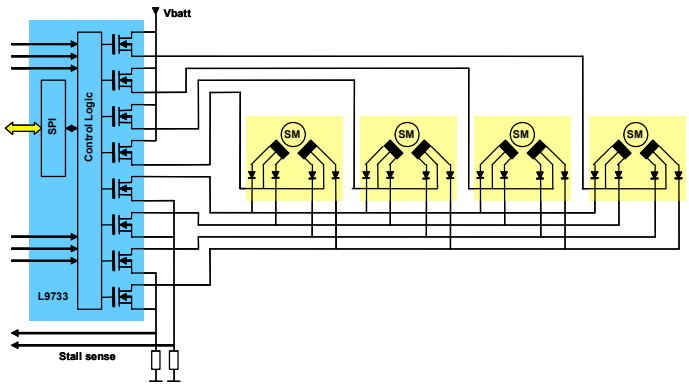
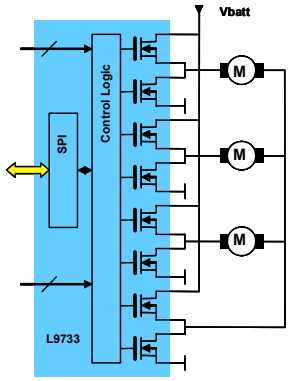



**Figure 8. L9733 HVAC applicative examples**

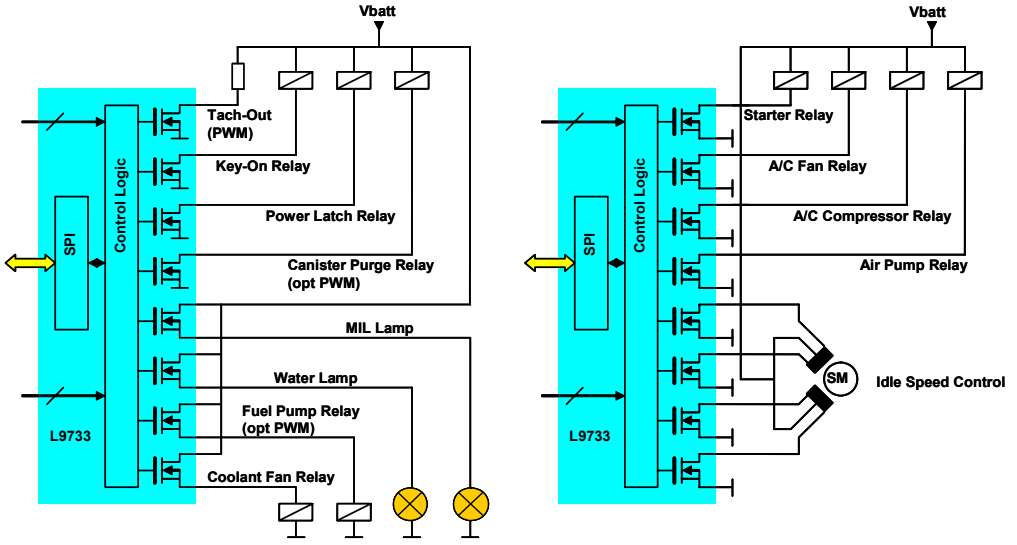



*Four flap motors become sequentially driven. Unipolar stepper motor are selected by 4 high-side configured switches. If the decoupling diodes are inside the motor housing, only 8 wires are needed to drive this arrangement.*




*4 channels configured to low- and 4 channels configured to high side build a quad half bridge. This allows to drive 3 DC-motors in sequential ly.*

**Figure 9. L9733 powertrain applicative examples**




*Main Relays and Lamps Driving*

*Idle speed stepper motor driving and auxiliary loads*

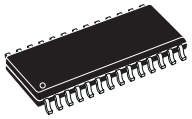
# 8 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

**Figure 10. SO28 mechanical data and package dimensions**

| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 2.65 | | | 0.104 |
| a1 | 0.1 | | 0.3 | 0.004 | | 0.012 |
| b | 0.35 | | 0.49 | 0.014 | | 0.019 |
| b1 | 0.23 | | 0.32 | 0.009 | | 0.013 |
| C | | 0.5 | | | 0.020 | |
| c1 | 45° (typ.) | | | | | |
| D | 17.7 | | 18.1 | 0.697 | | 0.713 |
| E | 10 | | 10.65 | 0.394 | | 0.419 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 16.51 | | | 0.65 | |
| F | 7.4 | | 7.6 | 0.291 | | 0.299 |
| L | 0.4 | | 1.27 | 0.016 | | 0.050 |
| S | 8 ° (max.) | | | | | |

**OUTLINE AND MECHANICAL DATA**



**SO-28**

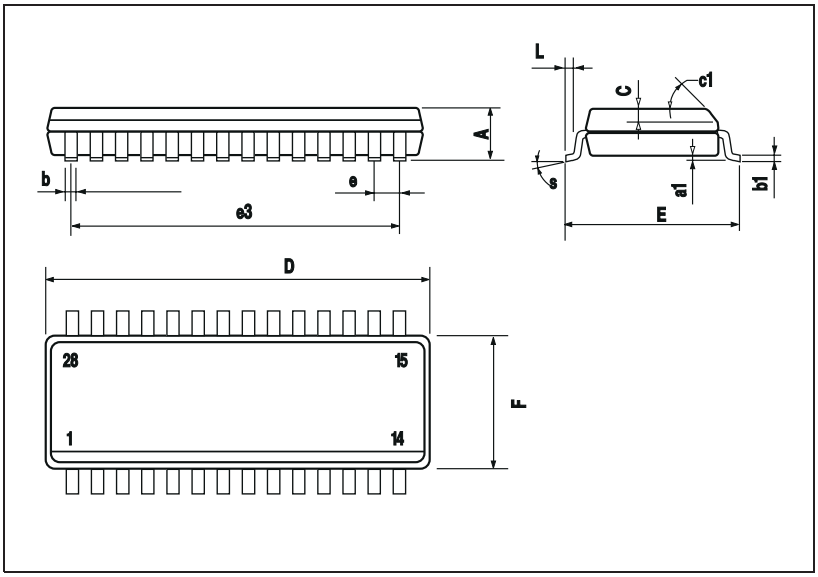
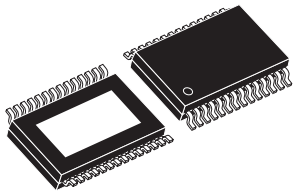


**Figure 11. PowerSSO28 mechanical data and package dimensions**

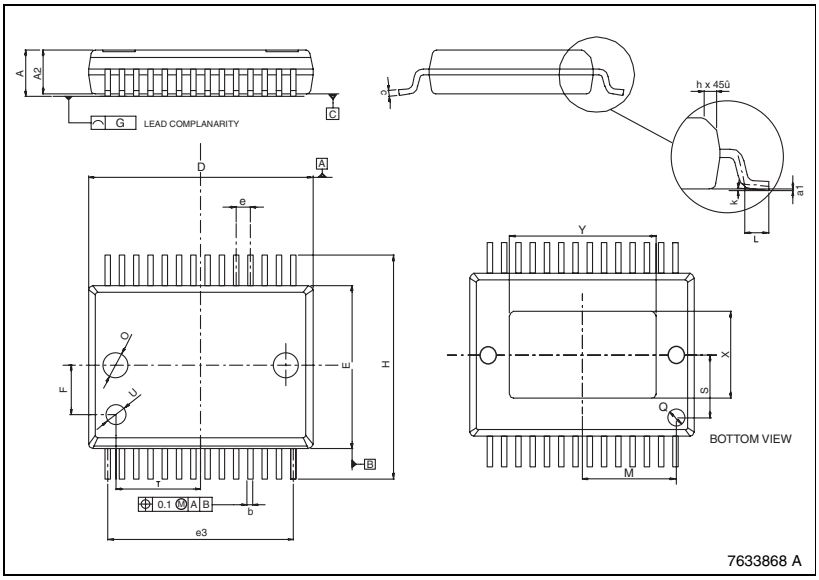
| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | 2.15 | | 2.47 | 0.084 | | 0.097 |
| A2 | 2.15 | | 2.40 | 0.084 | | 0.094 |
| a1 | 0 | | 0.075 | 0 | | 0.003 |
| b | 0.18 | | 0.36 | 0.007 | | 0.014 |
| c | 0.23 | | 0.32 | 0.009 | | 0.012 |
| D (1) | 10.10 | | 10.50 | 0.398 | | 0.413 |
| E (1) | 7.4 | | 7.6 | 0.291 | | 0.299 |
| e | | 0.65 | | | 0.025 | |
| e3 | | 8.45 | | | 0.033 | |
| F | | 2.3 | | | 0.090 | |
| G | | | 0.10 | | | 0.004 |
| G1 | | | 0.06 | | | 0.002 |
| H | 10.10 | | 10.50 | 0.398 | | 0.413 |
| h | | | 0.40 | | | 0.016 |
| k | | 5° | | | 5° | |
| L | 0.55 | | 0.85 | 0.022 | | 0.033 |
| M | | 4.3 | | | 0.169 | |
| N | | | 10° | | | 10° |
| O | | 1.2 | | | 0.047 | |
| Q | | 0.8 | | | 0.031 | |
| S | | 2.9 | | | 0.114 | |
| T | | 3.65 | | | 0.144 | |
| U | | 1.0 | | | 0.039 | |
| X | 4.2 | | 4.8 | 0.165 | | 0.190 |
| Y | 6.6 | | 7.2 | 0.260 | | 0.283 |

(1) "D" and "E" do not include mold flash or protrusions Mold flash or protrusions shall not exceed 0.15 mm per side(0.006")

**OUTLINE AND MECHANICAL DATA**



**PowerSSO-28 (exposed-pad)**



# 9 Revision history

**Table 13. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 13-Apr-2005 | 1 | Initial release. |
| 15-Jun-2006 | 2 | Changed only look and feel. |
| 08-Aug-2006 | 3 | Modified *Table 9: Bit command register definition on page 22*. |
| 28-May-2007 | 4 | Changed the min. value of the CSlead parameter on the *Table 8*. |
| 17-Jul-2007 | 5 | Updated *Table 6* and *Table 7*. Added new *Figure 4*.<br>Changed the status from Preliminary data to Datasheet. |
| 3-Aug-2007 | 6 | Updated in *Table 4* the ESD parameter. |

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