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P	N-Channel Enhancement-Mode
巴	N-Channel Enhancement-Mode Vertical DMOS Power FETs

## **Ordering Information**

	P	- Incom	Order Number / Package			
BV <sub>DSS</sub> / BV <sub>DGS</sub>	(max)	(min)	TO-39	TO-92	TO-220	
	6Ω	16	VN0216N2	VN0216N3	VN0216N5	
160V		1A	VN0220N2	VN0220N3	VN0220N5	
200V	6Ω			daaraa ahaa daaraa d		

### Features

- Freedom from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C<sub>ISS</sub> and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-Channel devices

### **Applications**

- Motor control
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

### **Absolute Maximum Ratings**

Drain-to-Source Voltage	BV <sub>DSS</sub>		
Drain-to-Gate Voltage	BV <sub>DGS</sub>		
Gate-to-Source Voltage	± 20V		
Operating and Storage Temperature	-55°C to +150°C		
Soldering Temperature*	300°C		

\*Distance of 1.6 mm from case for 10 seconds.

## Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicongate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermallyinduced secondary breakdown.

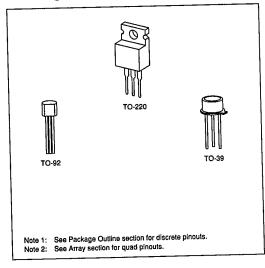
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Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

### **Package Options**

(Notes 1 and 2)



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#### VN02C

<b>Thermal C</b>	haracteristics
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Thermal Characteristics					7-39-05		
Package	I <sub>D</sub> (continuous)*	l <sub>p</sub> (pulsed)*	Power Dissipation @ T <sub>c</sub> = 25°C	θ <sub>ja</sub> ° <b>C/W</b> 125	θ <sub>lc</sub> °C/W 32	I <sub>DR</sub>	I <sub>DRM</sub> * 2.5А
TO-39	0.7A	2.5A	4W			0.7A	
TO-92	0.4A	2.5A	1W	170	125	0.5A	2.5A
TO-220	1.5A	2.5A	28W	70	4.6	1.7A	2.5A

\* Ip (continuous) is limited by max rated T

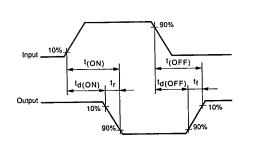
# Electrical Characteristics (@ 25°C unless otherwise specified)

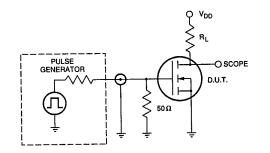
(Notes 1 and 2)

Symbol	Parameter		Min	Тур	Max	Unit	Conditions
BV <sub>DSS</sub>	Drain-to-Source	VN0216	160			v	V <sub>GS</sub> = 0, I <sub>D</sub> = 2.0mA
033	Breakdown Voltage	VN0220	200				
V <sub>GS(th)</sub>	Gate Threshold Voltage		0.75		3	V	$V_{GS} = V_{DS}, I_D = 2.0 \text{mA}$
ΔV <sub>GS(th)</sub>	Change in VGS(th) with Tempera	iture		-4.6	-5.5	mV/°C	$V_{gg} = V_{pg}, I_p = 1.0 \text{mA}$
IGSS	Gate Body Leakage				100	nA	$V_{GS} = \pm 20V, V_{DS} = 0$
I <sub>DSS</sub>	Zero Gate Voltage Drain Curren	nt			25	μA	V <sub>GS</sub> = 0, V <sub>DS</sub> = Max Rating
000					2.5	mA	$V_{GS} = 0$ , $V_{DS} = 0.8$ Max Rating
					ļ		T <sub>A</sub> = 125°C
I <sub>D(ON)</sub>	ON-State Drain Current		0.5	1.3		Α	$V_{GS} = 5V, V_{DS} = 25V$
·D(ON)			1.0	2.2	1	A	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 25V
R <sub>DS(ON)</sub>	Static Drain-to-Source			5.0	8		V <sub>GS</sub> = 5V, I <sub>D</sub> = 0.5A
· ·DS(ON)	ON-State Resistance			4.0	6	Ω	$V_{GS} = 10V, I_{D} = 0.5A$
ΔR <sub>DS(ON)</sub>	Change in R <sub>DS(ON)</sub> with Temper	rature		0.8	1.4	%/°C	V <sub>GS</sub> = 10V, I <sub>D</sub> = 500mA
G <sub>FS</sub>	Forward Transconductance		0.3	0.7		σ	$V_{DS} = 25V, I_{D} = 1A$
C <sub>ISS</sub>	Input Capacitance		1	75	150		$V_{GS} = 0, V_{DS} = 25V$
C <sub>oss</sub>	Common Source Output Capa			34	85	] pF	f = 1  MHz
C <sub>RSS</sub>	Reverse Transfer Capacitance	)	1	15	35	]	
t <sub>d(ON)</sub>	Turn-ON Delay Time				10		V <sub>DD</sub> = 25V
t,	Rise Time				10	ns	$V_{DD} = 25V$ $I_{D} = 0.5A$
t <sub>d(OFF)</sub>	Turn-OFF Delay Time				20	] 113	$R_{s} = 50\Omega$
t <sub>f</sub>	Fall Time				20		
V <sub>SD</sub>	Diode Forward Voltage Drop			1.2	1.8	V	$V_{GS} = 0, I_{SD} = 1A$
t <sub>rr</sub>	Reverse Recovery Time			430		ns	$V_{GS} = 0, I_{SD} = 1A$

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.) Note 2: All A.C. parameters sample tested.

### Switching Waveforms and Test Circuit





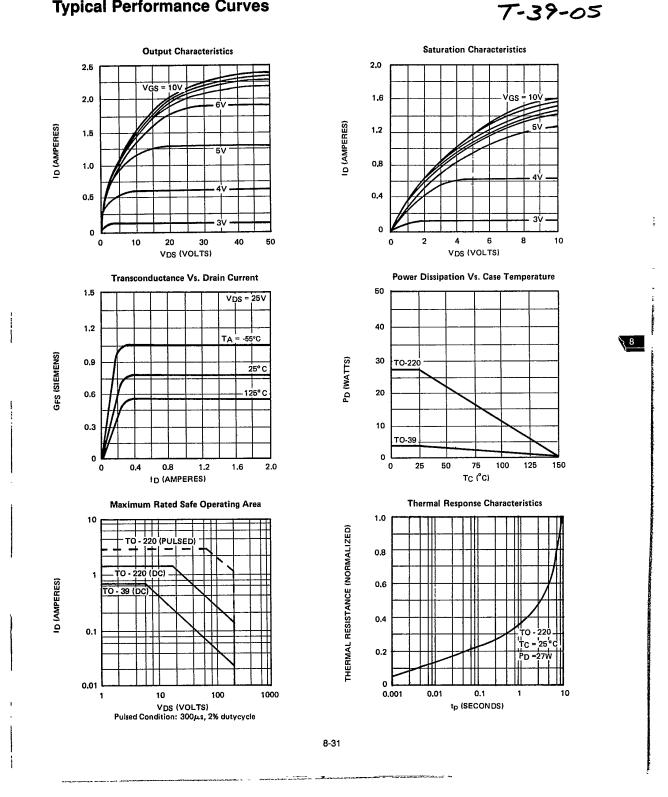
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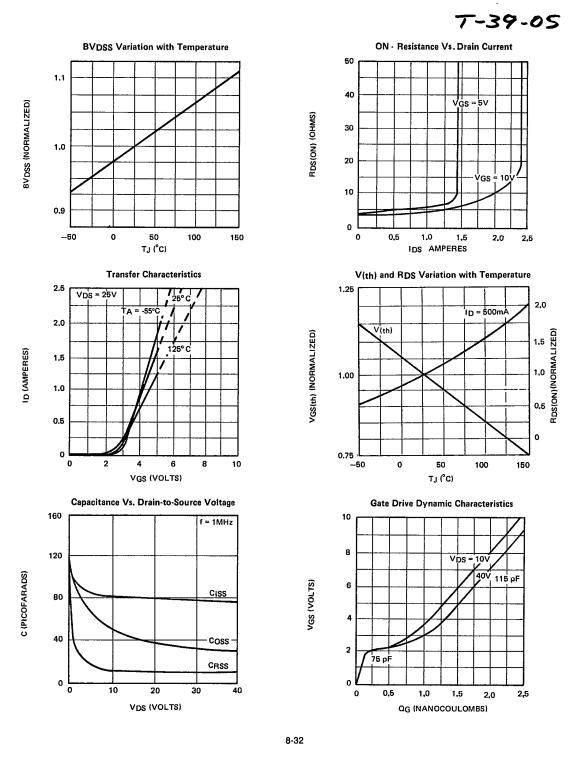
### **Typical Performance Curves**



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