R2J20751NP

Peak Current Mode Synchronous Buck Controller with Power MOS FETs

R07DS0240EJ0100
Rev.1.00
Jan 26, 2011

Description

This all-in-one SiP for POL (point-of-load) applications is a multi-chip module incorporating a high-side MOS FET, low-side MOS FET, and PWM controller in a single QFN package. The on and off timing of the power MOS FET is optimized by the built-in driver circuit, making this device suitable for large-current high-efficiency buck converters. In a simple peak-current mode topology, stable operation is obtained in a closed power loop, and a fast converter is easily realized with the addition of simple components. Furthermore, the same topology can be applied to realize converters for parallel synchronized operation with current sharing, and multi-phase operation. The package also incorporates a high-side bootstrap switch (Boot switch), eliminating the need for an external SBD for this purpose.

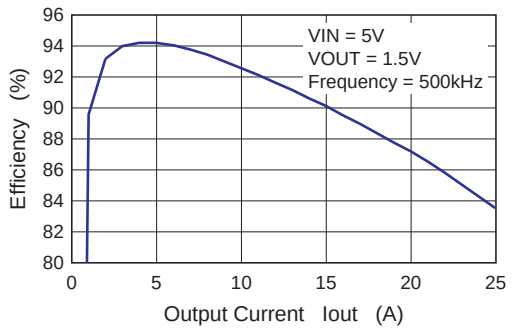
Features

- Three chip in one package for high efficiency and space saving
- Large average output current (25 A)
- Wide input voltage range: 3.3 V to 27 V
- 0.6 V reference voltage accurate to within 2%
- Wide programmable switching frequency: 200 kHz to 1 MHz
- Peak current mode topology with Active Current Sensing
- Slope compensation function
- Current sensing error: 1.5 A maximum @15 A load current
- Built-in Boot switch for boot strapping
- ON/OFF control
- Hiccup operation under over load condition
- Tracking function
- Thin and small package: QFN40 pins (6 mm × 6 mm)
- Power Good function
- Over voltage protection
- Pre-OVP function

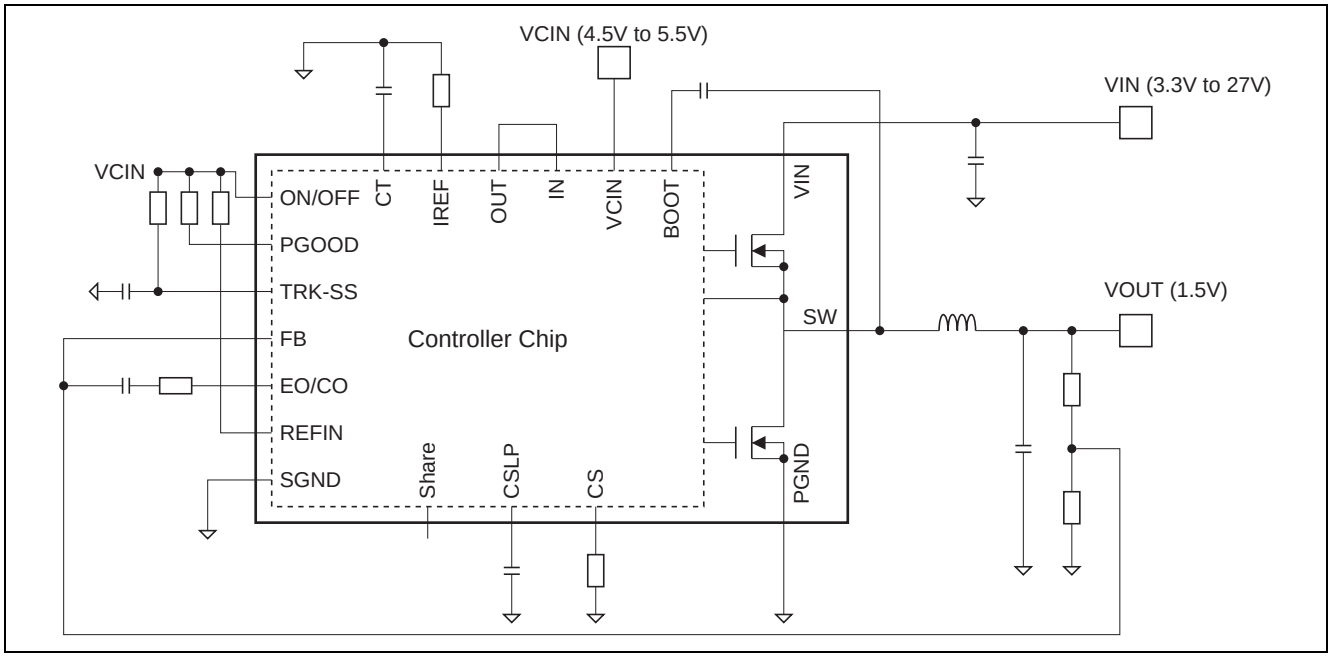
Applications

- Mother board
- Servers

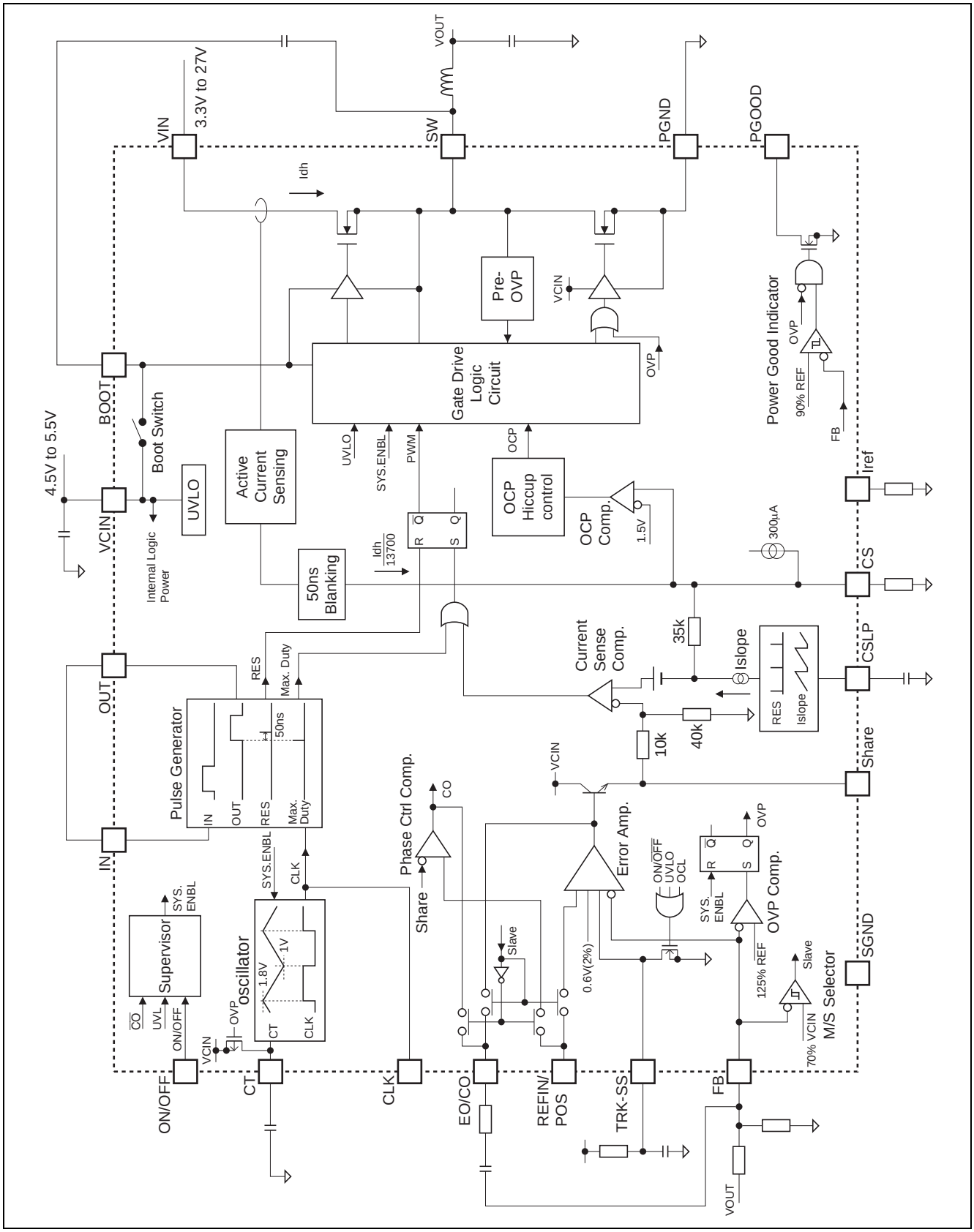
Typical Characteristic Curve



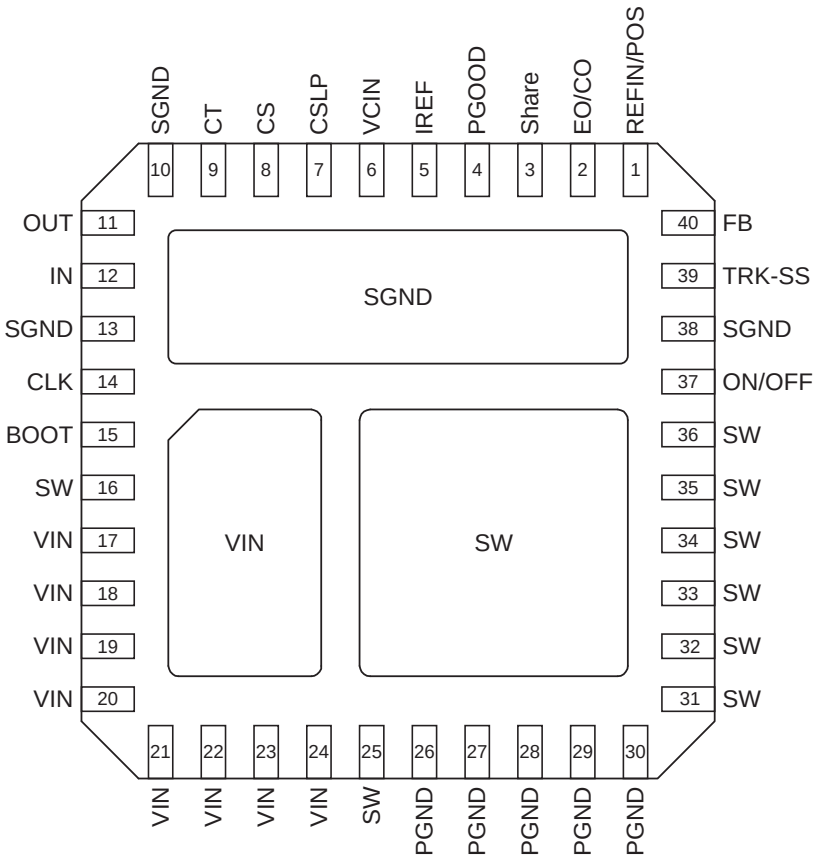
Application Circuit Example



Block Diagram



Pin Arrangement



Top view
Package: QFN40 pin (6 mm × 6 mm, 0.5-mm pin pitch)

Pin Description

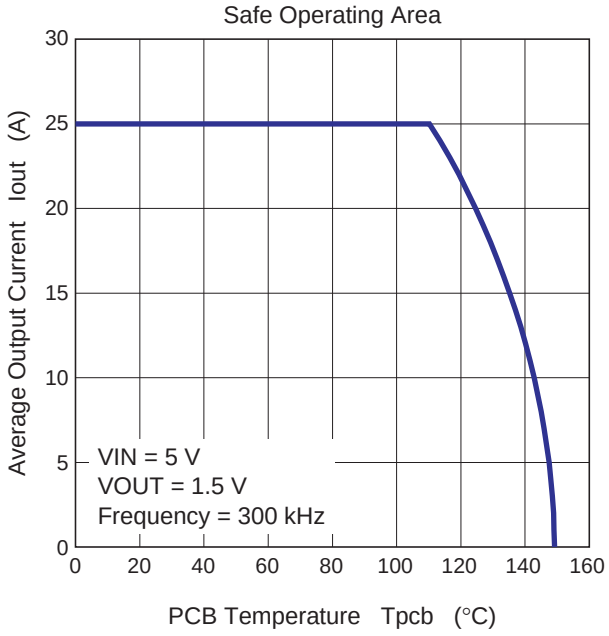
Pin Name	Pin No.	Description	Remarks
VIN	17 to 24	Input voltage for buck converter.	
SW	16, 25, 31 to 36	Switching node. Connect a choke coil between the SW pin and dc output node of the converter.	
PGND	26 to 30	Ground of the power stage.	Should be connected to SGND externally.
SGND	10, 13, 38	Ground of the IC chip.	Should be connected to PGND externally.
VCIN	6	Input voltage for control circuit.	Should be connected to 5 V power supply.
BOOT	15	Bootstrap voltage pin. A bootstrap capacitance should be connected between BOOT pin and SW pin.	To be supplied +5 V through the internal SBD.
TRK-SS	39	Start-up timing control input.	
FB	40	Feedback voltage input for the closed loop.	
EO/CO	2	Error amplifier output pin. (Master mode) Comparator output pin. (Slave mode)	
Share	3	Current share bus.	Should be connected to each Share pin in multi phase operation.
IREF	5	Reference current generator for the IC.	Need a 18 kΩ resistance between IREF to GND plane.
CSLP	7	Additional current slope input pin.	Should be connected capacitor between CSLP to GND.
CS	8	Current output pin of Active Current Sensing circuit.	Need a resistance appropriately between CS to GND plane.
CT	9	Timing capacitor pin for the oscillator.	
OUT	11	Switching trigger output.	Tie to IN pin of previous device in multi phase operation.
IN	12	Switching trigger input.	Tie to OUT pin of next device in multi phase operation.
CLK	14	I/O pin for synchronous operation.	Should be connect to each CLK pin in multiphase operation.
ON/OFF	37	Signal disable pin.	Disabled when ON/OFF pin is low state.
PGOOD	4	Power Good Indicator output. (Open drain)	Pulled low when No Good.
REFIN/POS	1	Reference voltage input. (Master mode) Comparator positive pin. (Slave mode)	

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Rating	Unit	Note
Power dissipation	Pt(25)	25	W	1
	Pt(100)	8		
Average output current	Iout	25	A	
Input voltage	VIN(DC)	–0.3 to +27	V	2
	VIN(AC)	30		2, 5
Supply voltage	VCIN(DC)	–0.3 to +6	V	2
Switch node voltage	Vsw(DC)	27	V	2
	Vsw(AC)	30		2, 5
BOOT pin voltage	Vboot(DC)	32	V	2
	Vboot(AC)	36		2, 5
ON/OFF pin voltage	Von/off	–0.3 to VIN	V	2
PGOOD voltage	Vpgood	0 to VIN	V	3
Other pins voltage	Vic	–0.3 to (REG5 + 0.3)	V	2
TRK-SS dc current	Itrk	0 to 1	mA	3
IREF current	Iref	–120 to 0	μA	3
EO sink current	Iieo	0 to 2	mA	3
CO sink current	Iico	0 to 1	mA	3, 4
CO source current	Ioco	0 to 1	mA	3, 4
Operating junction temperature	Tj-opr	–40 to +150	°C	
Storage temperature	Tstg	–55 to +150	°C	

Notes: 1. Pt(25) represents a PCB temperature of 25°C, and Pt(100) represents 100°C.
2. Rated voltages are relative to voltages on the SGND and PGND pins.
3. For rated current, (+) indicates inflow to the chip and (–) indicates outflow.
4. Rated currents are only for slave mode.
5. Ratings for which "ac" is indicated are limited to within 100 ns.



Electrical Characteristics

(Ta = 25°C, VIN = VCIN = 5 V, unless otherwise specified)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Supply	VCIN start threshold	VH	4.1	4.3	4.5	V	
	VCIN shutdown threshold	VL	3.6	3.8	4.0	V	
	UVLO hysteresis	dUVL	—	0.5 *1	—	V	
	Input bias current	Iin	15	30	45	mA	Freq = 500 kHz, Duty = 50%
	Slave standby current	I-sin	2.1	3.5	4.9	mA	Von/off = 5 V, Vfb = 5 V
	Input shutdown current	Isd	3.1	4.5	5.9	mA	ON/OFF = 0 V
Remote On/off	Disable threshold	Voff	1.0	1.3	1.6	V	
	Enable threshold	Von	2.0	2.5	3.0	V	
	Input current	Ion/off	0.5	2.0	5.0	μA	Von/off = 1 V
Reference current generator	IREF pin voltage	VIref	1.75	1.80	1.85	V	Riref = 18 kΩ
Oscillator	CT oscillating frequency	Fct	—	500	—	kHz	CT = 180 pF
	CT higher trip voltage	Vhct	—	1.8 *1	—	V	CT = 180 pF
	CT lower trip voltage	Vlct	—	1 *1	—	V	CT = 180 pF
	CT source current	Ict-src	–176	–160	–144	μA	CT = 0.5 V
	CT sink current	Ict-snk	144	160	176	μA	CT = 2.3 V
Error amplifier	Feedback voltage	Vfb	588	600	612	mV	TRK-SS = 1 V
	FB input bias current	Ifb	–0.1	0	+0.1	μA	
	REFIN input bias current	Irefin	0.5	2	5	μA	
	Output source current	Ieo-src	150	200	250	μA	EO = 4 V, FB = 0 V
	Output sink current	Ieo-snk	3.5	7.0	14.0	mA	EO = 1 V, FB = 0.7 V
	Voltage gain	Av	—	80 *1	—	dB	
	Band width	BW	—	15 *1	—	MHz	
	Share pin resistance	Rshare	35	50	65	kΩ	EO = 0 V. Ishare = 1 V
Phase control comparator	Output source current	Ico-src	–3.0	–2.0	–1.0	mA	Share = 0 V, POS = 1 V, CO = 4.5 V
	Output sink current	Ico-snk	2.0	3.0	4.0	mA	Share = 1 V, POS = 0 V, CO = 0.5 V
	Input bias current	Ipos	0.5	2	5.0	μA	POS = 1.0 V
Current sense	CS current accuracy	Idh/Ics	—	13700 *1	—	—	
	Leading edge blanking time	TLD	—	60 *1	—	ns	
	CS comparator delay to output	Td-cs	—	65 *1	—	ns	
	OCP comparator threshold on CS pin	Vocp	1.4	1.5	1.6	V	
	Hiccup interval	Tocp	1.85	2.05	2.26	ms	CT = 180 pF
	RAMP offset voltage	Vramp-dc	70	100	130	mV	CT = 180 pF
	CS offset current	Ics-dc	—	300	—	μA	CS = 0 V
Power good indicator	Rising threshold on FB	Vgood	0.855	0.9	0.945	V	REFIN = 1.0 V
	Power good hysteresis	dVgood	—	50 *1	—	mV	
	Power good output low voltage	Vpglow	0.6	1.0	1.4	V	Ipgood = 2 mA

Note: 1. Reference values for design. Not 100% tested in production.

(Ta = 25°C, VIN = VCIN = 12 V, unless otherwise specified)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Over-voltage protection	OVP trip voltage	Vtovp	1.19	1.25	1.31	V	REFIN = 1.0 V
	Pre-OVP trip voltage	Vpovp	—	1.67	—	V	
Slope generator	Slope current	ISLP	7	10	13	μA	VSLP = 0 V
Clock generator	Clock frequency	Fclk	450	500	550	kHz	CT = 180 pF
	OUT high voltage	Vh-out	4.0	5.0	—	V	Rout = 51 kΩ to GND
	OUT low voltage	Vl-out	0	—	1.0	V	Rout = 51 kΩ to VCIN
	IN input bias current	Ibin	0.5	2.0	5.0	μA	V-in = 1 V
	IN input threshold	Vth-in	—	2.2	—	V	
	IN input hysteresis	Vth-hys	—	0.25	—	V	

Note: 1. Reference values for design. Not 100% tested in production.

Description of Operation

Peak Current Control

The control IC operates as current programmed control mode, in which output of the converter is controlled by the choice of the peak current from the high-side MOS FET. The current from this MOS FET is sensed by an active current sensing circuit (ACS), the output current of which is 1/13700 (50 ppm) of the MOS FET current. The ACS current is then converted to certain voltage by external resistor on the CS pin. The CS voltage is fed to the internal current sense comparator via the slope compensation circuit, and then compared with current control signal which determined from the error amplifier output voltage (EO) via an NPN transistor and resister network.

To start with, the RES pulse from pulse generator resets a latch, then the high-side MOS FET is turned on. The latch output (Q bar) is toggled when CS voltage reaches the level of the current control signal on EO, the high-side MOS FET is turned off, and the low-side MOS FET is turned off after a certain dead time interval. The IC remains in this state until the arrival of the next RES pulse.

Applying current information for the control loop, the converter loop compensation design will be simple.

Maximum Duty-Cycle Limitation

If the current-sense comparator output is not toggled 60-ns prior to the arrival of the next RES pulse, an internal maximum duty pulse is generated and forces toggling of SR latch. So, the duty cycle of the high-side MOS FET is limited by the maximum duty period.

The maximum duty period of the high-side MOS FET depends on its switching frequency.

$$\text{Max. duty} = 1 - 60\ \text{ns} \times \text{Fsw}$$

OCP Hiccup Operation

Eight times the voltage of CS exceeds 1.5 V, OCP hiccup circuit disables switching operation of the IC and MOS FETs.

Internal circuitry also pulls the TRK-SS pin down to SGND. The IC is turned off for a period of 1024 RES pulses; after this has elapsed, switching operation of the IC is restarted from the soft-start state.

UVLO and ON/OFF Control

When VCIN is under the start-up voltage, it is in the UVLO condition, functioning of the IC is disabled. The oscillator is turned off, both high and low-side MOS FETs are turned off, and the TRK-SS pin is pulled down. Furthermore, if the ON/OFF pin is the low state or left open, functioning of the IC is disabled and both MOS FETs are turned off.

Oscillator and Pulse Generator

The frequency of the oscillator (Fct) is set by the value of the external capacitor connected to the CT pin. The switching frequency (Fsw) is not the same as Fct, which also depends on the phase number N. The following equations determine these frequencies.

$$\text{Oscillator frequency: Fct} = 160\ \mu\text{A} / (2 \times \text{CT(F)} \times 0.8\ \text{V}) \times \text{N} \quad \text{(Hz)}$$

$$\text{Switching frequency: Fsw} = \text{Fct} / \text{N} \quad \text{(Hz)}$$

In multi-phase operation, connect the CT pins for all devices.

Soft Start

TRK-SS pin is provided for start-up setup. Both simple soft start and sequential start up can be realized with this pin setup. The error amp has two reference inputs and one input for soft start. One of lower voltage inputs of the two positive inputs is dominant for the amplifier. Therefore simply having CR charging circuit on TRK-SS pin is easier for soft start design.

The soft start period is determined with the equation as follows when TRK-SS pin has CR charging circuit.

$$Tss = -C \cdot R \cdot Ln (1 - REF / VCIN) \quad (s)$$

REF is REFIN voltage or 0.6 V in internal reference voltage.

Power Good Indicator

The power good indicator is useful for controlling timing when multiple converter systems are started up or shut down. Voltage on the FB pin is internally monitored by a power good comparator. The power good comparator compares the voltage on the pin with 90% of the reference voltage. When the comparator detects the FB voltage reaching the reference voltage, the Power Good pin becomes high impedance. If the voltage on FB goes over 125% or falls below 80% of the reference voltage, the pin is pulled down to SGND. PGOOD has an n-channel MOS FET operating as an open drain output and capable of sinking up to 2 mA of current.

Overvoltage Protection

When the output voltage (FB voltage) reaches or exceeds 125% of the reference voltage, switching stops immediately, the gate of the low-side MOS FET is latched in the high level, which causes shorting of the SW pin to GND. Resetting to leave the OVP mode is by resupplying VCIN or switching the circuit OFF and ON.

Pre-Overvoltage Protection

When the IC is starting up, an internal circuit monitors the voltage at the switch node and detects the output of excessive voltages. When a voltage exceeding 1.67 V is detected on the SW pin after release from the UVL state, the gate of the low-side MOS FET is latched in the high level, which causes shorting of the SW pin to GND. The low-side MOS FET remains in this state until VCIN is resupplied.

Multi Phase Operation

The R2J20751NP is a scalable solution. Pulling the FB pin of a device up to VCIN causes the device to operate as a slave. Clock timing is synchronized by connecting the CLK and CT pins of all devices. Current sharing is available by connecting the Share pins. The timing of switching of the signal on the SW pin is generated from the switching trigger signal on the IN pin. A device that has received the switching trigger signal outputs the same signal on its OUT pin for the next device one clock cycle later. The phase number is controllable by the internal phase control comparators of slave devices.

Slope Compensation

If peak current control leads to the duty cycle being over 50%, sub-harmonic oscillation is generated and the output voltage becomes unstable regardless of the negative feedback for constant voltage control. The duty cycle, D, is obtained from the following equation.

$$D = Vout / VIN \times 100 \ (\%)$$

To prevent such oscillation, add a constant slope to the slope of the voltage on the CS pin. This added slope is determined by 10 uA constant current output through the CSLP pin and the value of the connected external capacitor. Insufficient added slope leads to sub-harmonic oscillation. Too much added slope leads to voltage-mode operation and poorer response characteristics. An optimal slope (determined by the value of the external capacitor) needs to be set. The capacitance (Cslp) is determined by the following equation.

$$Cslp = 70\ \mu A \times 13700 \times Toff / (2 \times Ipp \times Rcs \times M)$$

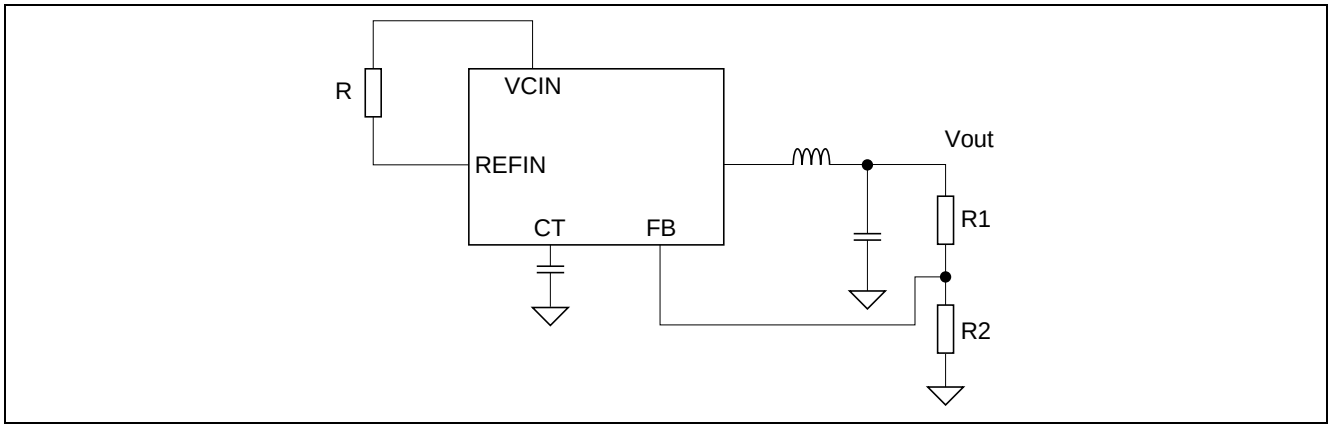
In the above equation, Toff is the off portion of the duty cycle (as time), Ipp is the ripple current of the output inductor, Rcs is the value of the external resistor connected to the CS pin, and M is the rate of the added slope. A capacitor value that leads to a greater setting of M in the range from 0.5 to 1.0 will lead to a greater added slope.

Output Voltage Setting

The error amplifier of the device has an accurate 0.6 V reference voltage and REFIN pin which can input reference voltage from external voltage. When reference voltage is 0.6 V, feedback loop leads to the FB pin a voltage of 0.6 V in case of stable condition on the converter. Therefore the output voltage is;

$$Vout = 0.6\ V \times (R1 + R2) / R2$$

REFIN pin should be pulled up to VCIN, when reference voltage refer to internal 0.6 V.



Loop Compensation

Peak-current control makes design in terms of phase margins easier than is the case with voltage control. This is because of differences between the characteristics of the PWM modulator and power stage in the two methods.

Figure 1 and 2 shows the behavior of the PWM modulator and power stage in the case of voltage control and peak current control, respectively.

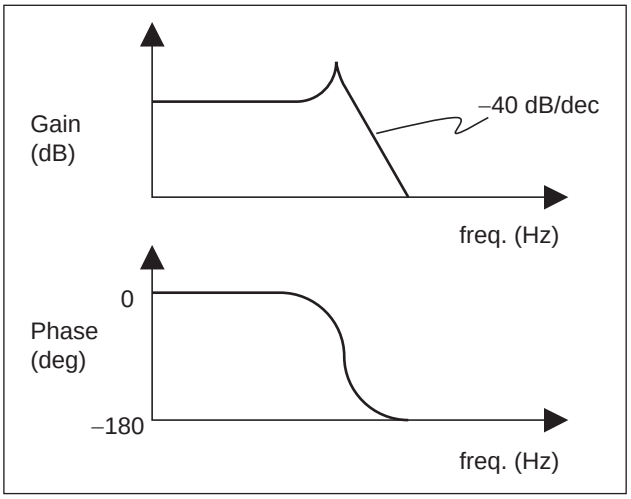


Figure 1 Bode Plot (Voltage Mode)

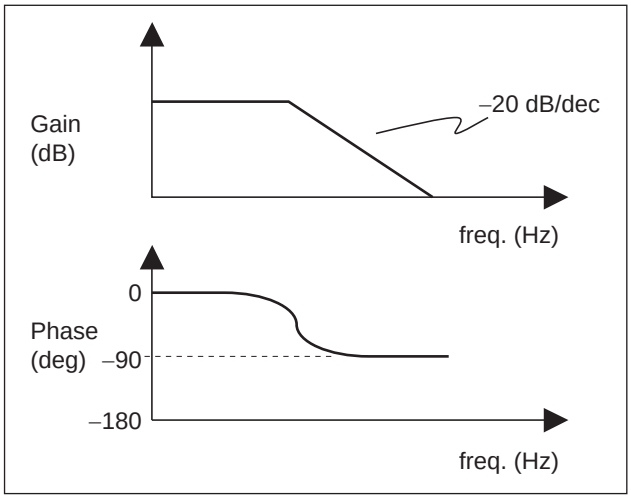


Figure 2 Bode Plot (Peak Curent Mode)

Feed-forward current to the modulator in the case of peak-current control means that the system is single pole, so we see a –20 dB/decade cutoff and phase margin of 90° in the Bode plot. In voltage control, the system configures a two-pole system. That is why rather complicated loop compensation of the error amplifier is required. Such as type-III compensation. The design of effective compensation is thus much simpler in the case of peak-current control (refer to figure 3).

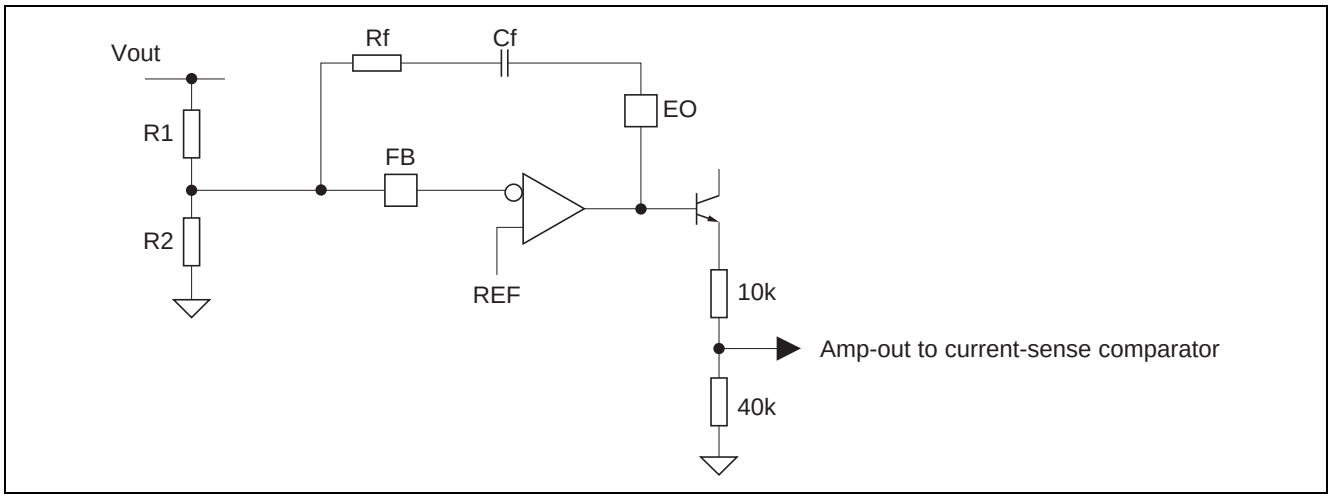


Figure 3 Error Amplifier Compensation

Design example;

Specification: L = 470 nH, Co = 600 μF, Fsw = 500 kHz, Vin = 5 V, Vout = 1.5 V, R1 = 1 kΩ, R2 = 1 kΩ, RCS = 820 Ω

1. Flat band gain of error amplifier

   The flat band gain is; $Af = Rf / (R1 // R2) \times 4 / 5 \times \{R2 / (R1 + R2)\}$

   Hence,

   $Rf = 5 / 4 \times Af \times (R1 // R2) / \{R2 / (R1 + R2)\}$ .....(1)

   In the Bode plot, the total gain should be lower than 1 (0 dB) at the switching frequency.
   The total gain at Fsw (= Asw) depends on the flat-band gain, so Af should be expressed as follows;

   $Af = Asw \times 2\pi \times Fsw \times Co \times RCS / Nt$ ……(2)

   Here, $Nt = Idh / Ics = 13700$

   In the typical way, the value chosen for Asw is in the range from 0.1 to 0.5, since this produces a stable control loop. The transient response will be faster if a large Asw is adopted, but the system might be unstable.
   We choose 0.2 for Asw in the example below.

   $Af = 0.2 \times 2\pi \times 500\ kHz \times 600\ \mu F \times 820\ \Omega / 13700 = 22.564$

   $Rf = 5 / 4 \times 22.564 \times 0.6\ k\Omega / (2 / 3) = 25.385\ k\Omega$

   Therefore, we select a value of 24 kΩ for Rf.

2. Selecting the Cf value to determine the frequency of the zero.

   The frequency of the zero established by Cf and Rf is about ten times the frequency of the pole for the power stage and modulator.

   We must start with the dc gain of the power stage and modulator.

$$A0 = \frac{Nt/RCS \times L \times Vin \times Fsw}{SQRT\{Vin^2 - 8 \times L \times Vin \times Fsw \times (VCS0 \times Nt / RCS)\}} \quad \text{……(3)}$$

   Here VCS0 is the peak ac voltage on CS pin when the load current is zero, thus

   $VCS0 = 0.5 \times RCS \times (Vin - Vout) \times Vout / (L \times Vin \times Fsw) / 13700$ ……(4)

   $= 0.5 \times 820\ \Omega \times (5\ V - 1.5\ V) \times 1.5\ V / (470\ nH \times 5\ V \times 500\ kHz) / 13700$

   $= 0.134\ V$

equation (3),

$$A0 = \frac{Nt/RCS \times L \times Vin \times Fsw}{SQRT\{Vin^2 - 8 \times L \times Vin \times Fsw \times (VCS0 \times Nt / RCS)\}} \quad \ldots\ldots(3)$$

$$= \frac{13700 / 820\ \Omega \times 470\ nH \times 5\ V \times 500\ kHz}{SQRT\{5\ V^2 - 8 \times 470\ nH \times 5\ V \times 500\ kHz \times (0.134\ V \times 13700 / 820\ \Omega)\}}$$

$$= \frac{19.63}{SQRT\{3.955\}}$$

$$= 9.871$$

The frequency of the pole established by the power stage and modulator is

$F0 = Nt / (2 \pi \times Co \times RCS \times A0)$ .....(5)

Thus,

$F0 = 13700 / (2 \pi \times 600\ \mu F \times 820\ \Omega \times 9.871) = 448.967\ Hz$

Thus,

$Fzero = 10 \times F0 = 4.489\ kHz$

$Cf = (2 \pi \times Fzero \times Rf)^{-1} = (2 \pi \times 4.489\ kHz \times 24\ k\Omega)^{-1} = 1477\ pF$

Therefore, we select 1500 pF for Cf.

Basically, the transient response is faster when Cf is smaller, but too small a value will make the system-loop unstable.

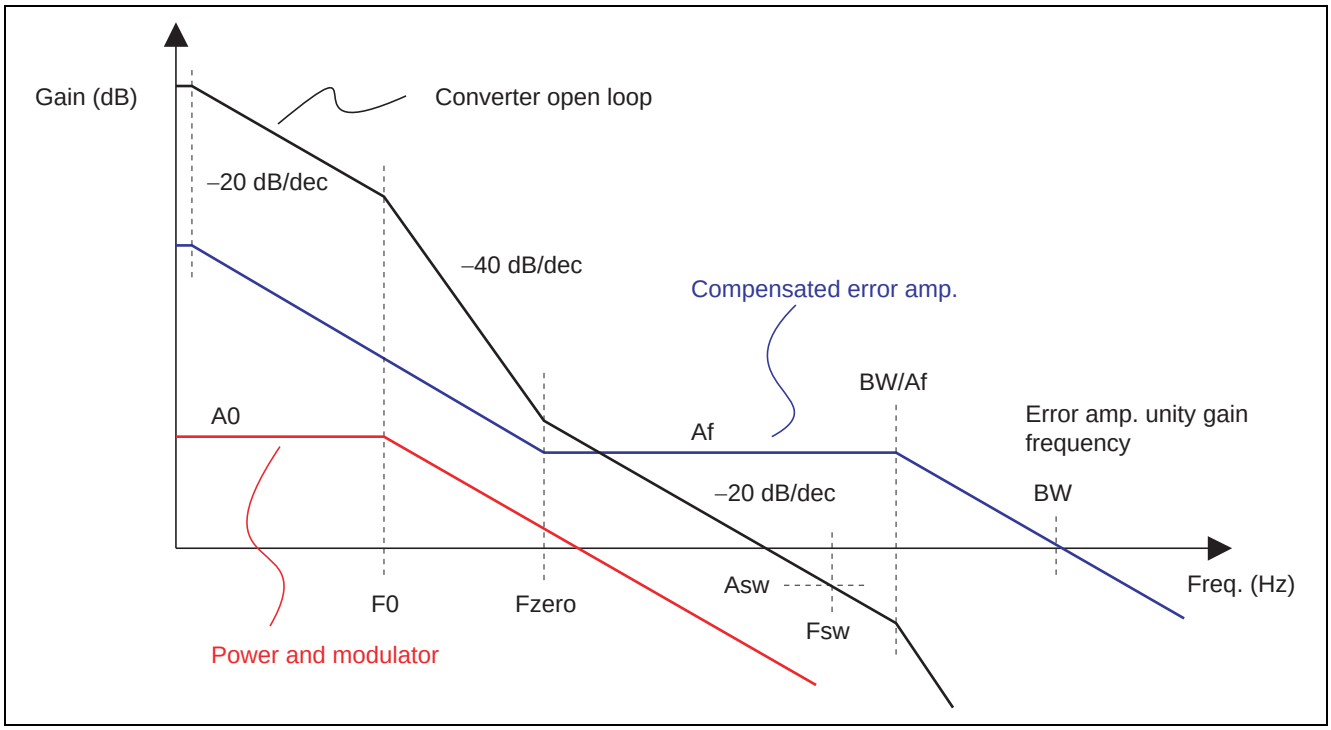


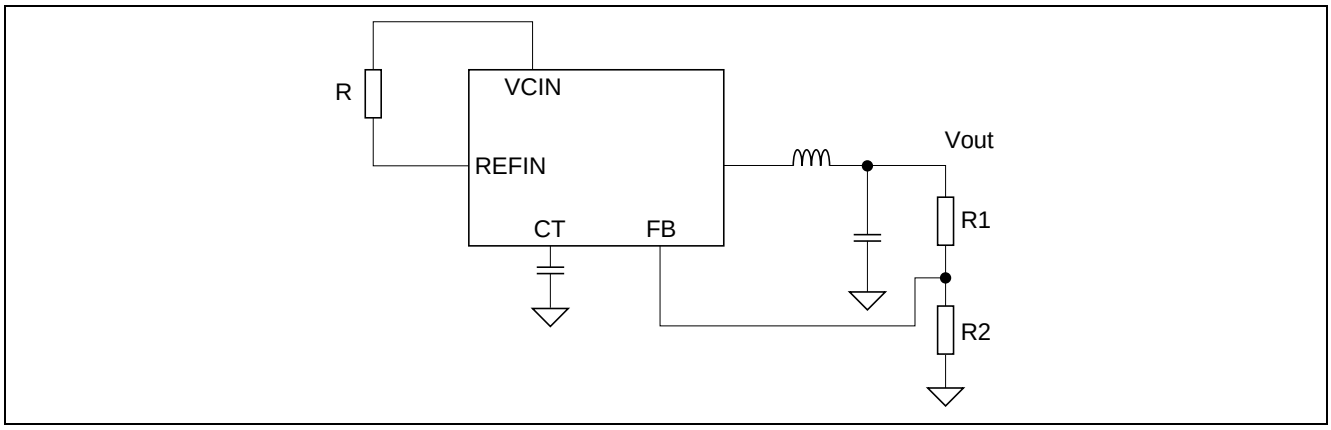
Figure 4

Study of Vout Accuracy

The nominal output voltage is calculated as

$$Vout = VFB \times (R1 + R2) / R2 \quad .....(6)$$

Here, the typical FB voltage is 0.6 V.



The accuracy of Vout is strongly dependent on the variation of VFB, R1 and R2. VFB has variation of 1% and resistance intrinsically has a certain variation. When we take the variation in resistance into account, equation (6) is extended to produce equation (7).

$$Vout = \frac{R1 \times K1 + R2 \times K2}{R2 \times K2} \times FB$$

$$= \frac{R1 \times K1 / K2 + R2}{R2} \times FB \quad \ldots\ldots(7)$$

Here, K1 and K2 are coefficients, Both are 1.00 in the ideal case.

By equation (6), R1 is chosen as;

$$R1 = \left[\frac{Vout\ (typical)}{VFB\ (typical)} - 1 \right] \times R2 \quad \ldots\ldots(8)$$

Substituting the expression for R1 into equation (7) yields the following

$$Vout = VFB \times \left\{ \left[\frac{Vout\ (typical)}{VFB\ (typical)} - 1 \right] \times \frac{K1}{K2} + 1 \right\} \quad \ldots\ldots(9)$$

Therefore, variation in Vout is expressed as

$$\frac{Vout}{Vout\ (typical)} = \left[\frac{VFB}{Vout\ (typical)} \times \left\{ \left[\frac{Vout\ (typical)}{VFB\ (typical)} - 1 \right] \times \frac{K1}{K2} + 1 \right\} - 1 \right] \times 100 \ (\%) \quad \ldots\ldots(10)$$

The accuracy of Vout can be estimated by using equation (10).

For Example, if Vout (typical) = 1.5 V, resistance variation is 1% (i.e K1, K2 = 1.01 and 0.99), and VFB = 588 mV to 612 mV.

$$\frac{\text{Vout}}{\text{Vout (typical)}} = \left[\frac{\text{VFB}}{\text{Vout (typical)}} \times \left\{ \left[\frac{\text{Vout (typical)}}{\text{VFB (typical)}} - 1 \right] \times \frac{\text{K1}}{\text{K2}} + 1 \right\} - 1 \right] \times 100 \ (\%) \quad \ldots\ldots(10)$$

$$= \left[\frac{612 \text{ mV}}{1.5 \text{ V}} \times \left\{ \left[\frac{1.5 \text{ V}}{600 \text{ mV}} - 1 \right] \times \frac{1.01}{0.99} + 1 \right\} - 1 \right] \times 100 \ (\%)$$

$$= 3.23\%$$

or

$$= \left[\frac{588 \text{ mV}}{1.5 \text{ V}} \times \left\{ \left[\frac{1.5 \text{ V}}{600 \text{ mV}} - 1 \right] \times \frac{0.99}{1.01} + 1 \right\} - 1 \right] \times 100 \ (\%)$$

$$= -3.16\%$$

Therefore, the output accuracy will be ±3.2% under the above conditions.

Figure 5 shows the relationship between the accuracy of the resistance and the accuracy of the output voltage. The resistor value must have an accuracy of 0.5% if the variation in output voltage from the system is to be kept within three percent across the voltage range from 0.6 V to 3.3 V.

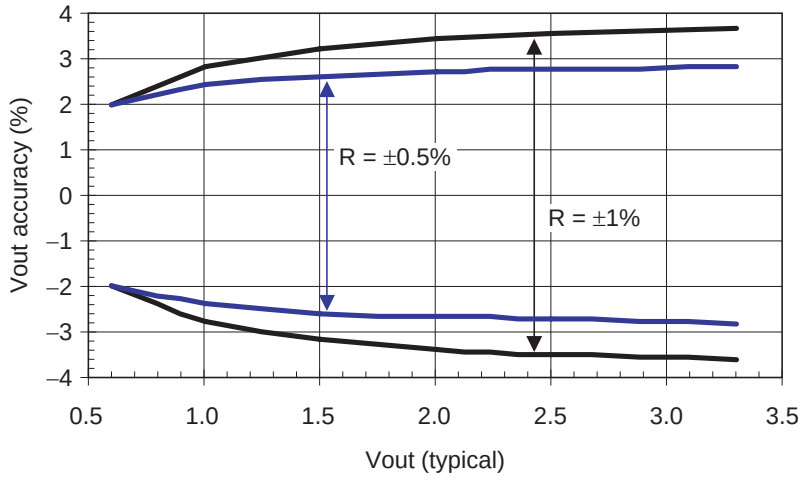
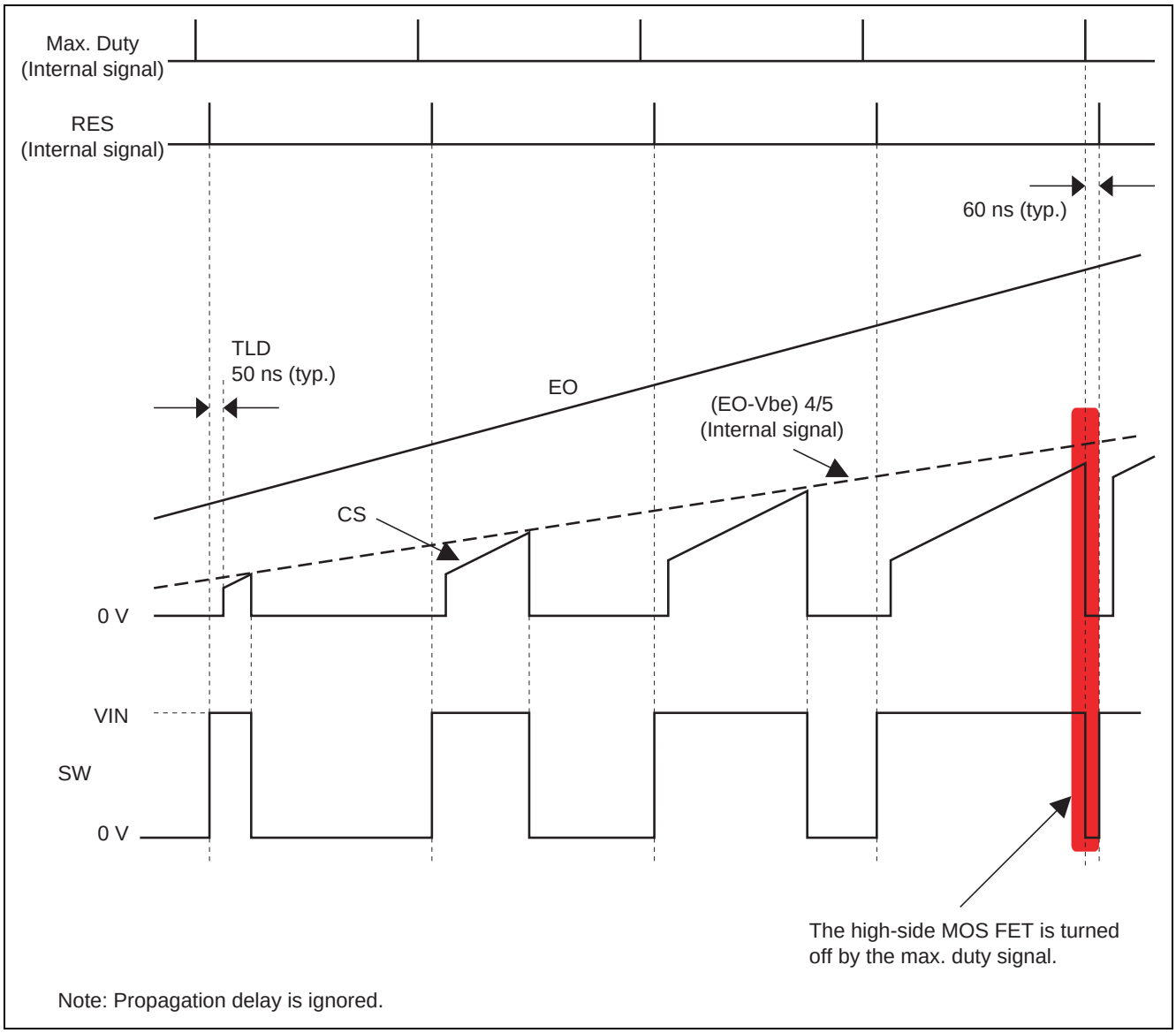


Figure 5 Vout Accuracy vs. Vout Set Voltage

Timing Chart

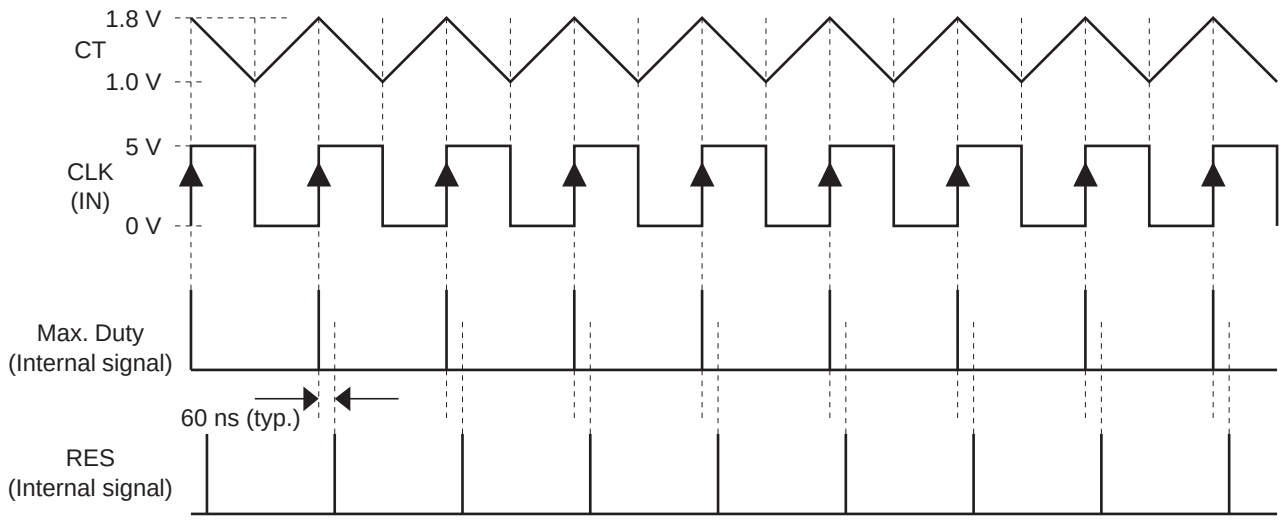
Peak Current Control



Note: Propagation delay is ignored.

Oscillator and Pulse Generator

1. Standalone operation or working as Master Chip in parallel configuration with other chips.



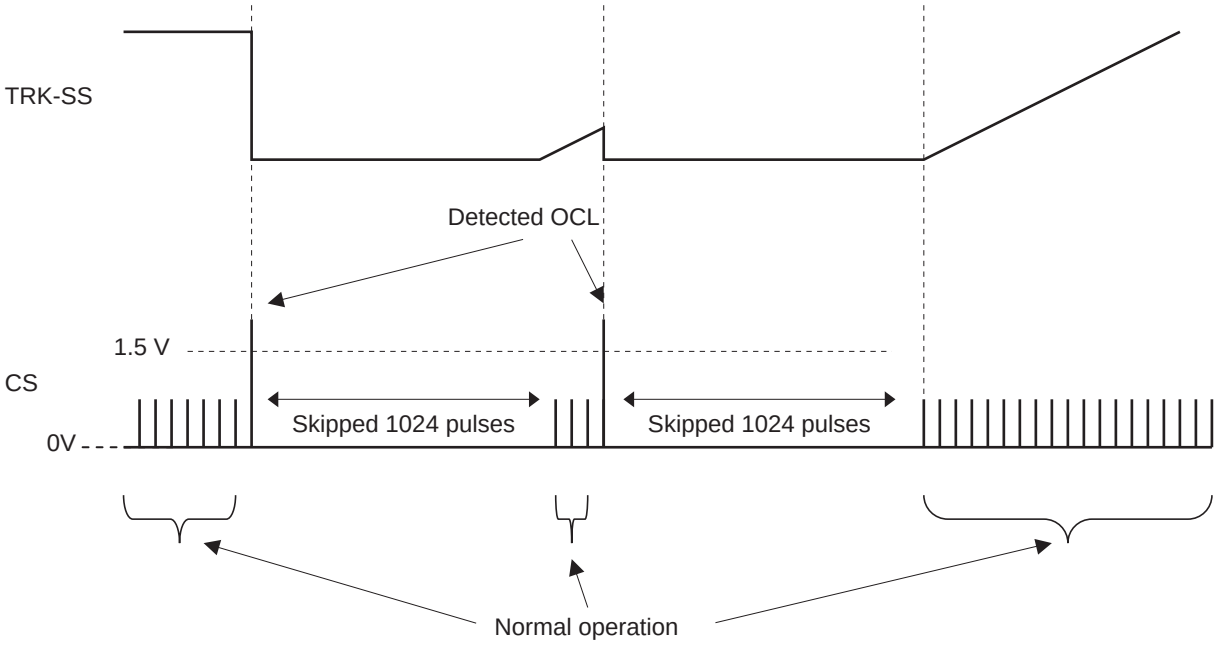
Note: Propagation delay is ignored.

Switching frequency for CT

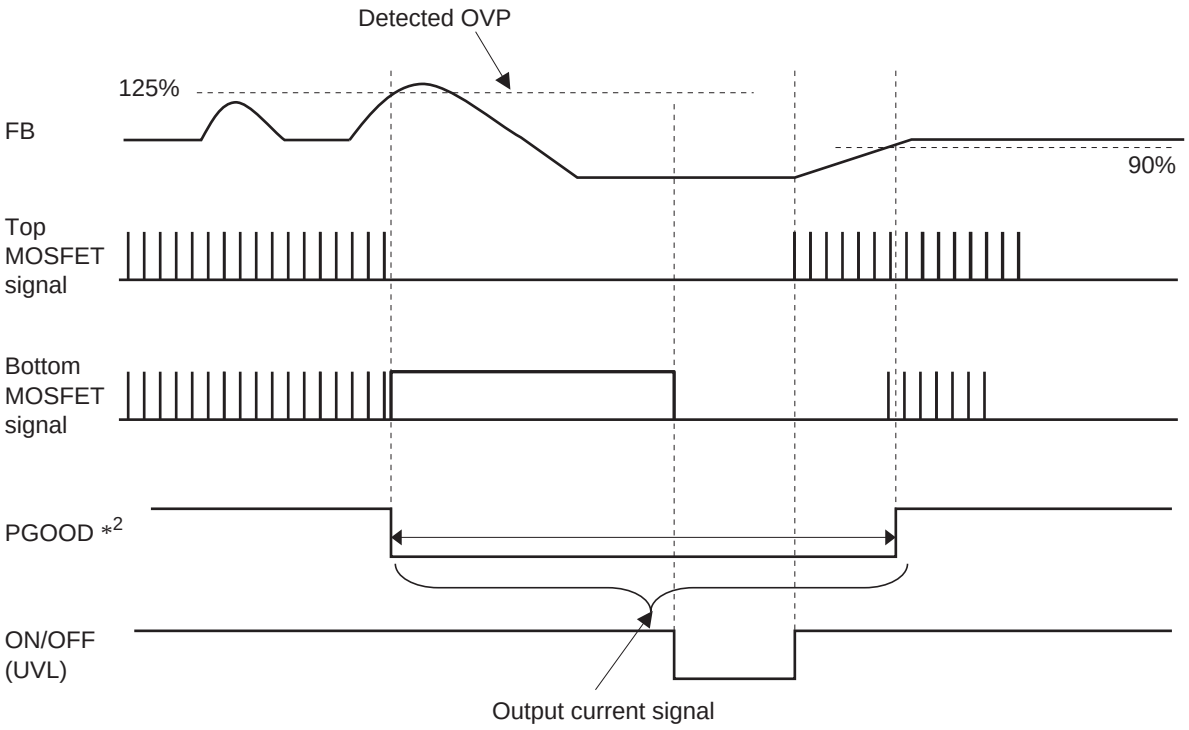
$$Fsw = \frac{160\ \mu A}{2 \times (CT(F) + 20\ pF) \times 0.8\ V \times N}\ (Hz)$$

Frequency set range: 200 kHz to 1 MHz

Hiccup Operation when the Over-Current Limit (OCL) is Reached



Note: Propagation delay is ignored.



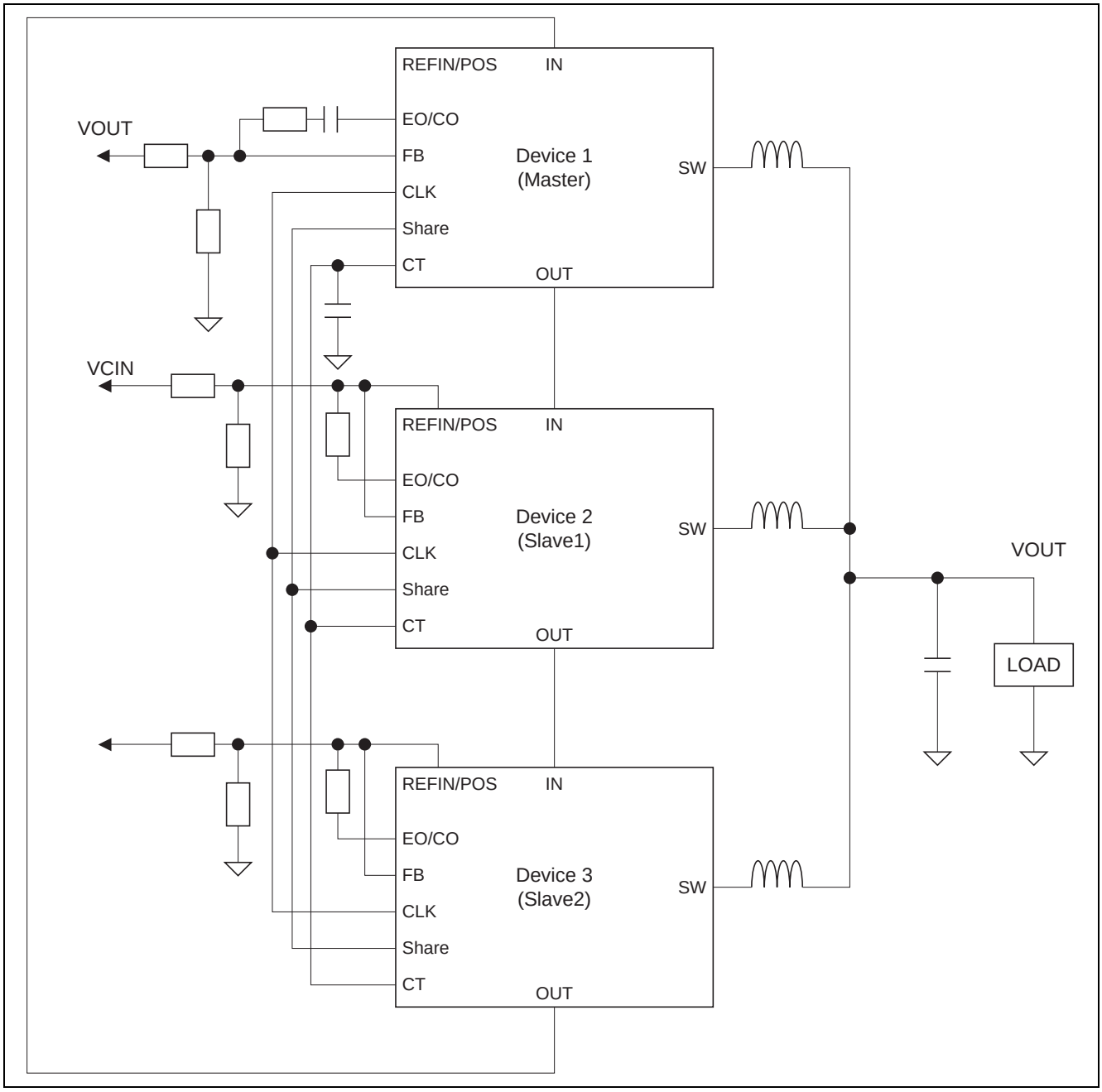
Note: 2. Connected 51 kΩ resistor between PGOOD and VCIN.

Applications

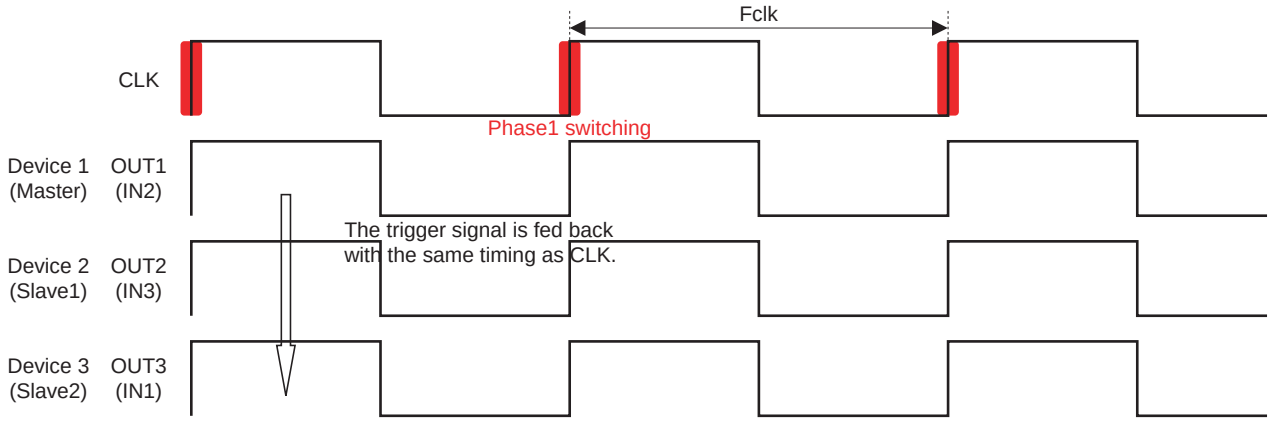
Multi Phase Operation

Tie each CT, CLK and Share pin.

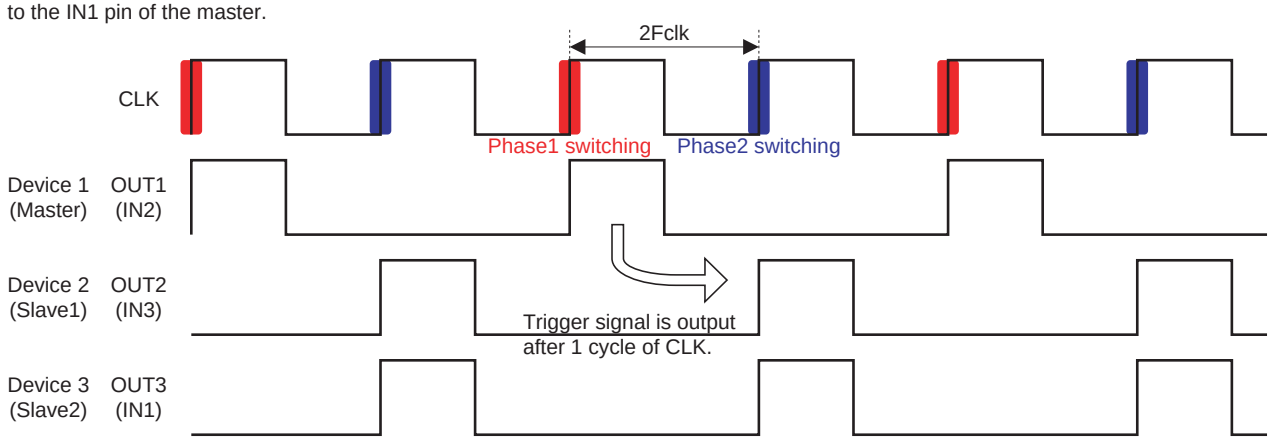
Connect OUT pin to IN pin of next switching device.



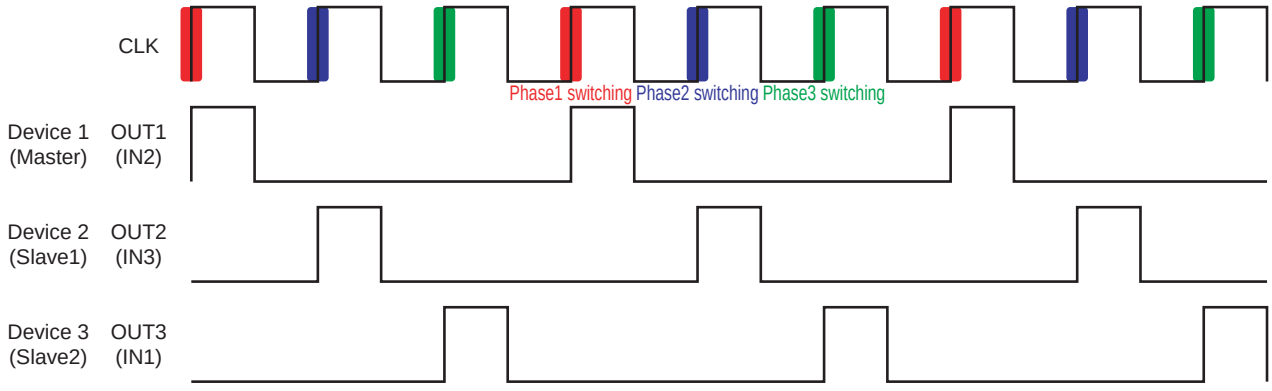
Multi Phase Operation Waveforms (3 Phase)



For the three-phase system, only the master device operates while the voltages on the POS pins of slave devices 1 and 2 are higher than the voltage on the Share pins. In single-phase operation, although the switching trigger signal is input on the IN pin of both slaves, both slaves 1 and 2 are disabled so they output the signal on the OUT pin with the same timing as the clock signal (CLK), feeding it back to the IN1 pin of the master.



When only slave 1 is enabled, that is, the voltage on the POS pin is higher than the voltage on the Share pins only for slave 2, operation becomes two phase. The frequency is double that in single-phase mode because slave 1 supplies current at the frequency of CLK that is applied to the CT pin with the same timing as the master. Slave 1 outputs a switching trigger signal one clock cycle after it has received a switching trigger signal. Accordingly, the phase of the timing for turning slave 1 on lags 90? behind that for the master.



When slaves 1 and 2 are both enabled, the frequency is triple that in single-phase mode because slaves 1 and 2 supply current at the frequency of CLK that is applied to the CT pin with the same timing as the master. Switching operation is with the timing of the CLK signal, so the phase angle becomes 120? in three-phase operation and the phase shift is automatic.

Phase Control

The device incorporates a comparator for control of the phase number. Pulling the voltage on the FB pin up to that on VCIN exchanges the phase control comparator for the error amplifier, and the device operates as a slave. In this case, the output of the comparator (CO) is exchanged for the output of the error amplifier (EO), and the positive input (REFIN) of the error amplifier is exchanged for the positive input (POS) for the comparator. Furthermore, the inverse input for the comparator is internally connected to the Share pin. The level where the phase number is switched is set by an external resistor.

Design example;

Specification: L = 470 nH, Fsw = 500 kHz, Vin = 5 V, Vout = 1.5 V, RCS = 820 Ω,
Phase switching level is Iout = 10 A, hysteresis = 3.48 A

1. Deriving the voltage on the Share pins to return to single-phase operation with Iout = 6.52 A (3.48 A of hysteresis) from two-phase operation with Iout = 10 A.
   The peak of the output ripple current is:
   $Ipp\ (10\ A) = (VIN - Vout) / L \times Vout / VIN / Fsw / 2 + Iout\ (10\ A) = 12.23\ A$

   When Iout = 6.52 A in two-phase mode, current from each device is 3.26 A. Thus,
   $Ipp\ (3.26\ A) = (VIN - Vout) / L \times Vout / VIN / Fsw / 2 + Iout\ (3.26\ A) = 5.49\ A$

   The ratio between currents for the sense MOS FET and main MOS FET is 1:13700, so a bias current of 300 μA flows through the CS pin.
   Thus, voltages on the CS pin are:
   $Vcs\ (10\ A) = (Ipp\ (10\ A) / 13700 + 300\ \mu A) \times Rcs = 978\ mV$ and

   $Vcs\ (3.26\ A) = (Ipp\ (3.26\ A) / 13700 + 300\ \mu A) \times Rcs = 575\ mV$.

   The non-inverted input terminal of the internal current sense comparator has an offset voltage of 0.2 V, and 40-kΩ and 10-kΩ resistors are connected to the inverted input terminal.
   Therefore, the Share voltages are:
   $Vshare\ (10\ A) = (Vcs\ (10\ A) + 0.2\ V) \times 5 / 4 = 1.473\ V$ and .....(11)

   $Vshare\ (3.26\ A) = (Vcs\ (3.26\ A) + 0.2\ V) \times 5 / 4 = 0.969\ V$. .....(12)

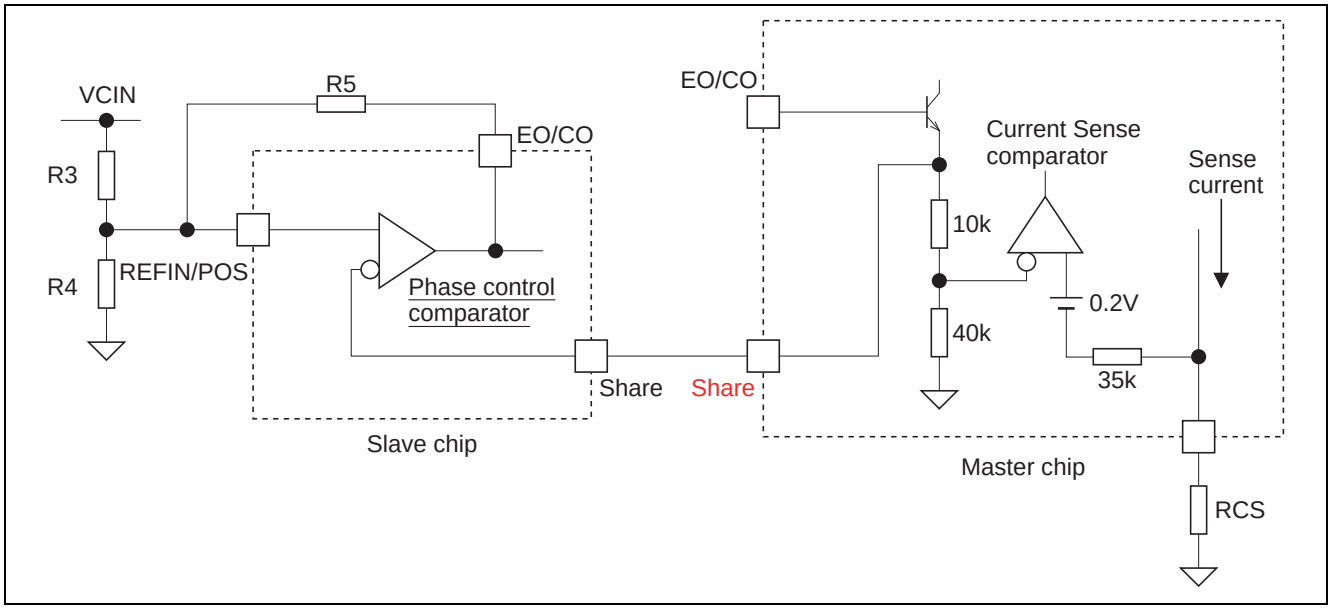
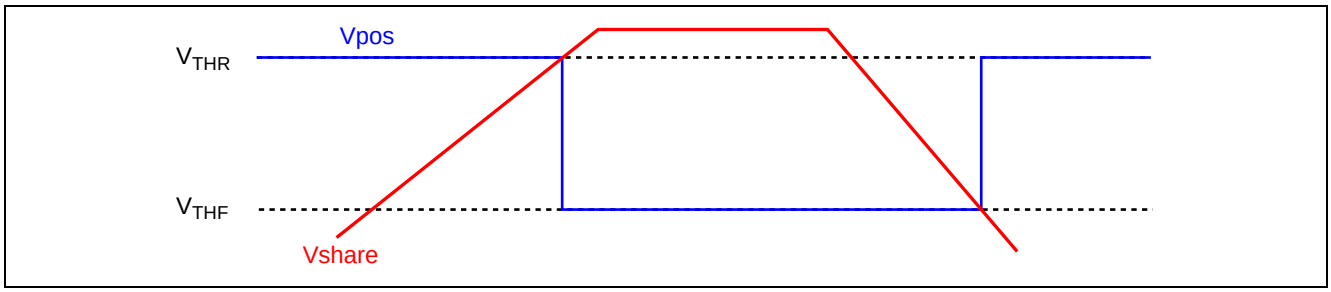


Figure 6 Phase Switching Control



2. Selecting the external resistors

When the output of phase control comparator becomes low, switching operation of the slave device starts and operation becomes two phase. According to the results of (11) and (12), VTHR and VTHF are 1.473 V and 0.969 V. These become the voltages on the POS pins (comparator non-inverted input pin). VTHR is the start-up level for the slave device and VTHF is the shut-down level for the slave device.

We set the output current of CO at around 100 μA when the voltage on Share is 1.379 V. In this case, R5 is:

$R5 = (V_{CIN} – 1.379) / 100\ \mu A = 35.27\ k\Omega$

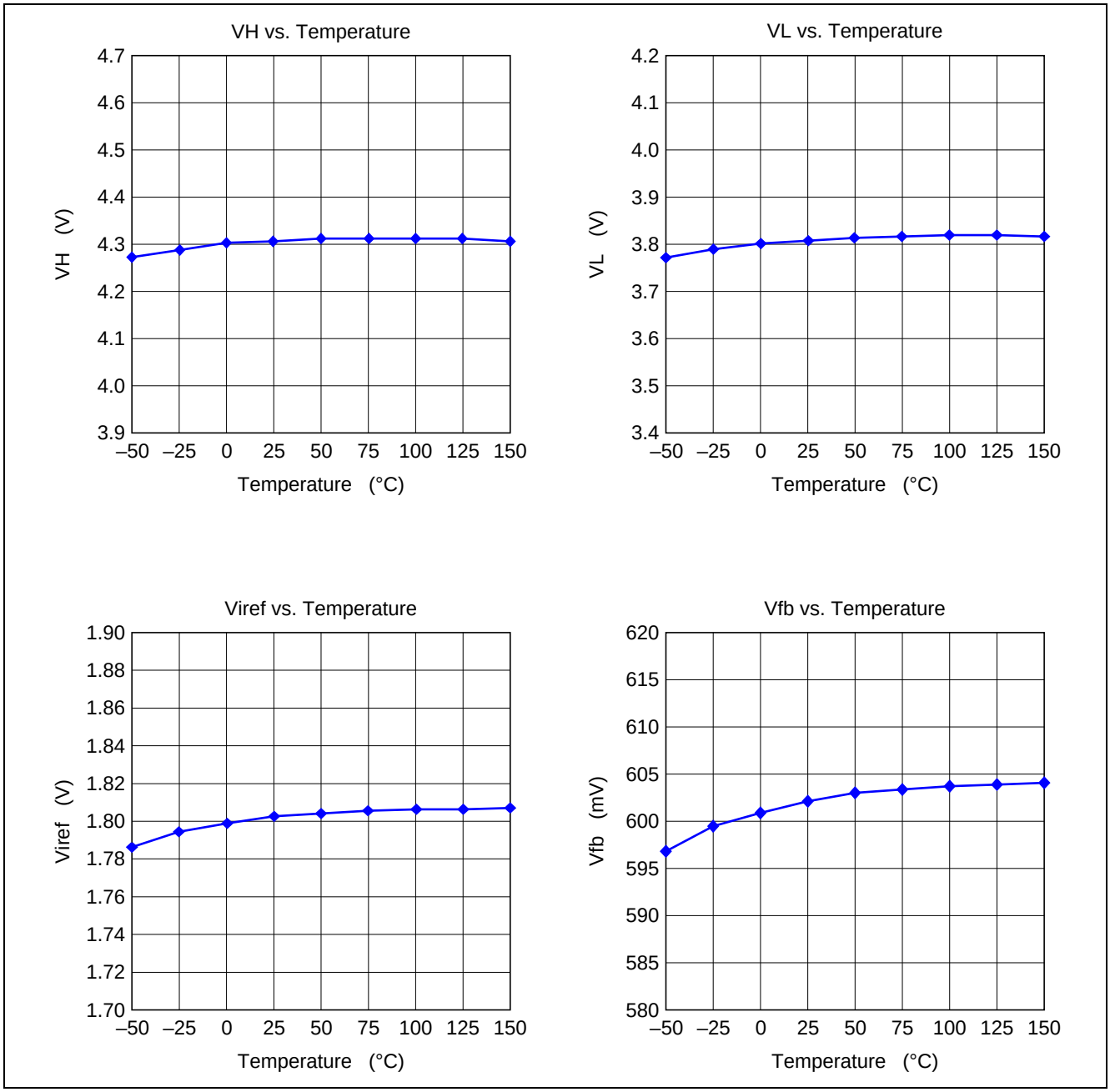
The formulae that express R3 and R4 are:

$R3 = R4 \times R5 / (R4 + R5) \times (V_{CIN} – V_{THF}) / V_{THF} = 18.34\ k\Omega$ and

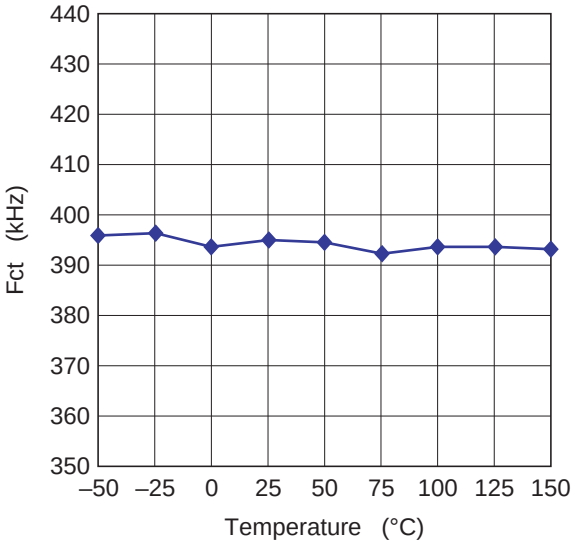
$R4 = R5 \times (V_{THR} – V_{THF}) / (V_{CIN} – V_{THR}) = 5.04\ k\Omega$.

With E24-series resistors, R3 = 18 kΩ, R4 = 5.1 kΩ, and R5 = 36 kΩ.

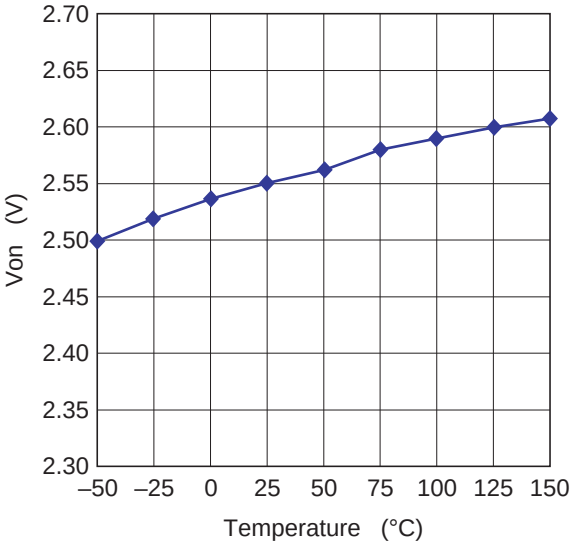
Main Characteristics



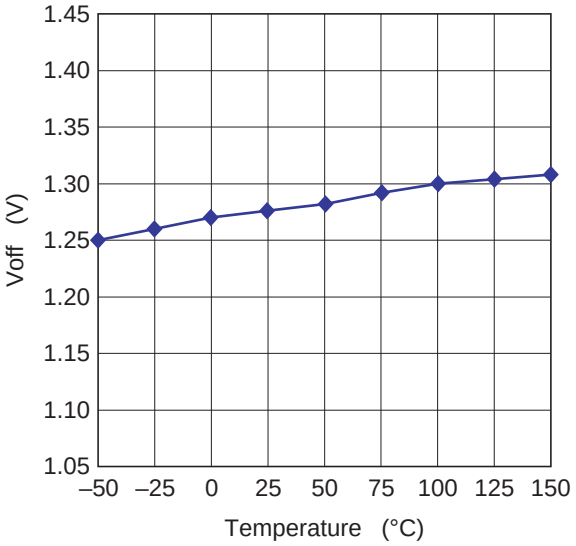
Fsync vs. Temperature



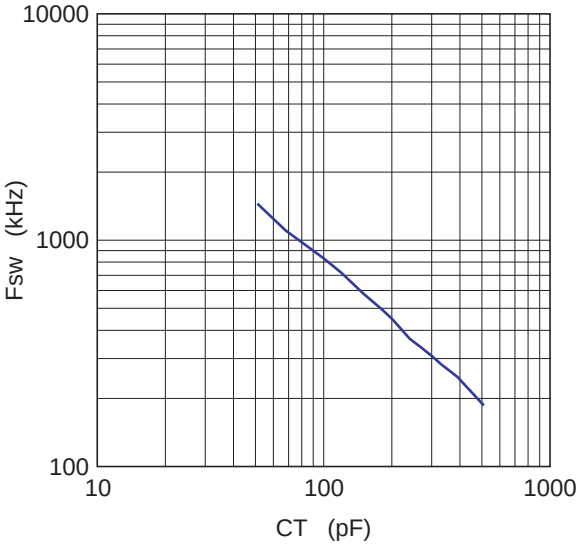
Von vs. Temperature



Voff vs. Temperature

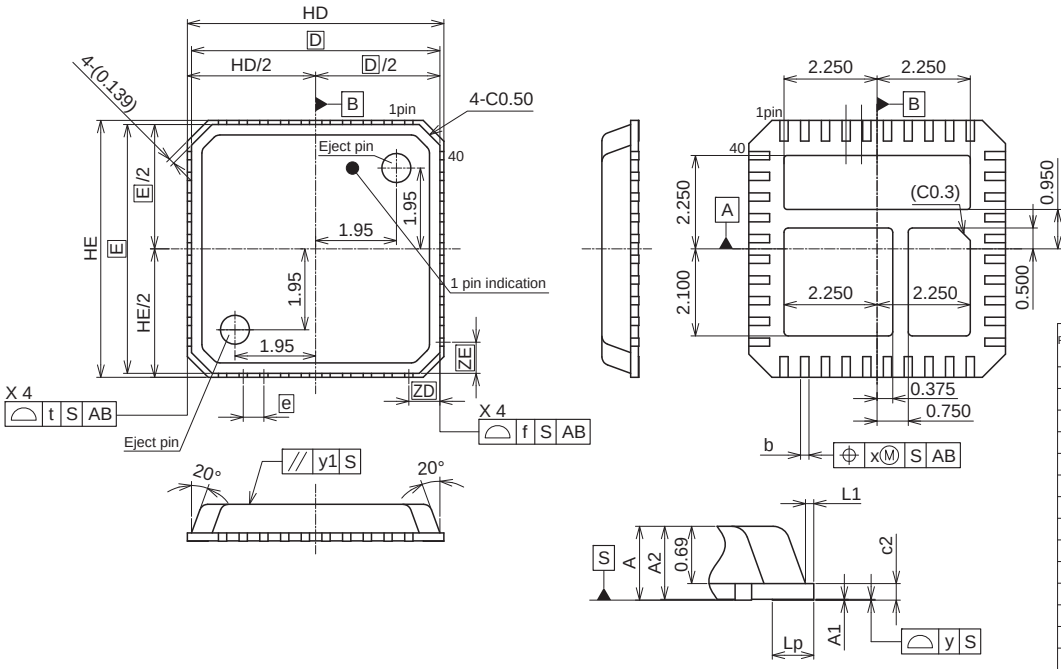


Fsw vs. CT



Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
—	PVQN0040KD-A	—	0.07



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	6.00	—
E	—	6.00	—
A2	—	—	—
f	—	—	0.20
A	—	—	0.95
A1	0.005	—	—
b	0.17	0.22	0.27
e	—	0.50	—
Lp	0.40	0.50	0.60
x	—	—	0.05
y	—	—	0.05
y1	—	—	0.20
t	—	—	0.20
HD	6.15	6.20	6.25
HE	6.15	6.20	6.25
ZD	—	0.75	—
ZE	—	0.75	—
L1	—	0.10	—

Ordering Information

Part Name	Quantity	Shipping Container
R2J20751NP#G0	2500 pcs	Taping Reel

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.
   - "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.
   - "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.
   - "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

RENESAS

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
7F, No. 363 Fu Shing North Road Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

Colophon 1.0