Data Sheet April 2000 File Number 2915.5

100MHz, Low Noise, Precision Operational Amplifier

The HA-5221 is a single high performance dielectrically isolated, op amp, featuring precision DC characteristics while providing excellent AC characteristics. Designed for audio, video, and other demanding applications, noise (3.4nV/$\sqrt{Hz}$ at 1kHz), total harmonic distortion (<0.005%), and DC errors are kept to a minimum.

The precision performance is shown by low offset voltage (0.3mV), low bias currents (40nA), low offset currents (15nA), and high open loop gain (128dB). The combination of these excellent DC characteristics with the fast settling time (0.4µs) makes the HA-5221 ideally suited for precision signal conditioning.

The unique design of the HA-5221 gives it outstanding AC characteristics not normally associated with precision op amps, high unity gain bandwidth (35MHz) and high slew rate (25V/µs). Other key specifications include high CMRR (95dB) and high PSRR (100dB). The combination of these specifications will allow the HA-5221 to be used in RF signal conditioning as well as video amplifiers.

For MIL-STD-883C compliant product and Ceramic LCC packaging, consult the HA-5221/883C data sheet. (Intersil AnswerFAX (321-724-7800) Document #3716.)

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HA7-5221-5	0 to 75	8 Ld CERDIP	F8.3A
HA9P5221-5 (H52215)	0 to 75	8 Ld SOIC	M8.15

Features

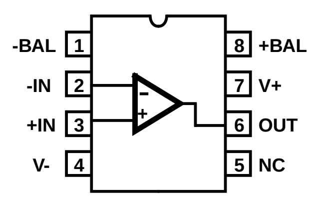
- Gain Bandwidth Product. 100MHz
- Unity Gain Bandwidth. 35MHz
- Slew Rate 25V/µs
- Low Offset Voltage 0.3mV
- High Open Loop Gain. 128dB
- Low Noise Voltage at 1kHz. . . . . 3.4nV/$\sqrt{Hz}$
- High Output Current 56mA
- Low Supply Current 8mA

Applications

- Precision Test Systems
- Active Filtering
- Small Signal Video
- Accurate Signal Processing
- RF Signal Conditioning

Pinout

HA-5221
(CERDIP, SOIC)
TOP VIEW



Absolute Maximum Ratings

Supply Voltage Between V+ and V- Terminals. 35V
Differential Input Voltage (Note 1) 5V
Output Current Short Circuit Duration . . . . Indefinite

Operating Conditions

Temperature Range
HA-5221-5 . . . . 0^oC to 75^oC

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CERDIP Package	135	50
SOIC Package	157	N/A

Maximum Junction Temperature (Hermetic Package) . . . . 175^oC
Maximum Junction Temperature (Plastic Package) . . . . 150^oC
Maximum Storage Temperature Range . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Input is protected by back-to-back zener diodes. See applications section.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$V_{SUPPLY} = \pm 15V$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (^oC)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
Input Offset Voltage		25	-	0.30	0.75	mV
		Full	-	0.35	1.5	mV
Average Offset Voltage Drift		Full	-	0.5	-	$\mu V/^oC$
Input Bias Current		25	-	40	100	nA
		Full	-	70	200	nA
Input Offset Current		25	-	15	100	nA
		Full	-	30	150	nA
Input Offset Voltage Match		25	-	400	750	µV
		Full	-	-	1500	µV
Common Mode Range		25	±12	-	-	V
Differential Input Resistance		25	-	70	-	kΩ
Input Noise Voltage	f = 0.1Hz to 10Hz	25	-	0.25	-	μV_{P-P}
Input Noise Voltage Density (Notes 3, 11)	f = 10Hz	25	-	6.2	10	$nV/\sqrt{Hz}$
	f = 100Hz	25	-	3.6	6	$nV/\sqrt{Hz}$
	f = 1000Hz	25	-	3.4	4.0	$nV/\sqrt{Hz}$
Input Noise Current Density (Notes 3, 11)	f = 10Hz	25	-	4.7	8.0	$pA/\sqrt{Hz}$
	f = 100Hz	25	-	1.8	2.8	$pA/\sqrt{Hz}$
	f = 1000Hz	25	-	0.97	1.8	$pA/\sqrt{Hz}$
THD+N	Note 4	25	-	<0.005	-	%
TRANSFER CHARACTERISTICS						
Large Signal Voltage Gain	Note 5	25	106	128	-	dB
		Full	100	120	-	dB
CMRR	$V_{CM} = \pm 10V$	Full	86	95	-	dB
Unity Gain Bandwidth	-3dB	25	-	35	-	MHz

Electrical Specifications V_{SUPPLY} = ±15V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
Gain Bandwidth Product	1kHz to 400kHz	25	-	100	-	MHz
Minimum Stable Gain		Full	1	-	-	V/V
OUTPUT CHARACTERISTICS						
Output Voltage Swing	R_L = 333Ω	Full	±10	-	-	V
	R_L = 1kΩ	25	±12	±12.5	-	V
	R_L = 1kΩ	Full	±11.5	±12.1	-	V
Output Current	V_{OUT} = ±10V	Full	±30	±56	-	mA
Output Resistance		25	-	10	-	Ω
Full Power Bandwidth	Note 6	25	239	398	-	kHz
TRANSIENT RESPONSE (Note 11)						
Slew Rate	Notes 7, 11	Full	15	25	-	V/µs
Rise Time	Notes 8, 11	Full	-	13	20	ns
Overshoot	Notes 8, 11	Full	-	28	50	%
Settling Time (Notes 9, 10)	0.1%	25	-	0.4	-	µs
	0.01%	25	-	1.5	-	µs
POWER SUPPLY						
PSRR	V_S = ±10V to ±20V	Full	86	100	-	dB
Supply Current		Full	-	8	11	mA

NOTES:

3. Refer to typical performance curve in data sheet.
4. A_{VCL} = 10, f_O = 1kHz, V_O = 5V_{RMS}, R_L = 600Ω, 10Hz to 100kHz, minimum resolution of test equipment is 0.005%.
5. V_{OUT} = 0 to ±10V, R_L = 1kΩ, C_L = 50pF.
6. Full Power Bandwidth is calculated by: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}, V_{PEAK} = 10V$.
7. V_{OUT} = ±2.5V, R_L = 1kΩ, C_L = 50pF.
8. V_{OUT} = ±100mV, R_L = 1kΩ, C_L = 50pF.
9. Settling time is specified for a 10V step and A_V = -1.
10. See Test Circuits.
11. Guaranteed by characterization.

Test Circuits and Waveforms

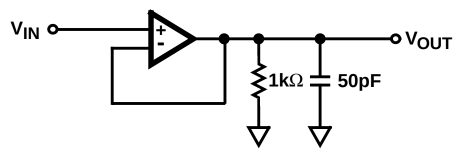
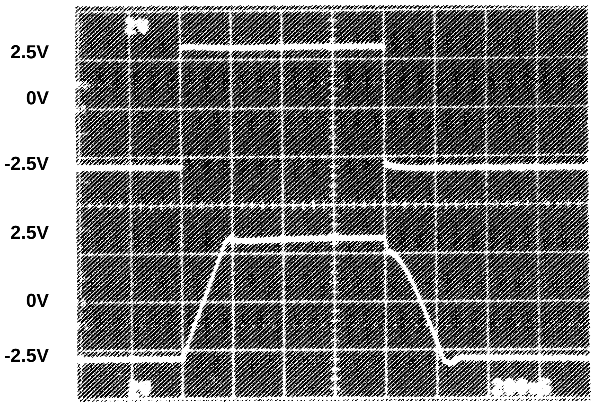


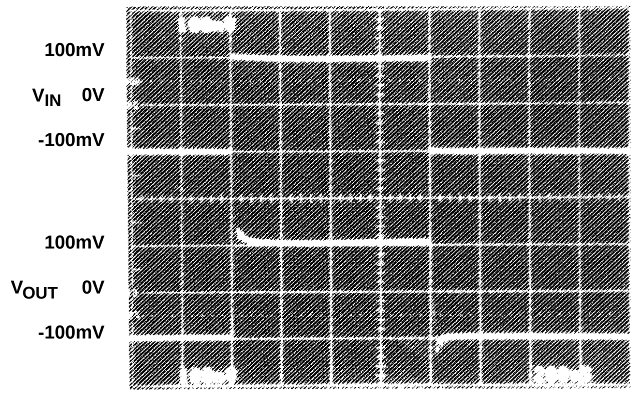
FIGURE 1. TRANSIENT RESPONSE TEST CIRCUIT

Test Circuits and Waveforms (Continued)



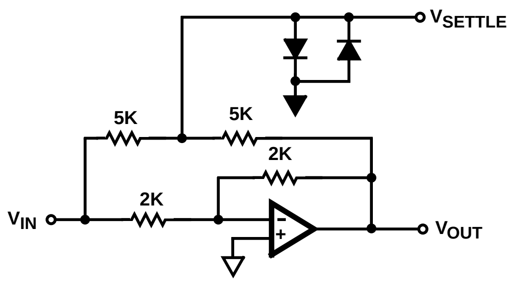
V_{OUT} = 2.5V
Vertical Scale = 2V/Div.,
Horizontal Scale = 200ns/Div.

FIGURE 2. LARGE SIGNAL RESPONSE



V_{OUT} = ±100mV
Vertical Scale = 100mV/Div.,
Horizontal Scale = 200ns/Div.

FIGURE 3. SMALL SIGNAL RESPONSE



NOTES:

12. A_V = -1.
13. Feedback and summing resistors must be matched (0.1%).
14. HP5082-2810 clipping diodes recommended.
15. Tektronix P6201 FET probe used at settling point.

FIGURE 4. SETTLING TIME TEST CIRCUIT

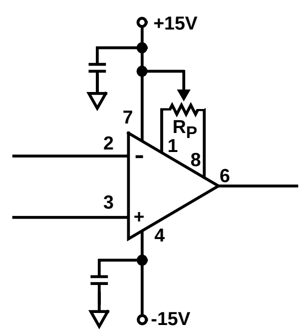
Application Information

Operation at Various Supply Voltages

The HA-5221 operates over a wide range of supply voltages with little variation in performance. The supplies may be varied from ±5V to ±15V. See typical performance curves for variations in supply current, slew rate and output voltage swing.

Offset Adjustment

The following diagram shows the offset voltage adjustment configuration for the HA-5221. By moving the potentiometer wiper towards pin 8 (+BAL), the op amps output voltage will increase; towards pin 1 (-BAL) decreases the output voltage. A 20kΩ trim pot will allow an offset voltage adjustment of about 10mV.



Capacitive Loading Considerations

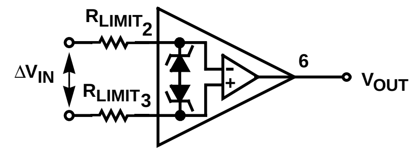
When driving capacitive loads >80pF, a small resistor, 50Ω to 100Ω, should be connected in series with the output and inside the feedback loop.

Saturation Recovery

When an op amp is over driven, output devices can saturate and sometimes take a long time to recover. By clamping the input, output saturation can be avoided. If output saturation can not be avoided, the maximum recovery time when overdriven into the positive rail is 10.6µs. When driven into the negative rail the maximum recovery time is 3.8µs.

Input Protection

The HA-5221 has built in back-to-back protection diodes which limit the maximum allowable differential input voltage to approximately 5V. If the HA-5221 is used in circuits where the maximum differential voltage may be exceeded, then current limiting resistors must be used. The input current should be limited to a maximum of 10mA.



PC Board Layout Guidelines

When designing with the HA-5221, good high frequency (RF) techniques should be used when building a PC board. Use of ground plane is recommended. Power supply decoupling is very important. A 0.01µF to 0.1µF high quality ceramic capacitor at each power supply pin with a 2.2µF to 10µF tantalum close by will provide excellent decoupling. Chip capacitors produce the best results due to ease of placement next to the op amp and basically no lead inductance. If leaded capacitors are used, the leads should be kept as short as possible to minimize lead inductance.

Typical Performance Curves $V_S = \pm 15V$, $T_A = 25^oC$

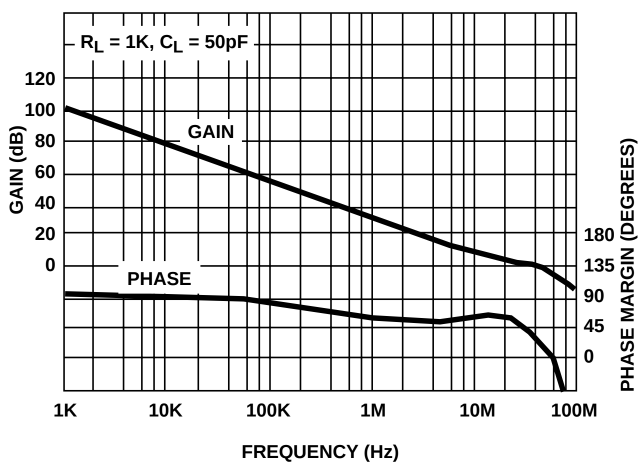


FIGURE 5. OPEN LOOP GAIN AND PHASE vs FREQUENCY

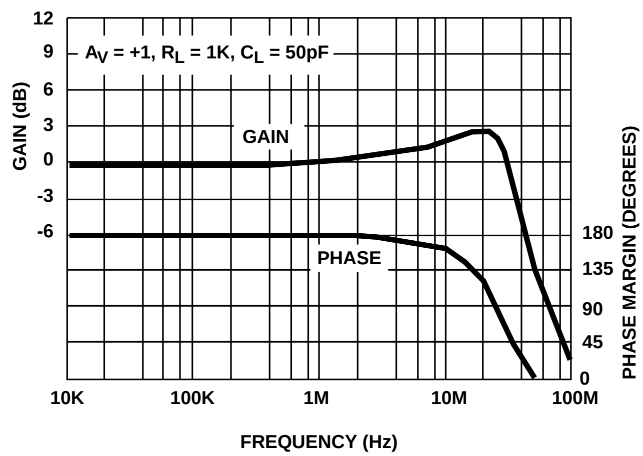


FIGURE 6. CLOSED LOOP GAIN vs FREQUENCY

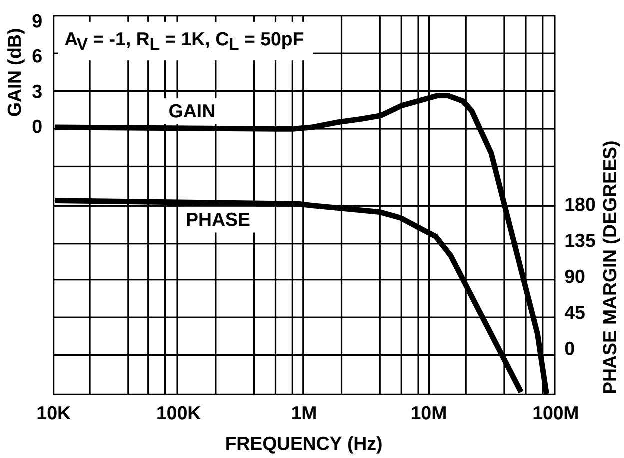


FIGURE 7. CLOSED LOOP GAIN vs FREQUENCY

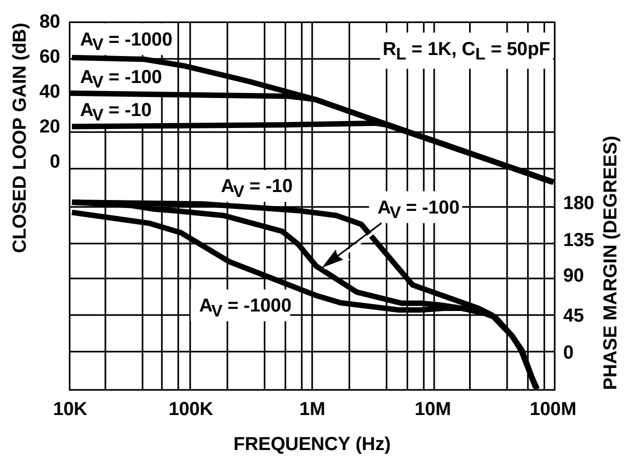


FIGURE 8. VARIOUS CLOSED LOOP GAINS vs FREQUENCY

Typical Performance Curves $V_S = \pm15V$, $T_A = 25^oC$ **(Continued)**

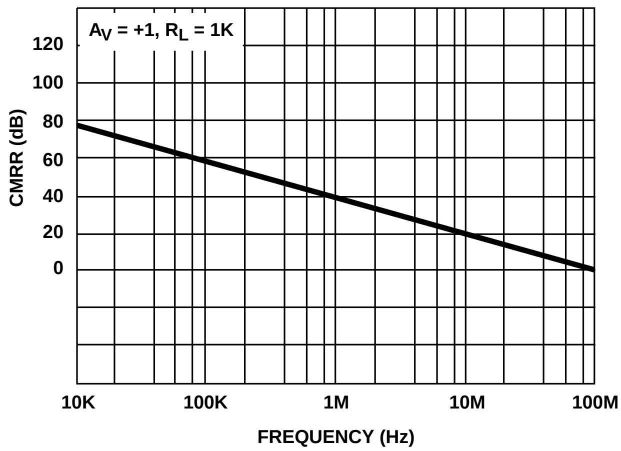


FIGURE 9. CMRR vs FREQUENCY

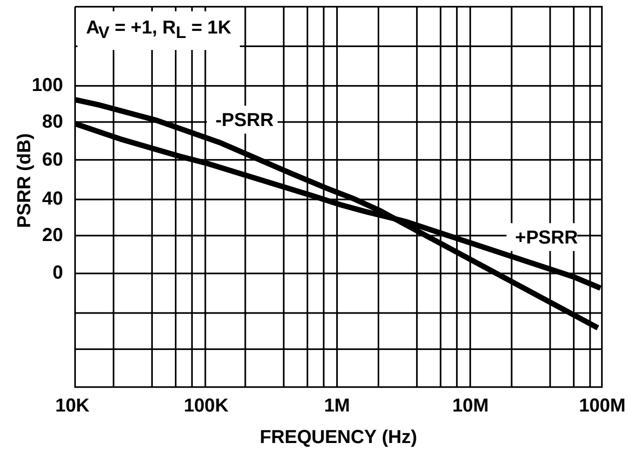


FIGURE 10. PSRR vs FREQUENCY

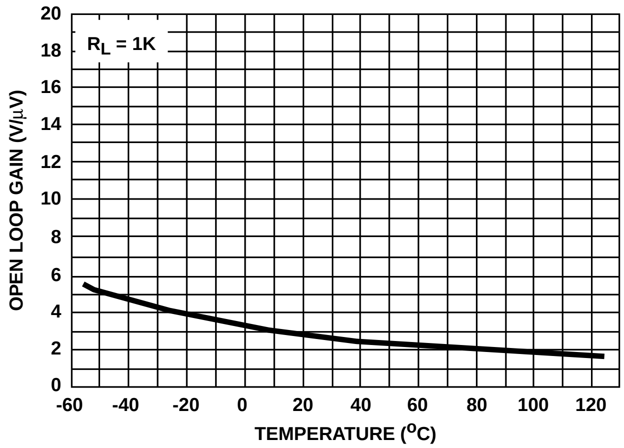


FIGURE 11. OPEN LOOP GAIN vs TEMPERATURE

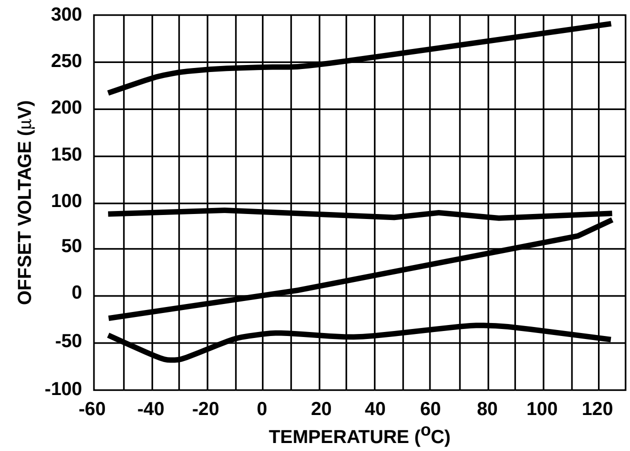


FIGURE 12. OFFSET VOLTAGE vs TEMPERATURE (4 REPRESENTATIVE UNITS)

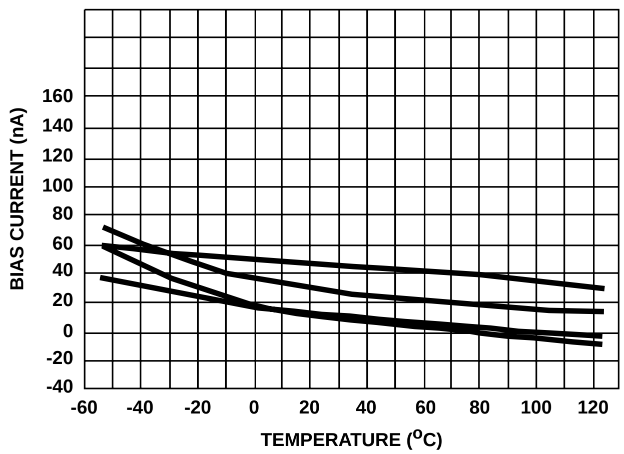


FIGURE 13. BIAS CURRENT vs TEMPERATURE (4 REPRESENTATIVE UNITS)

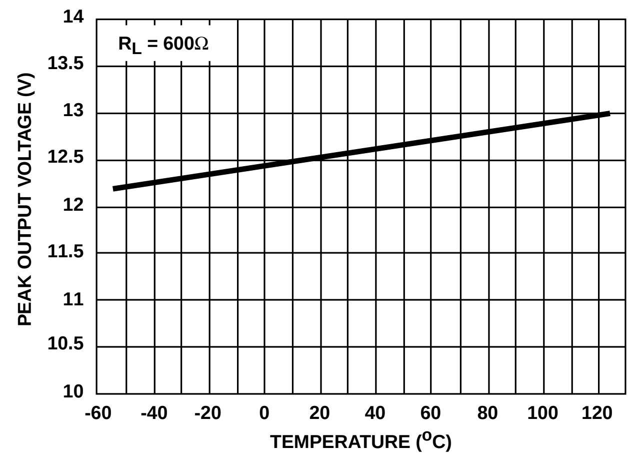


FIGURE 14. OUTPUT VOLTAGE SWING vs TEMPERATURE

Typical Performance Curves $V_S = \pm15V$, $T_A = 25^oC$ **(Continued)**

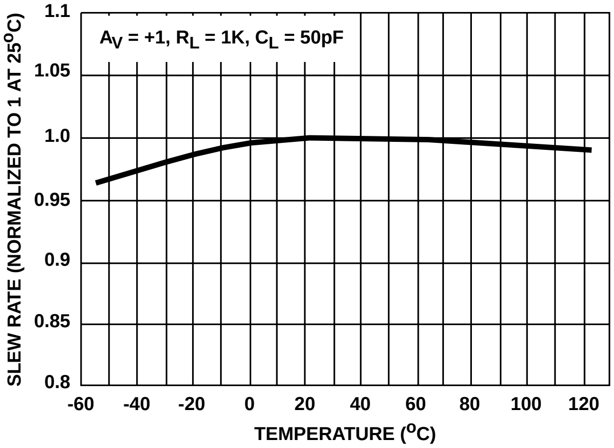


FIGURE 15. SLEW RATE vs TEMPERATURE

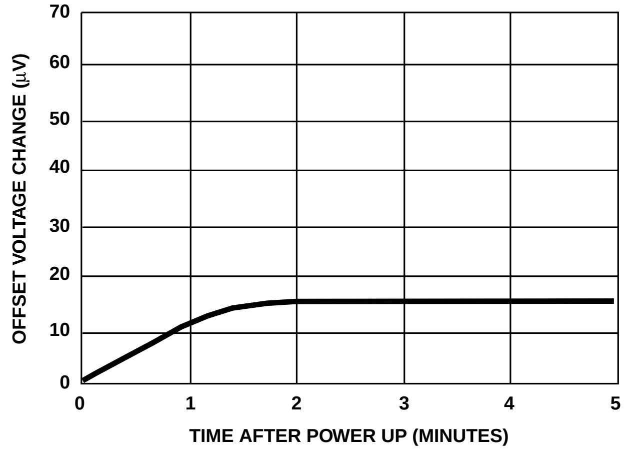


FIGURE 16. OFFSET VOLTAGE WARM-UP DRIFT (CERDIP PACKAGES)

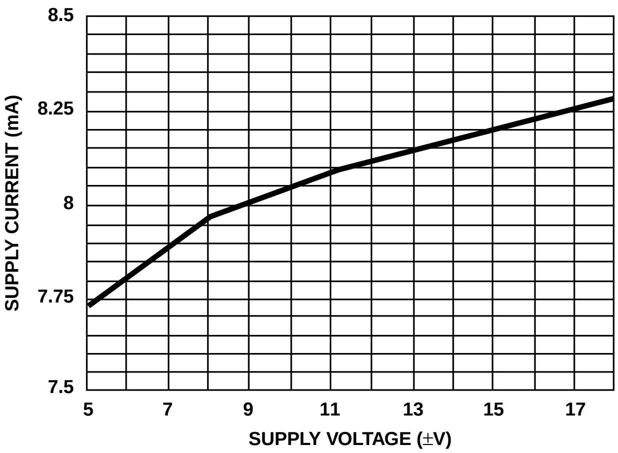


FIGURE 17. SUPPLY CURRENT vs SUPPLY VOLTAGE

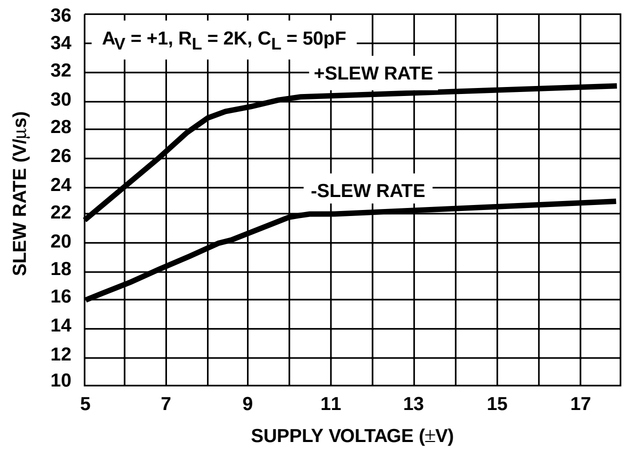


FIGURE 18. SLEW RATE vs SUPPLY VOLTAGE

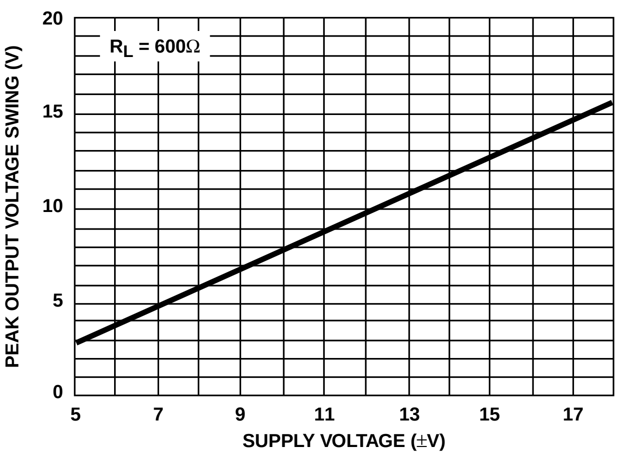


FIGURE 19. OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE

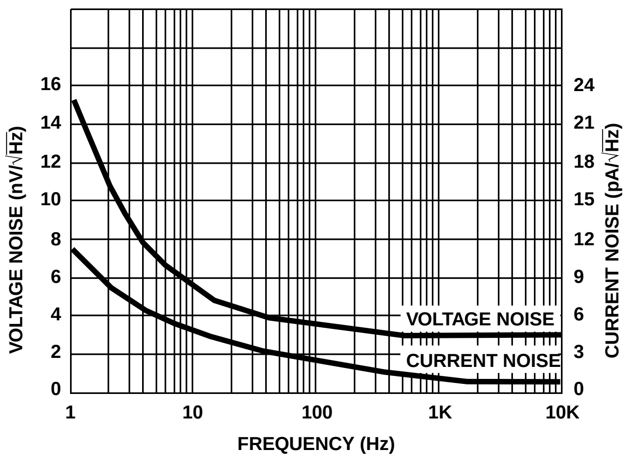


FIGURE 20. NOISE CHARACTERISTICS

Typical Performance Curves $V_S = \pm15V$, $T_A = 25^oC$ **(Continued)**

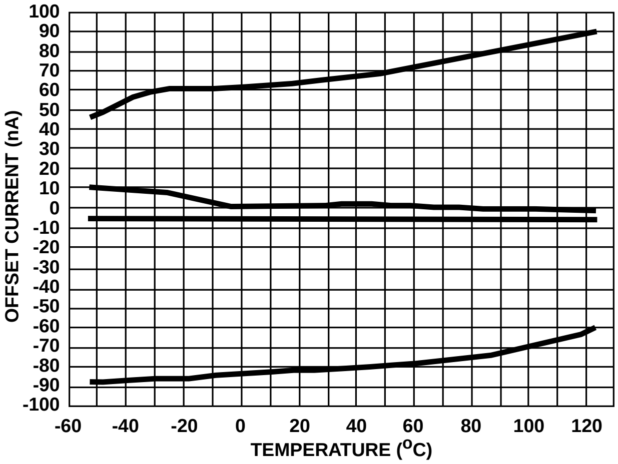


FIGURE 21. OFFSET CURRENT vs TEMPERATURE (4 REPRESENTATIVE UNITS)

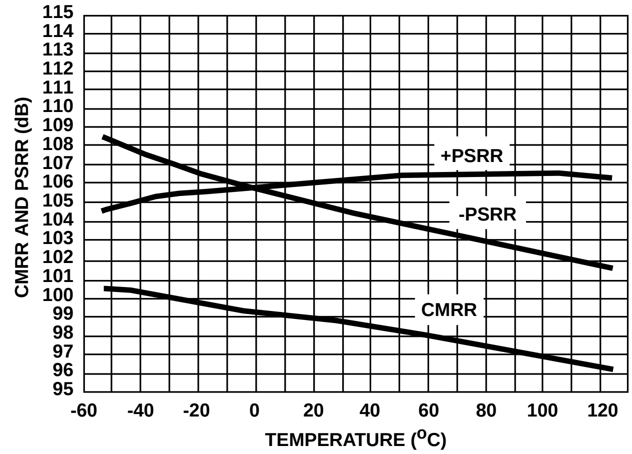


FIGURE 22. CMRR AND PSRR vs TEMPERATURE

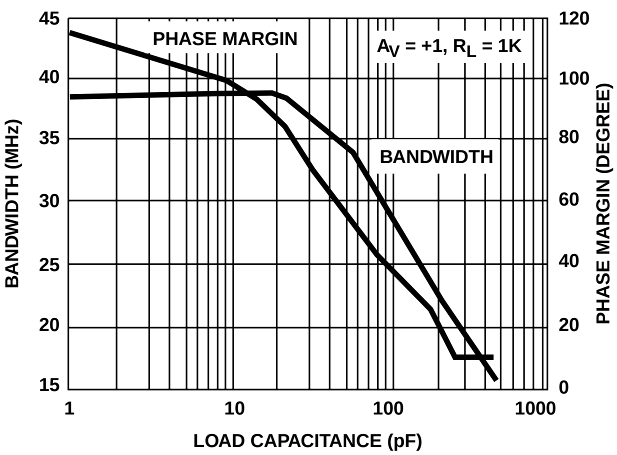


FIGURE 23. BANDWIDTH AND PHASE MARGIN vs LOAD CAPACITANCE

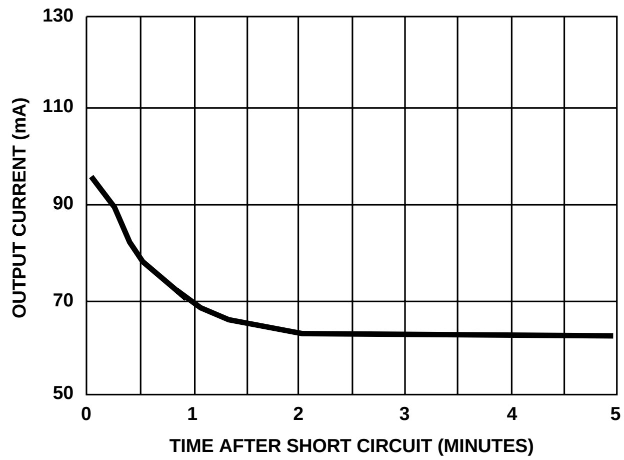
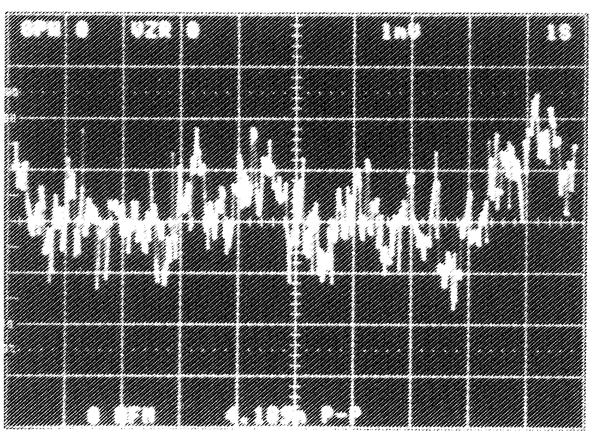
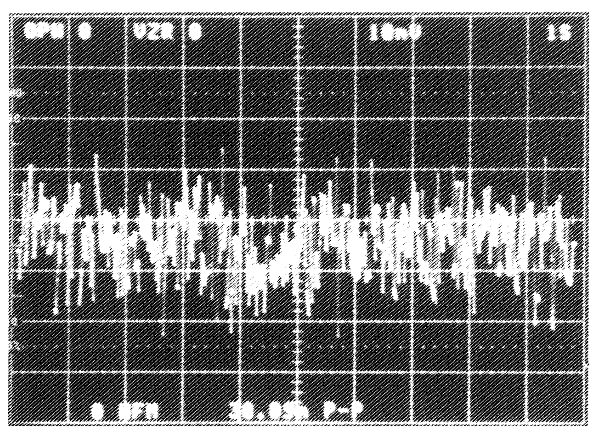


FIGURE 24. SHORT CIRCUIT OUTPUT CURRENT vs TIME



Vertical Scale = 1mV/Div.; Horizontal Scale = 1s/Div.
$A_V = +25{,}000$; $E_N = 0.168\mu V_{P\text{-}P}$ RTI

FIGURE 25. 0.1Hz TO 10Hz NOISE



Vertical Scale = 10mV/Div.; Horizontal Scale = 1s/Div.
$A_V = +25{,}000$; $E_N = 1.5\mu V_{P\text{-}P}$ RTI

FIGURE 26. 0.1Hz TO 1MHz

Typical Performance Curves $V_S = \pm15V$, $T_A = 25^oC$ **(Continued)**

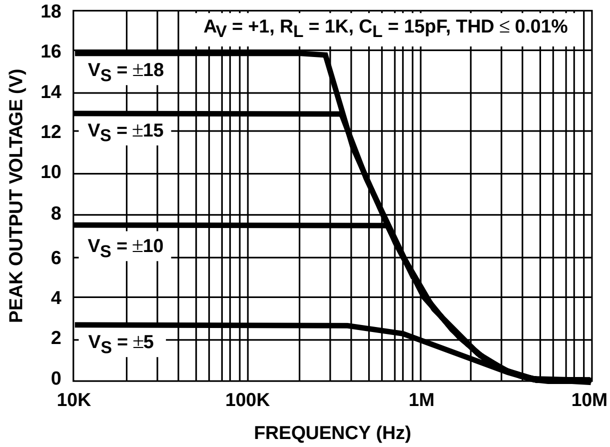


FIGURE 27. OUTPUT VOLTAGE SWING vs FREQUENCY

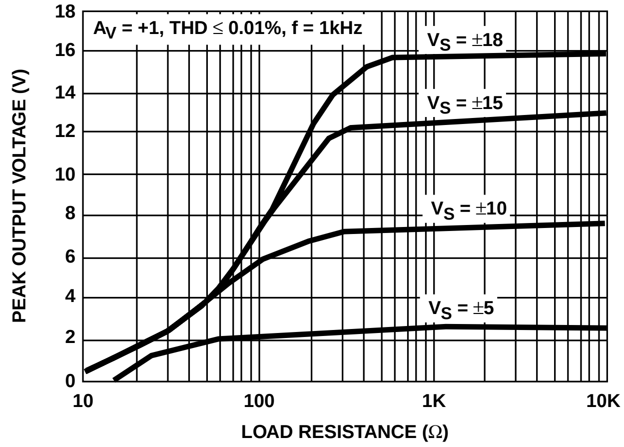


FIGURE 28. OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

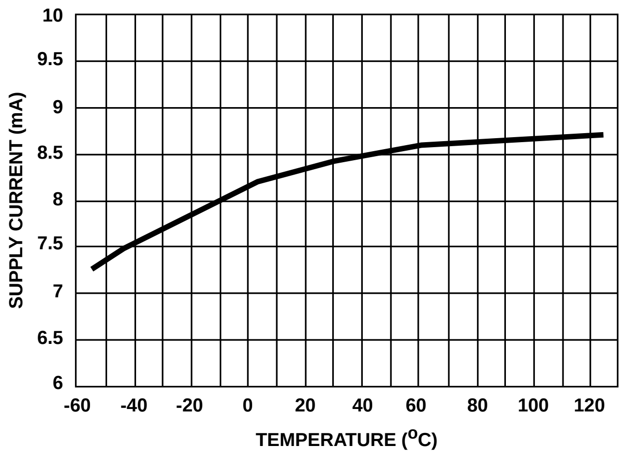


FIGURE 29. SUPPLY CURRENT vs TEMPERATURE

Die Characteristics

DIE DIMENSIONS:

72 mils x 94 mils
1840µm x 2400µm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

SUBSTRATE POTENTIAL (POWERED UP):

V-

TRANSISTOR COUNT:

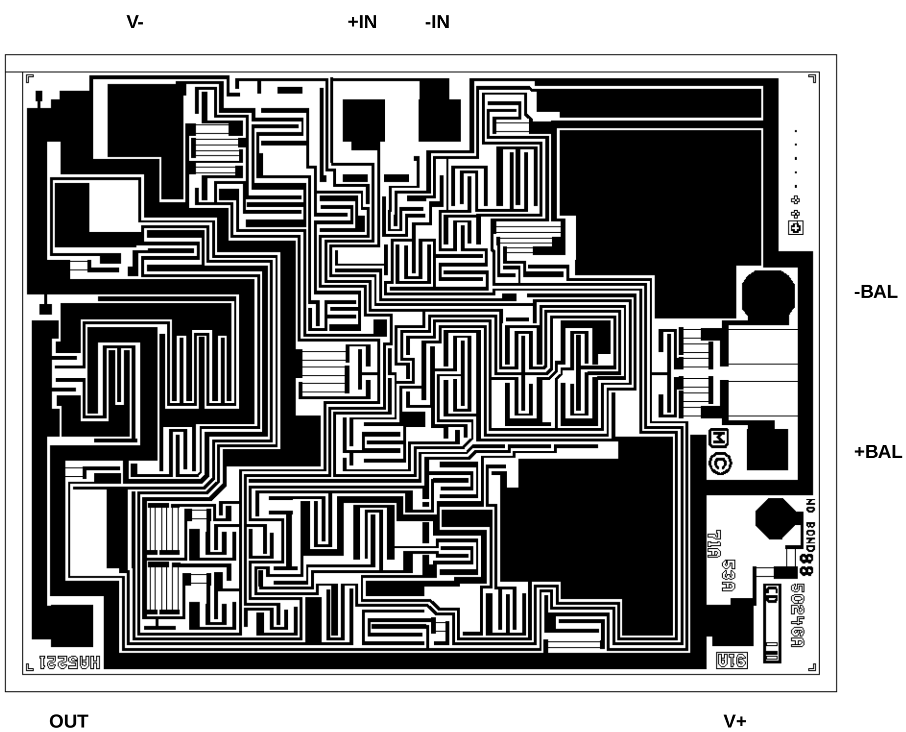
62

PROCESS:

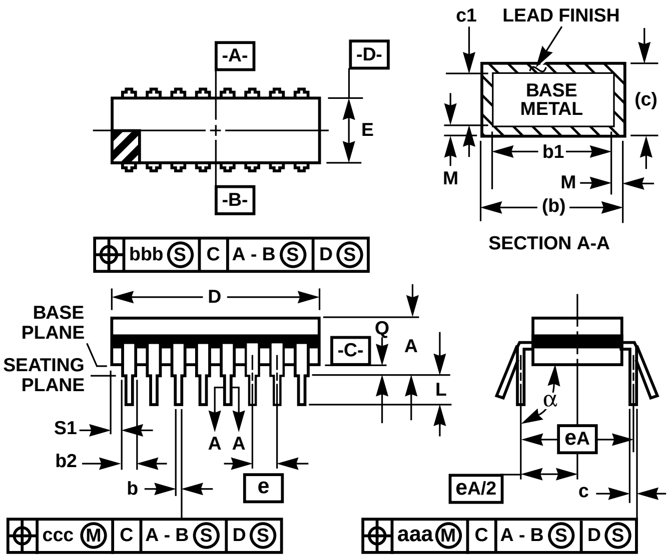
Bipolar Dielectric Isolation

Metallization Mask Layout

HA-5221



Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

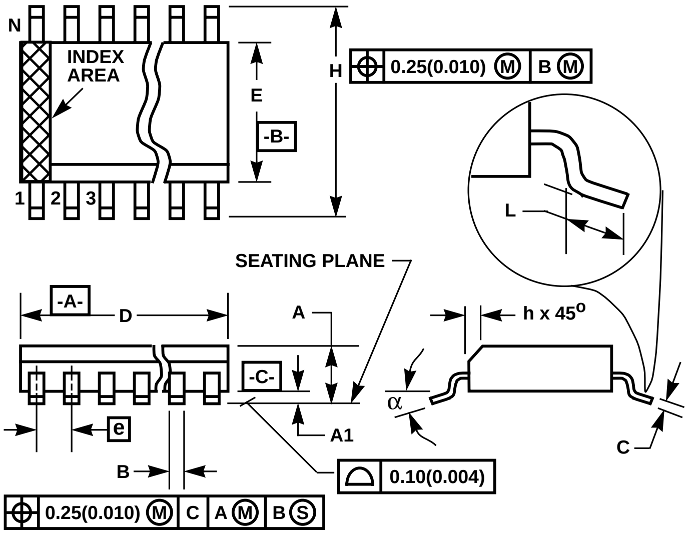
1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH

F8.3A MIL-STD-1835 GDIP1-T8 (D-4, CONFIGURATION A)
8 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.405	-	10.29	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	8		8		8

Rev. 0 4/94

Small Outline Plastic Packages (SOIC)



M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

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NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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