Quad, 235 MHz, DC Coupled VGA and Differential Output Amplifier

Preliminary Technical Data

AD8264

FEATURES

Low Noise
- **Voltage noise = 2.3 nV/√Hz**
- **Current noise = 5 pA/√Hz**

Wide Bandwidth
- **Small Signal: 235 MHz (VGAx); 80 MHz (Diff. Amp Out)**
- **Large Signal: 80 MHz (1Vp-p)**

Gain Range:
- **0 to +24 dB (Input to VGA Output)**
- **+6 to +30 dB (Input to Differential Output)**

Gain Scaling
- **20 dB/V**

DC Coupled

Single Ended Input and Differential Output

Supplies: ±2.5V to ±5V

Low power: 125 mW per channel @ ±3.3V

APPLICATIONS

Multi-Channel Data Acquisition
Positron Emission Tomography
Gain Trim
Industrial and Medical Ultrasound
Radar Receivers

FUNCTIONAL BLOCK DIAGRAM

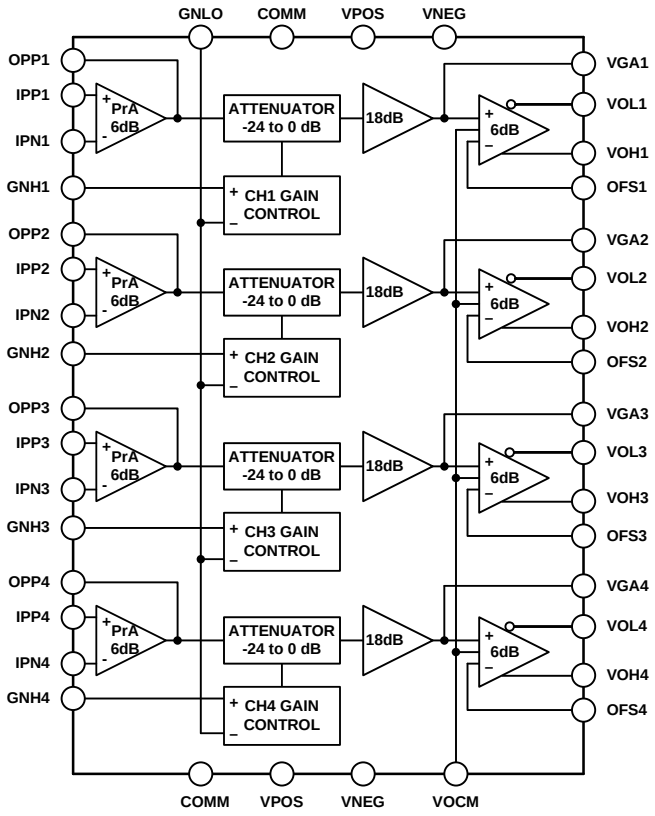

Figure 1.

GENERAL DESCRIPTION

The AD8264 is a four-channel linear-in-dB, general-purpose variable gain amplifier with a high-impedance pre-amplifier, and a flexible differential output buffer.

Each channel includes a single-ended preamp/VGA section to preserve the wide bandwidth and fast slew rate for low-distortion pulse applications. A 6dB differential output buffer with common-mode and offset adjustments enable direct coupling to most modern high-speed analog to digital converters, using the converter reference output for perfect dc matching levels.

The –3dB bandwidth of the preamp/VGA is DC to 235 MHz, the bandwidth of the differential driver is 80 MHz. Intended for a broad range of applications, DC coupling combined with wide bandwidth make this amplifier a very good pulse processor. The floating gain-control interface provides a precise linear-in-dB scale of 20 dB/V and is easy to interface to a variety of external circuits. The gain of each channel is adjusted independently, and all channels are referenced to a single pin GNLO. Combined with a multi-output digital–analog converter, each section of the AD8264 may be used for active calibration, or as a trim amplifier.

The gain range of the VGA sections is 24 dB. Operation from a dual polarity power supply enables amplification of negative voltage pulses that are generated by current-sinking pulses into a grounded load, such as is typically done with photodiodes or photo-multiplier tubes (PMT). Delay-free processing of wide-band video signals is also possible. The differential output amplifier permits convenient level shifting and interfacing to single–supply ADC's using the VOCM and OFSx pins. The AD8264 is available in a 40-lead, 6 mm x 6 mm LFCSP with an operating temperature range of –40°C to +85°.

Rev. PrA

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SPECIFICATIONS

V_S = ±2.5 V, T_A = 25°C, Gain Range = +6 to +30 dB, V_{GAIN} = (V_{GNHx} - V_{GNLO}), V_{OCM} = GND, V_{OFS} = GND, f = 10 MHz, C_L = 5 pF, R_L = 500 Ω per output (VGAx, VOHx, VOLx), unless otherwise specified.

Table 1.

Parameter	Conditions	Min	Typ (BOLD = Measured)	Max	Unit
GENERAL PARAMETERS					
–3 dB Small Signal Bandwidth (VGAx)	V_{OUT} = 10 mV p-p, V_{GAIN} = 0 V		**235**		MHz
–3 dB Large Signal Bandwidth (VGAx)	V_{OUT} = 1 V p-p, V_{GAIN} = 0 V		**150**		MHz
–3 dB Small Signal Bandwidth (Diff Out)	V_{OUT} = 100 mV p-p		**80**		MHz
–3 dB Large Signal Bandwidth (Diff Out)	V_{OUT} = 2 V p-p		**80**		MHz
Slew Rate	VGAx, V_{OUT} = 2 V p-p		**380**		V/µs
	VGAx, V_{OUT} = 1 V p-p		**290**		V/µs
	Diff Out, V_{OUT} = 2 V p-p		**470**		V/µs
	Diff Out, V_{OUT} = 1 V p-p		**220**		V/µs
Input Bias Current	Pins IPPx		-2.5		µA
Input Resistance	Pins IPPx at DC; $\Delta V_{IN}/\Delta I_{BIAS}$		5.2		MΩ
Input Capacitance	Pins IPPx		0.8		pF
Input Impedance	Pins IPPx at 10 MHz		15.7		kΩ
Input Voltage Noise			**2.3**		nV/√Hz
Input Current Noise			5		pA/√Hz
Noise Figure (Diff Out)	V_{GAIN} = 0.7 V, R_S = 50 Ω, unterminated		**9**		dB
Output-Referred Noise (Diff Out)	V_{GAIN} = 0.7 V (Gain = +30 dB)		**72**		nV/√Hz
	V_{GAIN} = -0.7 (Gain = +6 dB)		**45**		nV/√Hz
Output Impedance	VGAx, DC to 10 MHz		**3.5**		Ω
	Diff Out, DC to 10 MHz		**<1**		Ω
Output Signal Range	Preamp		$\|V_S\|$ - 1.3		V
	VGA, $R_L \geq$ 500 Ω		$\|V_S\|$ - 1.3		V
	Diff Amp, $R_L \geq$ 500 Ω per side		$\|V_S\|$ - 0.5		V
Output Offset Voltage	Preamp Offset		|<10|		mV
	VGAx Offset, V_{GAIN} = 0.7 V		|<10|		mV
	Diff Out Offset, V_{GAIN} = 0.7 V		|<10|		mV
DYNAMIC PERFORMANCE					
Harmonic Distortion	V_{GAIN} = 0V, VGAx = 1 Vpp, Diff Out = 2Vpp (Measured @ VGAx)				
HD2	f = 1 MHz		-81		dBc
HD3			-67		dBc
HD2	f = 10 MHz		-65		dBc
HD3			-61		dBc
HD2	f = 35 MHz		-56		dBc
HD3			-72		dBc
	V_{GAIN} = 0V, VGAx = 0.5Vpp, Diff Out = 1Vpp (Measured @ Diff Out)				
HD2	f = 1 MHz		-86		dBc
HD3			-78		dBc
HD2	f = 10 MHz		-66		dBc
HD3			-53		dBc
HD2	f = 35 MHz		-50		dBc
HD3			-33		dBc
Input 1 dB Compression Point	V_{GAIN} = -0.7 V, f = 10 MHz		13		dBm[1]

[1] All dBm values are calculated with 50 Ω reference, unless otherwise noted.

Parameter	Conditions	Min	Typ (BOLD = Measured)	Max	Unit
	V_{GAIN} = +0.7 V, f = 10 MHz		-11		dBm
Two-Tone Intermodulation Distortion (IMD3)	V_{GAIN} = 0, VGAx =1Vpp, f_1 = 10 MHz, f_2 = 11 MHz		-68		dBc
	V_{GAIN} = 0, VGAx =1Vpp, f_1 = 35 MHz, f_2 = 36 MHz		-56		dBc
	V_{GAIN} = 0, V_{OUT} = 2 Vpp, f_1 = 10 MHz, f_2 = 11 MHz		-45		dBc
	V_{GAIN} = 0, V_{OUT} = 2 Vpp, f_1 = 35 MHz, f_2 = 36 MHz		-36		dBc
Output Third Order Intercept	V_{GAIN} = 0, VGAx = 1 Vpp, f = 10 MHz		32		dBm
	V_{GAIN} = 0, VGAx = 1 Vpp, f = 35 MHz		26		dBm
	V_{GAIN} = 0, V_{OUT} = 2 Vpp, f = 10 MHz		27		dBm
	V_{GAIN} = 0, V_{OUT} = 2 Vpp, f = 35 MHz		22		dBm
Overload Recovery	V_{GAIN} = 0.7 V, V_{IN} stepped from 0.1 Vpp to 1Vpp		25		ns
Group Delay Variation	1 MHz < f < 100 MHz, Full Gain Range		±1		ns
ACCURACY					
Absolute Gain Error[1]	-0.7 V < V_{GAIN} < -0.6 V	**0.1**	**+0.2 to +1.8**	**+2**	dB
	-0.6 V < V_{GAIN} < -0.5 V	**-0.1**	**±0.2**	**+0.3**	dB
	-0.5 V < V_{GAIN} < 0.5 V	**-0.2**	**±0.2**	**+0.3**	dB
	0.5 V < V_{GAIN} < 0.6 V	**-0.5**	**±0.2**	**+0.3**	dB
	0.6 V < V_{GAIN} < 0.7 V	**-2**	**-0.4 to -2**	**-0.1**	dB
Gain Law Conformance[2]	-0.5 V < V_{GAIN} < 0.5 V, ±2.5 ≤ V_S ≤ ±5V		±0.2		dB
	-0.5 V < V_{GAIN} < 0.5 V, -40°C ≤ T ≤ 105°C		**±0.3**		dB
Channel-to-Channel Matching	single IC ; -0.5 V < V_{GAIN} < 0.5 V; -40°C ≤ T ≤ 105°C		**±0.3**		dB
	multiple ICs ; -0.5 V < V_{GAIN} < 0.5 V; -40°C ≤ T ≤ 105°C		TBD		dB
GAIN CONTROL INTERFACE					
Gain Scaling Factor	-40°C ≤ T ≤ 105°C	**19.8**	**19.9**	**20.1**	dB/V
Gain Range			24		dB
Intercept	Vgain = 0 V; Gain at VGAx; -40°C ≤ T ≤ 105°C	**11.8**	**11.9**	**12.0**	dB
	Vgain = 0 V; Gain at differential output; -40°C ≤ T ≤ 105°C	**17.8**	**17.9**	**18.0**	dB
Input Voltage (GNHx) Range	No foldover; GNLO=0V	$-V_S$		$+V_S$	V
Input Resistance	Measured via change in bias current over -0.7 V < V_{GAIN} < 0.7 V		70		MΩ
Bias Current	GNHx pins, -0.7 V < V_{GAIN} < 0.7 V, -40°C ≤ T ≤ 105°C	-0.4	-0.3	-0.2	µA
	GNLO pin, -0.7 V < V_{GAIN} < 0.7 V, -40°C ≤ T ≤ 105°C	-1.6	-1.2	-0.8	µA
Response Time	24 dB Gain Change		300		ns
OUTPUT BUFFER					
Bias Current	VOCM pin, -40°C ≤ T ≤ 105°C	-80	-140	-190	nA
	OFSx pins, -40°C ≤ T ≤ 105°C				µA
Input Voltage Range	VOCM pin				V
	OFSx pins ; VGAx pins = 0 V				V

[1] *Conformance to theoretical gain expression (see Equation 1*

$$Gain = 20\frac{dB}{V} \cdot V_{GAIN} + ICPT$$

Equation 2

).

[2] Conformance to best fit dB linear curve.

Parameter	Conditions	Min	Typ (BOLD = Measured)	Max	Unit
Gain	VGAx pins to differential output (VOHx – VOLx); -40°C ≤ T ≤ 105°C		6		dB
POWER SUPPLY					
Supply Voltage		±2.5		±5	V
	Vs = ± 2.5 V				
Quiescent Current	-40°C ≤ T ≤ 105°C	TBD	**79**	TBD	mA
Power Dissipation			**395**		mW
	Vs = ± 3.3 V				
Quiescent Current	-40°C ≤ T ≤ 105°C	TBD	**85**	TBD	mA
Power Dissipation			**560**		mW
	Vs = ± 5 V[1]				
Quiescent Current	-40°C ≤ T ≤ ***85 °C***	TBD	**99**	TBD	mA
Power Dissipation			**990**		mW
PSRR	From VPOS to Diff Out, V_{GAIN} = 0.7 V, f = 10 MHz		-15		dB
	From VNEG to Diff Out, V_{GAIN} = 0.7 V, f = 10 MHz		-25		dB

[1] For >±3.3 V supplies, the temperature range is limited to -40°C ≤ T ≤ 85°C.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Voltage	
Supply Voltage (VPOS, VNEG)	±6V
Input Voltage (INPx)	VPOS, VNEG
GAIN Voltage (GNHx, GNLO)	VPOS, VNEG
Power Dissipation	TBD W
Temperature	
Operating Temperature	–40°C to +85°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering 60 sec)	300°C
Package Glass Transition Temperature (T_G)	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. The θ_{JA} values in Table 3 assume a 4-layer JEDEC standard board with zero airflow.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
40-Lead LFCSP[1]	31.0	2.3	°C/W

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation for the AD8264 is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the properties of the plastic change. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the amplifiers. Exceeding a temperature of 150°C for an extended period of time can cause changes in silicon devices, potentially resulting in a loss of functionality.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

[1] Four-Layer JEDEC Board (2S2P).

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

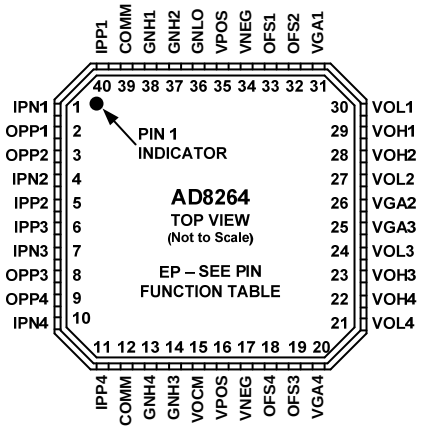

Figure 2. 40-Lead LFCSP

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
0 (EP), 12, 39	COMM	Ground – Exposed Paddle (Pin 0) needs an electrical connection to ground. For proper RF grounding and increased reliability the pad must be connected to the ground plane.
1, 4, 7, 10	IPNx	Negative Preamp Inputs for CH1 through 4 – Normally no external connection.
2, 3, 8, 9	OPPx	Preamp Output for CH1 through 4 – Internally connected to attenuator (VGA) input, normally no external connection.
5, 6, 11, 40	IPPx	Positive Preamp Input for CH1 through 4 – High Impedance.
13, 14, 37, 38	GNHx	Positive Gain Control Voltage Input for CH1 through 4; referenced to GNLO (pin 36).
15	VOCM	Sets Differential Output Amplifier (VOHx and VOLx) Common-Mode Voltage.
16, 35	VPOS	Positive Supply (Internally tied together)
17, 34	VNEG	Negative Supply (Internally tied together)
18, 19, 32, 33	OFSx	Voltage sets Differential Output Offset for CH1 through 4. This is the non-inverting input to the differential amp and has the same bandwidth as the inverting input (VGAx).
20, 25, 26, 31	VGAx	VGA Output for CH1 through 4
21, 24, 27, 30	VOLx	Negative Differential Amplifier Output for CH1 through 4
22, 23, 28, 29	VOHx	Positive Differential Amplifier Output for CH1 through 4
36	GNLO	Negative Gain Control Input (Reference for GNHx pins)

THEORY OF OPERATION

OVERVIEW

The AD8264 is a DC coupled quad channel VGA with a fixed gain-of-2 (6 dB) preamplifier, and a single-ended to differential amplifier with level shift capability that can be used as an ADC driver. Figure 3 shows a representative block diagram of a single channel; all four channels are identical. The supply can operate from ±2.5 V to ±5 V. The primary application is as a pulse processor for medical PET (Positron Emission Tomography) imaging; however, the part is useful for any DC coupled application.

The signal chain consists of three fundamental stages: the preamplifier, the variable gain amplifier, and the differential output buffer amplifier. The preamplifier has an internally fixed gain-of-2 (6 dB). The VGA is comprised of an attenuator that provides 0 to 24 dB of attenuation, followed by a fixed gain 18 dB (8×) amplifier. The single-ended VGA output is connected directly to the non-inverting input of the differential output (post) amplifier, which has a differential fixed gain-of-2 (6dB).

The gain range from the preamp input to the VGA output is 0 to +24 dB. The gain range from the preamp input to the differential post-amplifier output is +6 dB to +30 dB.

The ideal gain equation for the gain from the single-ended input to output is:

$$V_{GAIN} = V_{GNHx} - V_{GNLO}$$

Equation 1

$$Gain = 20\frac{dB}{V} \cdot V_{GAIN} + ICPT$$

Equation 2

The ideal value for ICPT, or the intercept, is defined at V_{GAIN} = 0V, where V_{GAIN} is defined as $V_{GNHx} - V_{GNLO}$. The ICPT for the VGA output and differential amplifier outputs equals 12.1 dB and 18.1 dB, respectively. The actual intercept will vary with any additional gain or loss along the signal path. The measured values are both about 0.2 dB low.

PREAMP

The preamplifier is a current feedback amplifier, designed to drive the internal 100 Ω gain setting resistors and the resistive attenuator, which together result in a nominal load to the preamplifier of about 113Ω. The negative pre-amp input, IPNx, normally has no external connections. The positive input IPPx is the high impedance input of the current feedback amp. Note that at the largest supply voltage of ±5 V, the input signal can become so large that the preamplifier output cannot deliver the required current to drive the 113 Ω load and therefore limits at 6 Vpp.

The input-referred noise at maximum VGA gain is about 2.3 nV/√Hz and accounts for all the internal amplifiers and gain-setting resistors. When measuring the input-referred noise from the VGA output, the number is slightly lower at 2.1 nV/√Hz because the noise of the post amplifier is not part of the noise calculation.

VGA

The VGA has a voltage feedback architecture and uses analog control to vary the gain. Its low gain range helps to maintain low offset and is intended for gain trim applications. Keeping the gain of each stage relatively low also allows the bandwidth to stay high.

The gain of the VGA is adjusted using the fully differential control inputs, GNHx and GNLO. The GNLO pin is internally connected to all four channels, and must be biased externally. Under typical conditions, the GNLO pin is grounded. The Gain High (GNHx) control pins are independent for each channel. The gain slope is nominally 20 dB/V, and with GNLO connected to ground, each GNHx input can have a voltage applied from VNEG to VPOS without gain foldover.

To make use of the VGA's full gain range, the nominal gain control voltage needed at GNHx is ±0.65 V, relative to the voltage applied to GNLO. At the lowest supply voltage of ±2.5 V, the pin GNLO should always be grounded. With increasing supply, the range of GNLO increases to ±1.2 V at ±3.3 V supplies, and to ±2.8 V at ±5 V supplies.

Table 5. Gain Control Input Range

Supply Voltage	GNLO Voltage Range	V_{GAIN} Range
±5V	±2.8V	±0.65V
±3.3V	±1.2V	±0.65V
±2.5V	0V	±0.65V

For example, at ±3.3 V supplies, one can use a single-supply unipolar DAC like the 10 bit, 4-channel AD5314 together with the ADR318 1.8V reference, bias the GNLO pin at Vref/2 = 0.9 V and drive the GNHx pins directly with the DAC outputs. Since the GNLO pin sources only about 1.2 µA for the 4 channels (~300 nA per channel, the same as for the GNHx pins) a simple resistive divider is generally adequate to set the voltage at the GNLO input.

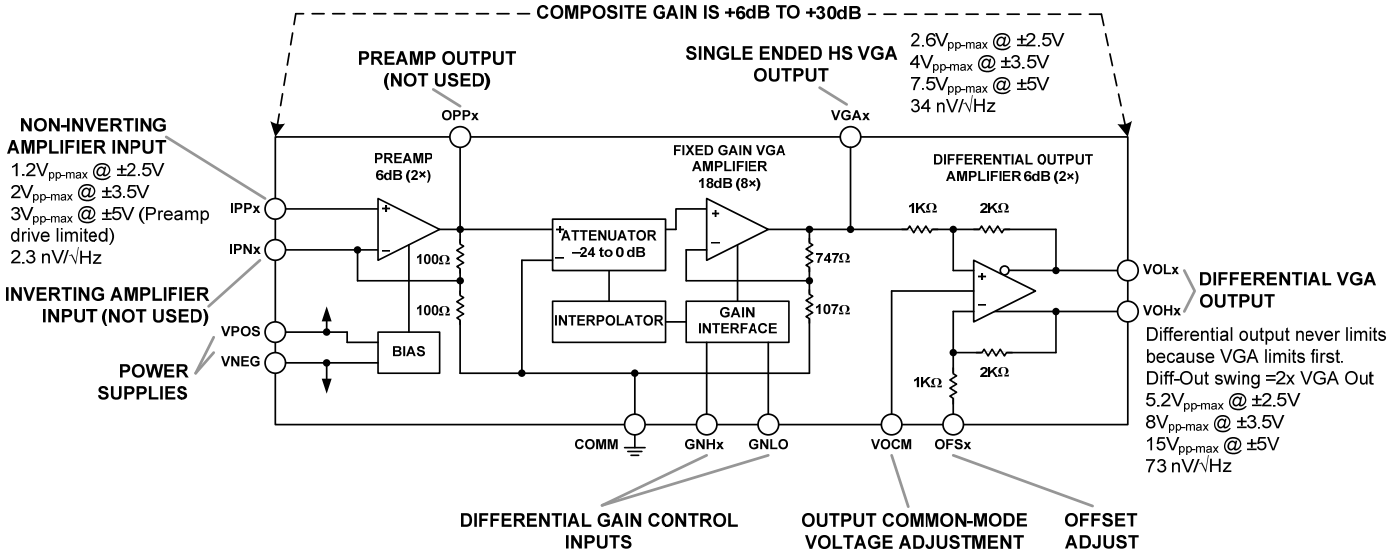

Figure 3. AD8264 Single-Channel Block Diagram

POST AMPLIFIER

From the preamp input to the VGA output (VGAx), the gain is non-inverting. As can be seen in Figure 3, the VGAx pins drive the positive input of the differential amplifier. The gain is inverting from the input of the preamp to the output pin at VOLx, and the gain is non-inverting to the output VOHx.

Other than the input from VGAx, the differential amplifier has two more inputs: VOCM and OFSx. A common VOCM pin is shared among all four post-amplifiers, while separate OFSx pins are provided for each channel.

VOCM Pin

The VOCM pin sets the common-mode voltage of the differential output and it must be biased by an external voltage. In the case of driving a DC coupled ADC, the voltage would typically come from the ADC reference as is shown in the Applications section.

If no DC level shift is necessary, the VOCM pin is connected to ground.

OFSx Pins

The OFSx pins are the inverting inputs of the differential post amplifiers and can be used to pre-bias a differential DC offset at the output. This is very useful when the input is a unipolar pulse, since the user can set up the gain and the offset in such a way as to optimally map a unipolar pulse into the full-scale input of an ADC, while DC coupling throughout.

If no DC offset is desired, then the OFSx pins should be connected to ground. However, it can also be used as a separate input if the user wants this function.

NOISE

At maximum gain, the preamplifier is the primary contributor of noise, and results in a differential output referred noise of roughly 73 nV/√Hz. The noise at the VGAx outputs is 34 nV/√Hz, and because of the gain-of-two, the VGA output noise is amplified by 6 dB to 68 nV/√Hz. The differential amplifier, including the gain setting resistors, contributes another 26 nV/√Hz, and the RMS sum results in a total noise of 73 nV/√Hz. At the lowest gain, the noise at the VGA output is approximately 19 nV/√Hz, and when multiplied by two, results in 38 nV/√Hz at the differential output; again RMS summing this with the 26 nV/√Hz of the differential amplifier causes the total output referred noise to be approximately 46 nV/√Hz.

The input referred noise to the preamplifier at maximum gain is 2.3 nV/√Hz and increases with decreasing gain. Note that all noise numbers include all the necessary gain-setting resistors.

OUTLINE DIMENSIONS

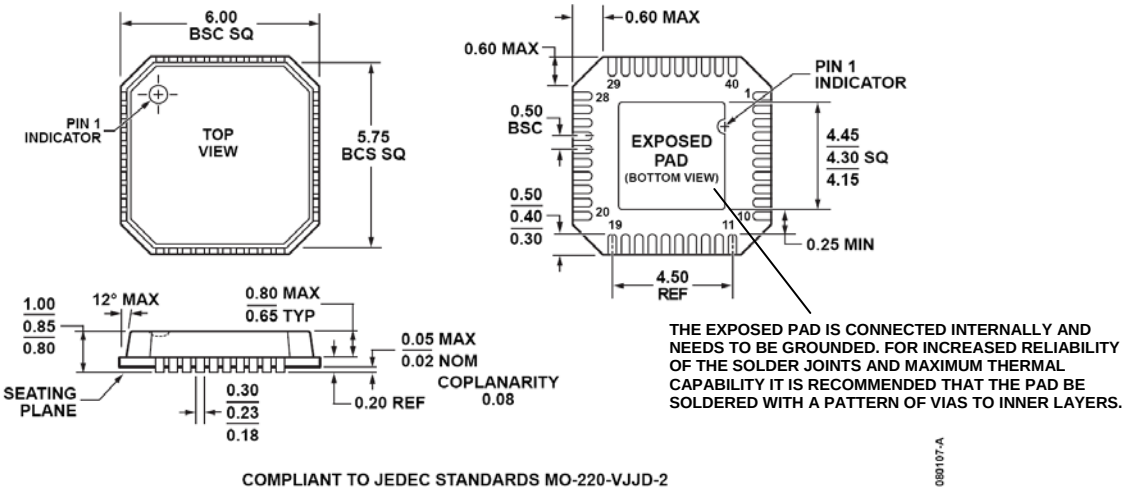

Figure 4. 40-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
6 mm × 6 mm Body, Very Thin Quad
(CP-40-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8264ACPZ[1]	-40°C to +85°C	40-Lead LFCSP	TBD
AD8264ACPZ-R7[1]	-40°C to +85°C	40-Lead LFCSP, 7″Tape and Reel	TBD
AD8264ACPZ-RL[1]	-40°C to +85°C	40-Lead LFCSP, 13″Tape and Reel	TBD

[1] Z = RoHS Compliant Part

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