

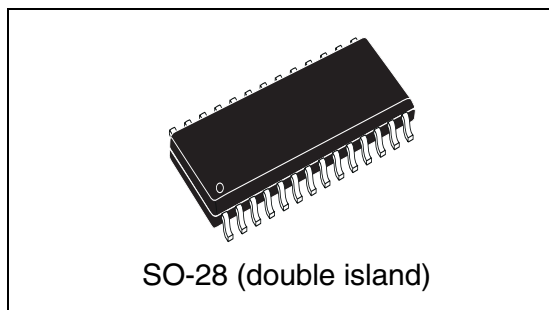
## Quad channel high side driver

### Features

Max supply voltage	$V_{CC}$	36V
Max On-state resistance	$R_{ON}$	$35m\Omega^{(1)}$
Current limitation (typ.)	$I_{LIM}$	25A

1. Per each channel.

- DC short circuit current: 22A
- CMOS compatible inputs
- Proportional load current sense.
- Undervoltage & overvoltage shutdown
- Overvoltage clamp
- Thermal shutdown
- Current limitation
- Very low standby power dissipation
- Protection against:
  - Loss of ground & loss of  $V_{CC}$
- Reverse battery protection <sup>(a)</sup>
- In compliance with the 2002/95/EC european directive



### Description

The VNQ600P-E is a quad HSD formed by assembling two VNQ600P-E chips in the same SO-28 package. The VNQ600P-E is a monolithic device designed in STMicroelectronics VIPower M0-3 Technology. The VNQ600P-E is intended for driving any type of multiple loads with one side connected to ground.

This device has four independent channels and four analog sense outputs which deliver currents proportional to the outputs currents.

Active current limitation combined with thermal shutdown and automatic restart protect the device against overload. Device automatically turns off in case of ground pin disconnection.

a. See [Application schematic on page 17](#)

**Table 1. Device summary**

Package	Order codes	
	Tube	Tape and reel
SO-28 (double island)	VNQ600P-E	VNQ600PTR-E

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# 1 Block diagram and pin description

Figure 1. Block diagram

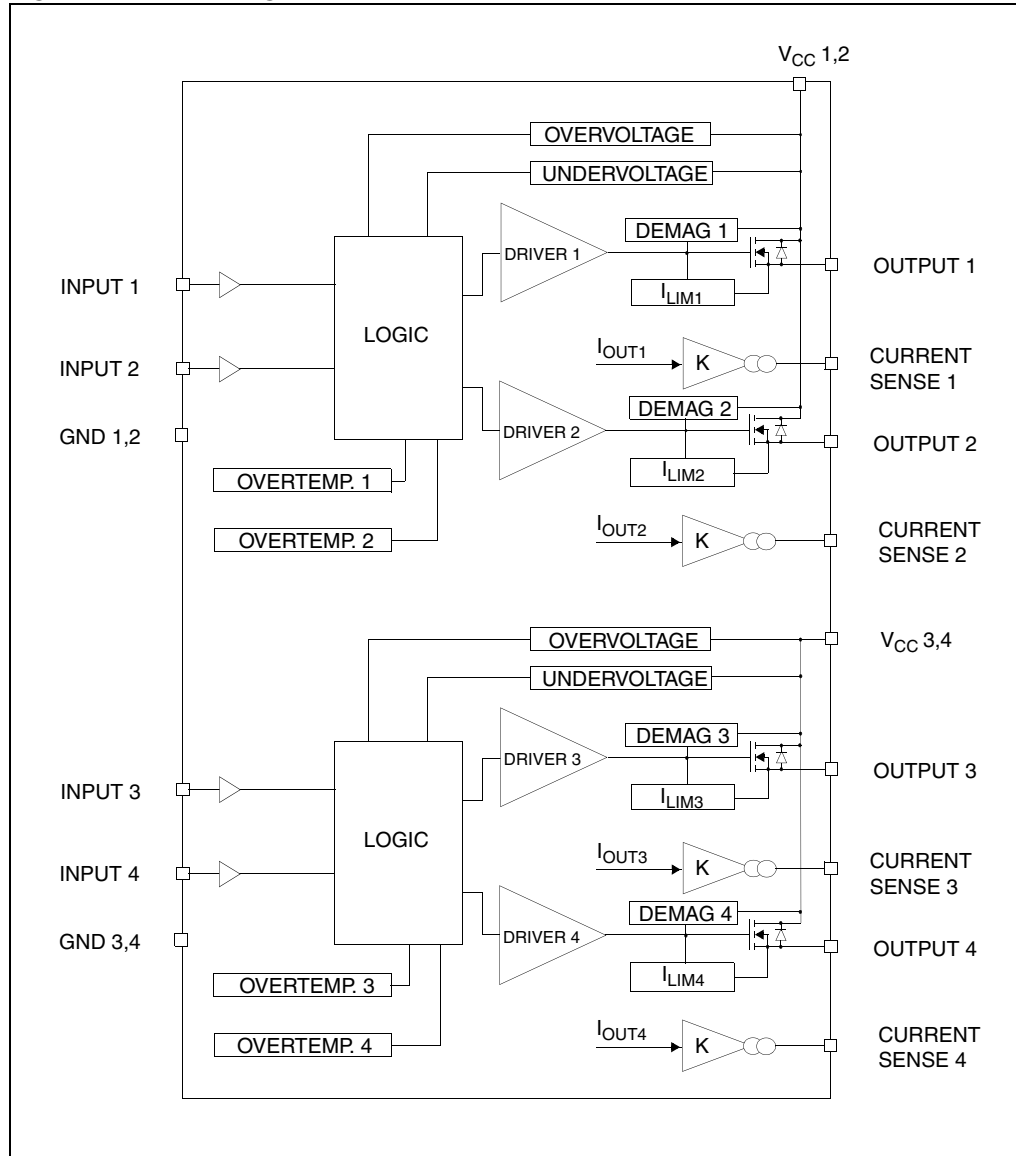


Figure 2. Configuration diagram (top view)

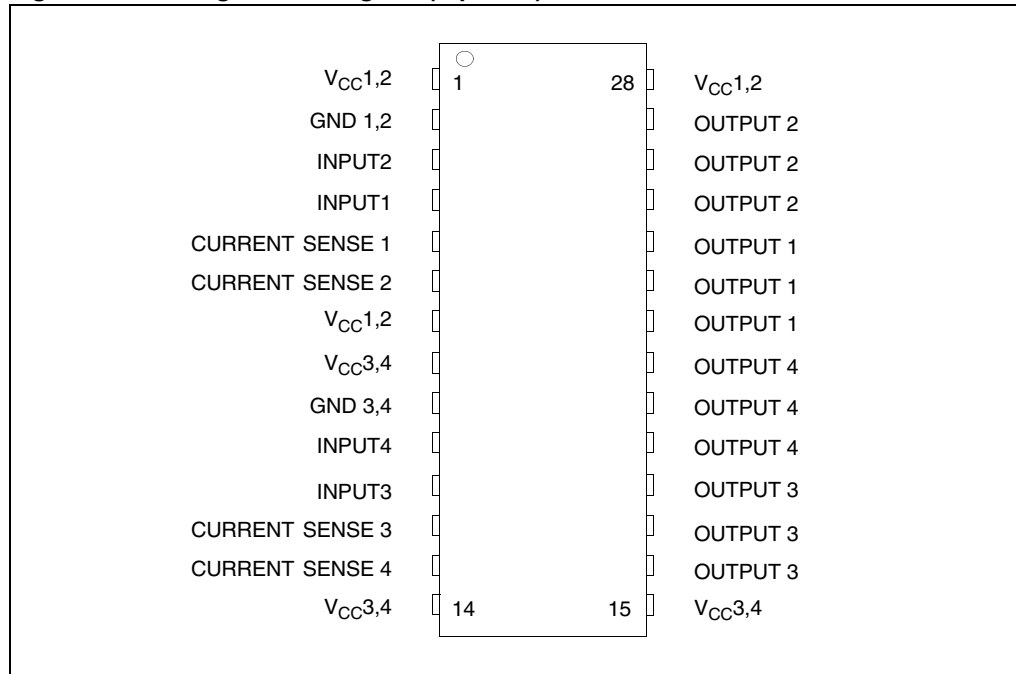


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Current sense	N.C.	Output	Input
Floating		X	X	X
To ground	Through 1KΩ resistor	X		Through 10KΩ resistor

## 2 Electrical specifications

### 2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

**Table 3. Absolute maximum rating**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage (continuous)	41	V
$-V_{CC}$	Reverse supply voltage (continuous)	-0.3	V
$I_{OUT}$	Output current (continuous), for each channel	15	A
$I_R$	Reverse output current (continuous), for each channel	-15	A
$I_{IN}$	Input current	+/- 10	mA
$V_{CSENSE}$	Current sense maximum voltage	-3	V
		+15	V
$I_{GND}$	Ground current at $T_{pins} \leq 25\text{ }^{\circ}\text{C}$ (continuous)	-200	mA
$V_{ESD}$	Electrostatic discharge (Human Body Model: $R=1.5\text{K}\Omega$ ; $C=100\text{pF}$ )		
	- INPUT	4000	V
	- CURRENT SENSE	2000	V
	- OUTPUT	5000	V
	- $V_{CC}$	5000	V
$E_{MAX}$	Maximum switching energy ( $L=0.11\text{mH}$ ; $R_L=0\Omega$ ; $V_{bat}=13.5\text{V}$ ; $T_{jstart}=150^{\circ}\text{C}$ ; $I_L=40\text{A}$ )	126	mJ
$P_{tot}$	Power dissipation (per island) at $T_{lead}=25^{\circ}\text{C}$	6.25	W
$T_j$	Junction operating temperature	Internally limited	$^{\circ}\text{C}$
$T_{stg}$	Storage temperature	-55 to 150	$^{\circ}\text{C}$

## 2.2 Thermal data

**Table 4. Thermal data (per island)**

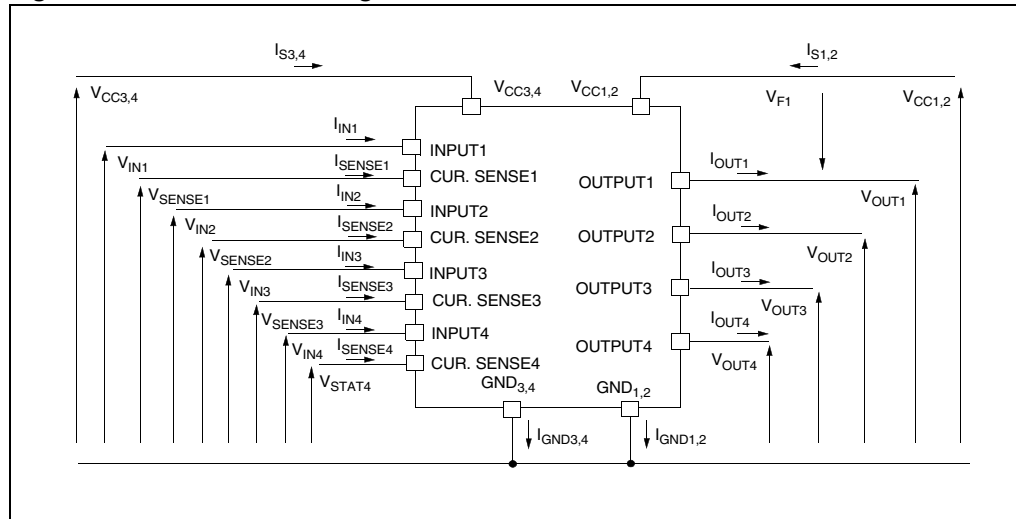
Symbol	Parameter	Value		Unit
$R_{thj-lead}$	Thermal resistance junction-lead	15		°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient (one chip ON)	60 <sup>(1)</sup>	44 <sup>(2)</sup>	°C/W
$R_{thj-amb}$	Thermal Resistance junction-ambient (two chips ON)	46 <sup>(1)</sup>	31 <sup>(2)</sup>	°C/W

1. When mounted on a standard single-sided FR-4 board with 0.5cm<sup>2</sup> of Cu (at least 35 μm thick) connected to all V<sub>CC</sub> pins. Horizontal mounting and no artificial air flow.
2. When mounted on a standard single-sided FR-4 board with 6cm<sup>2</sup> of Cu (at least 35 μm thick) connected to all V<sub>CC</sub> pins. Horizontal mounting and no artificial air flow.

## 2.3 Electrical characteristics

Values specified in this section are for 8V < V<sub>CC</sub> < 36V; -40°C < T<sub>j</sub> < 150°C, unless otherwise stated.

**Figure 3. Current and voltage conventions**



Note:  $V_{Fn} = V_{CCn} - V_{OUTn}$  during reverse battery condition.



Table 5. Power

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CC}$	Operating supply voltage		5.5	13	36	V
$V_{USD}$	Undervoltage shutdown		3	4	5.5	V
$V_{OV}$	Overvoltage shutdown		36			V
$R_{ON}$	On state resistance	$I_{OUT1,2,3,4}=5A$ ; $T_j=25^{\circ}C$			35	m $\Omega$
		$I_{OUT1,2,3,4}=5A$ ; $T_j=150^{\circ}C$			70	m $\Omega$
		$I_{OUT1,2,3,4}=3A$ ; $V_{CC}=6V$			120	m $\Omega$
$V_{clamp}$	Clamp voltage	$I_{CC}=20mA$	41	48	55	V
$I_S$	Supply current	Off State; $V_{CC}=13V$ ; $V_{IN}=V_{OUT}=0V$		12	40	$\mu A$
		Off State; $V_{CC}=13V$ ; $V_{IN}=V_{OUT}=0V$ ; $T_j=25^{\circ}C$		12	25	$\mu A$
		On State; $V_{CC}=13V$ ; $V_{IN}=5V$ ; $I_{OUT}=0A$ ; $R_{SENSE}=3.9K\Omega$			6	mA
$I_{L(off1)}$	Off state output current	$V_{IN}=V_{OUT}=0V$	0		50	$\mu A$
$I_{L(off2)}$	Off state output current	$V_{IN}=0V$ ; $V_{OUT}=3.5V$	-75		0	$\mu A$
$I_{L(off3)}$	Off state output current	$V_{IN}=V_{OUT}=0V$ ; $V_{CC}=13V$ ; $T_j=125^{\circ}C$			5	$\mu A$
$I_{L(off4)}$	Off state output current	$V_{IN}=V_{OUT}=0V$ ; $V_{CC}=13V$ ; $T_j=25^{\circ}C$			3	$\mu A$

Note:  $V_{clamp}$  and  $V_{OV}$  are correlated. Typical difference is 5V.

Table 6. Protections

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{lim}$	DC Short circuit current	$V_{CC}=13V$ $5.5V < V_{CC} < 36V$	25	40	70 70	A A
$T_{TSD}$	Thermal shutdown temperature		150	175	200	$^{\circ}C$
$T_R$	Thermal reset temperature		135			$^{\circ}C$
$T_{hyst}$	Thermal hysteresis		7	15		$^{\circ}C$
$V_{demag}$	Turn-off output voltage clamp	$I_{OUT}=2A$ ; $L=6mH$	$V_{CC}-41$	$V_{CC}-48$	$V_{CC}-55$	V
$V_{ON}$	Output voltage drop limitation	$I_{OUT}=0.5A$ ; $T_j=-40^{\circ}C...+150^{\circ}C$		50		mV

Note: To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 7. Switching ( $V_{CC}=13V$ ;  $T_j = 25^\circ C$ )

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L=2.6\Omega$ channels 1,2,3,4 (see Figure 5)		40		$\mu s$
$t_{d(off)}$	Turn-off delay time	$R_L=2.6\Omega$ channels 1,2,3,4 (see Figure 5)		40		$\mu s$
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	$R_L=2.6\Omega$ channels 1,2,3,4 (see Figure 5)		See Figure 10		V/ $\mu s$
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	$R_L=2.6\Omega$ channels 1,2,3,4 (see Figure 5)		See Figure 12		V/ $\mu s$

Table 8. Current sense ( $9V < V_{CC} < 16V$ )

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$K_1$	$I_{OUT}/I_{SENSE}$	$I_{OUT1}$ or $I_{OUT2}=0.5A$ ; $V_{SENSE}=0.5V$ ; other channels open; $T_j = -40^\circ C \dots 150^\circ C$	3300	4400	6000	
$dK_1/K_1$	Current sense ratio drift	$I_{OUT1}$ or $I_{OUT2}=0.35A$ ; $V_{SENSE}=0.5V$ ; other channels open; $T_j = -40^\circ C \dots 150^\circ C$	-10		+10	%
$K_2$	$I_{OUT}/I_{SENSE}$	$I_{OUT1}$ or $I_{OUT2}=5A$ ; $V_{SENSE}=4V$ ; other channels open; $T_j = -40^\circ C$ $T_j = 25^\circ C \dots 150^\circ C$	4200 4400	4900 4900	6000 5750	
$dK_2/K_2$	Current sense ratio drift	$I_{OUT1}$ or $I_{OUT2}=2A$ ; $V_{SENSE}=2.5V$ ; other channels open; $T_j = -40^\circ C \dots 150^\circ C$	-6		+6	%
$K_3$	$I_{OUT}/I_{SENSE}$	$I_{OUT1}$ or $I_{OUT2}=15A$ ; $V_{SENSE}=4V$ ; other channels open; $T_j = -40^\circ C$ $T_j = 25^\circ C \dots 150^\circ C$	4200 4400	4900 4900	5500 5250	
$dK_3/K_3$	Current sense ratio drift	$I_{OUT1}$ or $I_{OUT2}=15A$ ; $V_{SENSE}=4V$ ; other channels open; $T_j = -40^\circ C \dots 150^\circ C$	-6		+6	%
$V_{SENSE1,2}$	Max analog sense output voltage	$V_{CC}=5.5V$ ; $I_{OUT1,2}=2.5A$ ; $R_{SENSE}=10k\Omega$ $V_{CC}>8V$ , $I_{OUT1,2}=5A$ ; $R_{SENSE}=10k\Omega$	2 4			V V
$V_{SENSEH}$	Analog sense output voltage in overtemperature condition	$V_{CC}=13V$ ; $R_{SENSE}=3.9k\Omega$		5.5		V

**Table 8. Current sense (9V <math>V\_{CC}</math> <math>< 16V</math>) (continued)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$R_{VSENSEH}$	Analog sense output Impedance in overtemperature condition	$V_{CC}=13V$ ; $T_j > T_{TSD}$ ; All channels open		400		$\Omega$
$t_{DSENSE}$	Current sense delay response	To 90% $I_{SENSE}^{(1)}$			500	$\mu s$

1. Current sense signal delay after positive input slope.

**Table 9. Logic inputs**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IL}$	Low level input voltage				1.25	V
$V_{IH}$	High level input voltage		3.25			V
$V_{I(hyst)}$	Input hysteresis voltage		0.5			V
$I_{IL}$	Input current	$V_{IN}=1.5V$	1			$\mu A$
$I_{IN}$	Input current	$V_{IN}=3.5V$			10	$\mu A$
$V_{ICL}$	Input clamp voltage	$I_{IN}=1mA$ $I_{IN}=-1mA$	6	6.8 -0.7	8	V V

**Table 10.  $V_{CC}$  - output diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_F$	Forward on voltage	$-I_{OUT}=2.3A$ ; $T_j=150^\circ C$			0.6	V

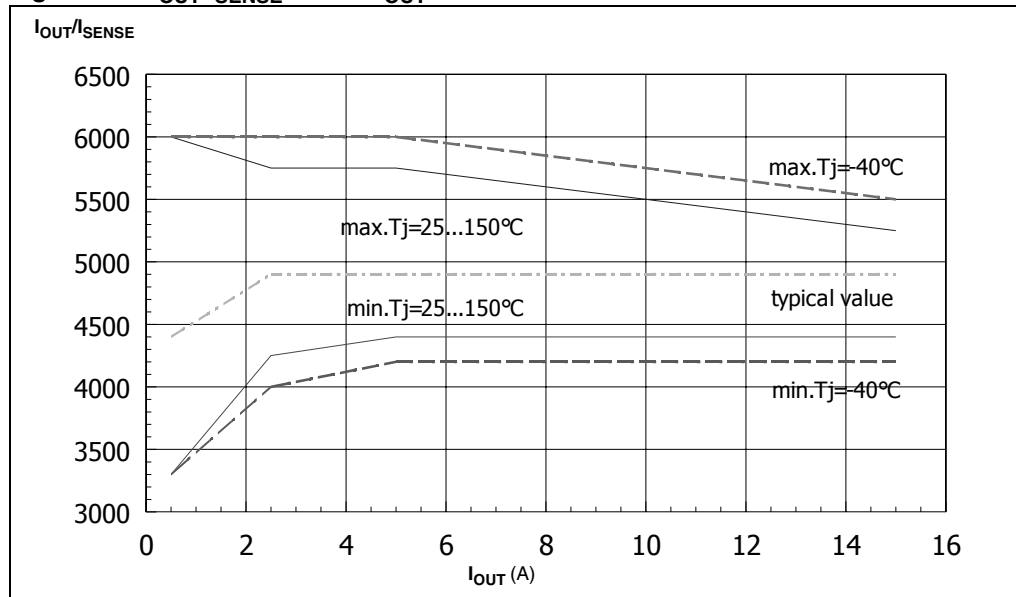
**Figure 4.  $I_{OUT}/I_{SENSE}$  versus  $I_{OUT}$** 

Figure 5. Switching characteristics

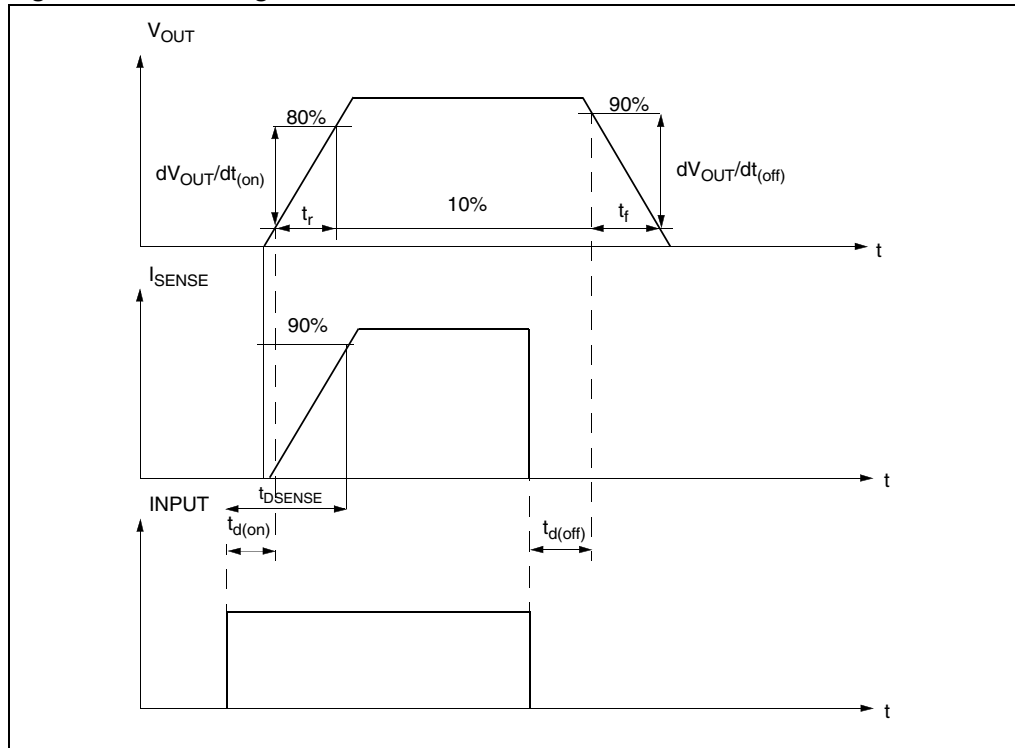


Table 11. Truth table

Conditions	Input	Output	Sense
Normal operation	L	L	0
	H	H	Nominal
Overtemperature	L	L	0
	H	L	$V_{SENSEH}$
Undervoltage	L	L	0
	H	L	0
Overvoltage	L	L	0
	H	L	0
Short circuit to GND	L	L	0
	H	L	$(T_j < T_{TSD}) 0$
	H	L	$(T_j > T_{TSD}) V_{SENSEH}$
Short circuit to $V_{CC}$	L	H	0
	H	H	< Nominal
Negative output voltage clamp	L	L	0

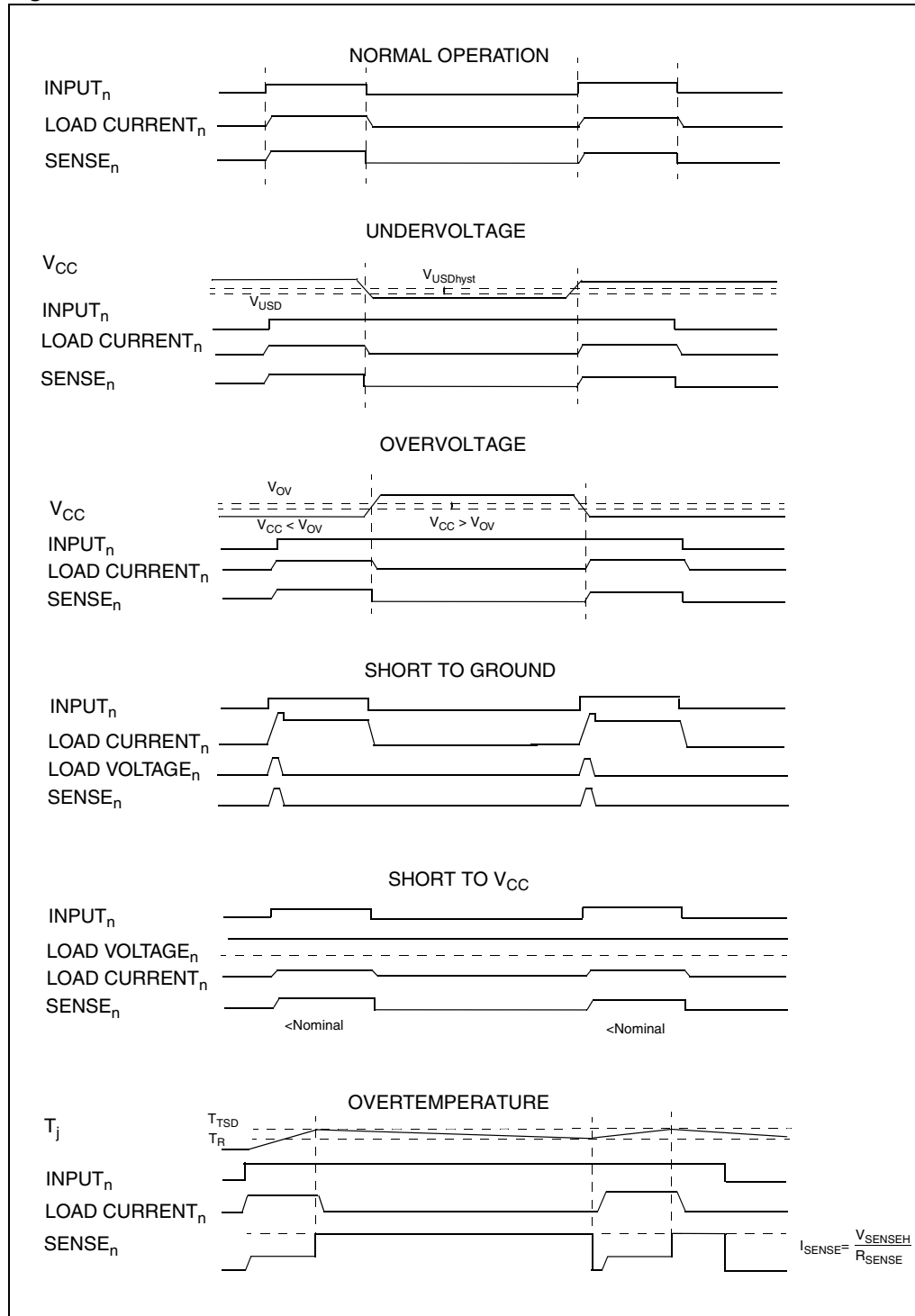
Table 12. Electrical transient requirements

ISO T/R 7637/1 Test pulse	Test levels I	Test levels II	Test levels III	Test levels IV	Test levels delays and impedance
1	-25V	-50V	-75V	-100V	2ms, 10Ω
2	+25V	+50V	+75V	+100V	0.2ms, 10Ω
3a	-25V	-50V	-100V	-150V	0.1 μs, 50Ω
3b	+25V	+50V	+75V	+100V	0.1 μs, 50Ω
4	-4V	-5V	-6V	-7V	100ms, 0.01Ω
5	+26.5V	+46.5V	+66.5V	+86.5V	400ms, 2Ω

ISO T/R 7637/1 Test pulse	Test levels result I	Test levels result II	Test levels result III	Test levels result IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure and cannot be returned to proper operation without replacing the device.

Figure 6. Waveforms



## 2.4 Electrical characteristics curves

Figure 7. Off state output current

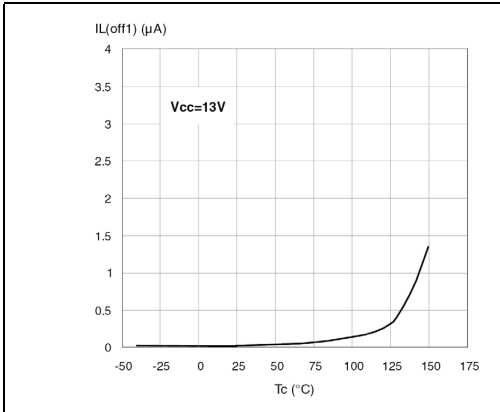


Figure 8. Low level input current

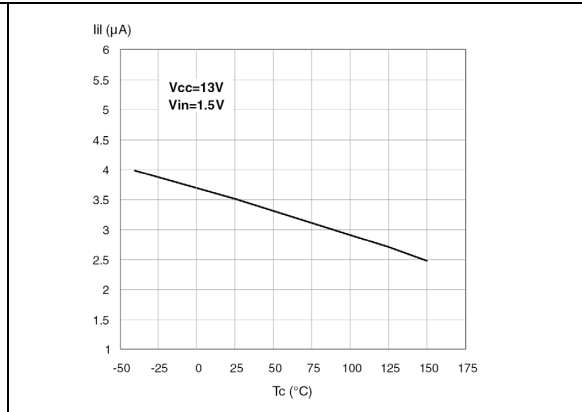


Figure 9. Input clamp voltage

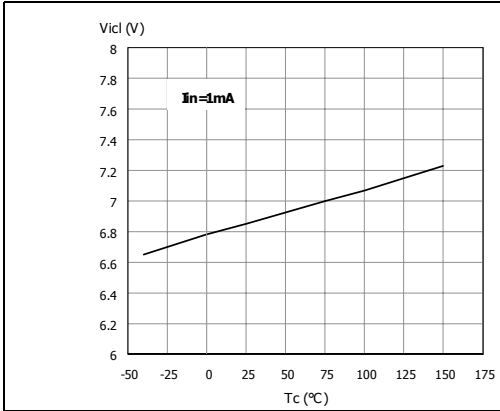


Figure 10. Turn-on voltage slope

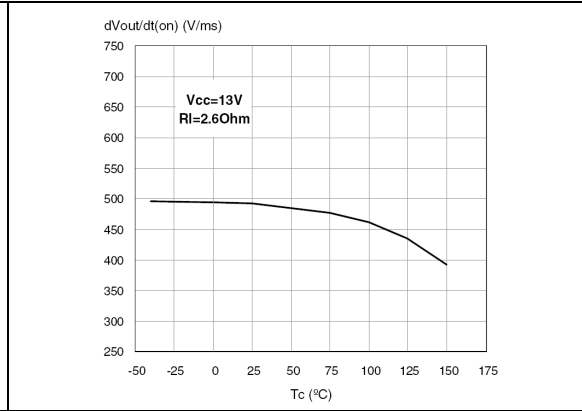


Figure 11. Overvoltage shutdown

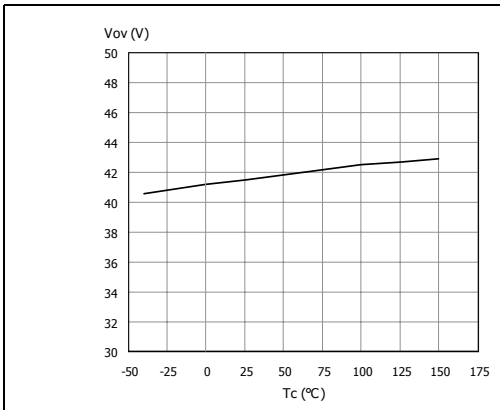


Figure 12. Turn-off voltage slope

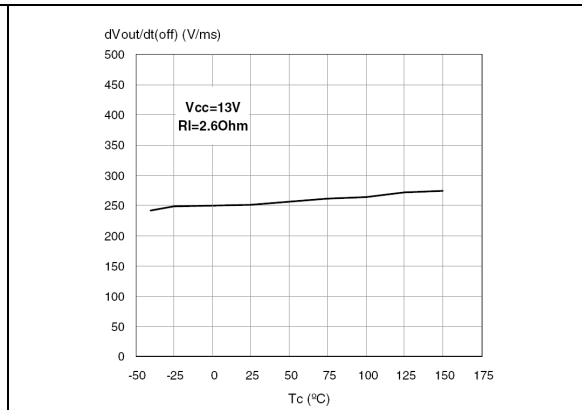


Figure 13.  $I_{LIM}$  vs  $T_{case}$

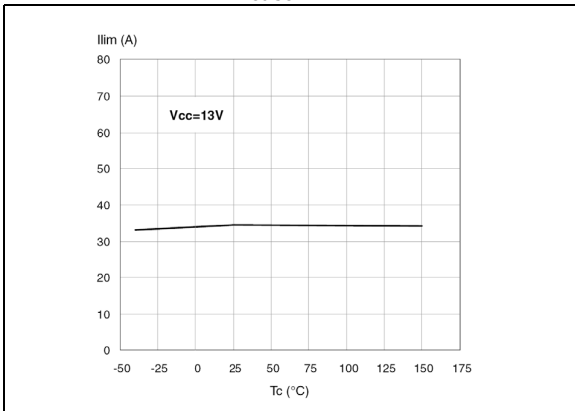


Figure 14. Input low level

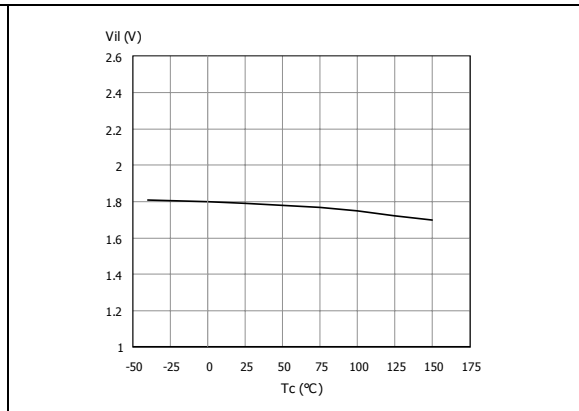


Figure 15. Input high level

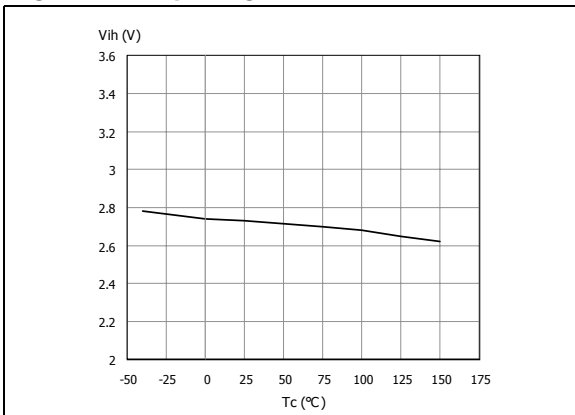


Figure 16. Input hysteresis voltage

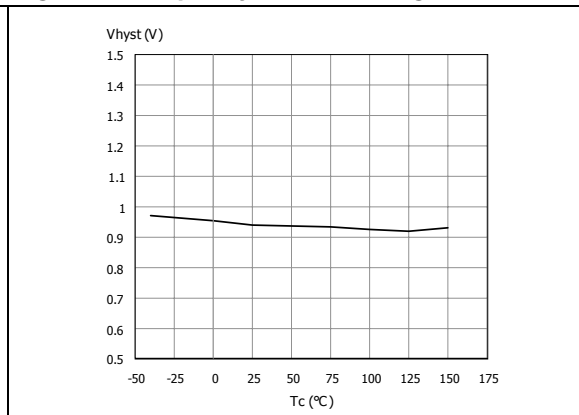
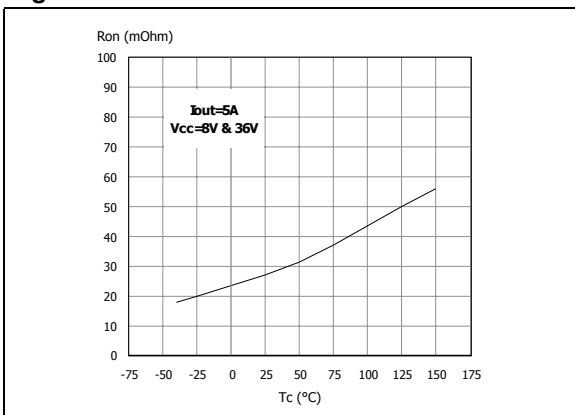


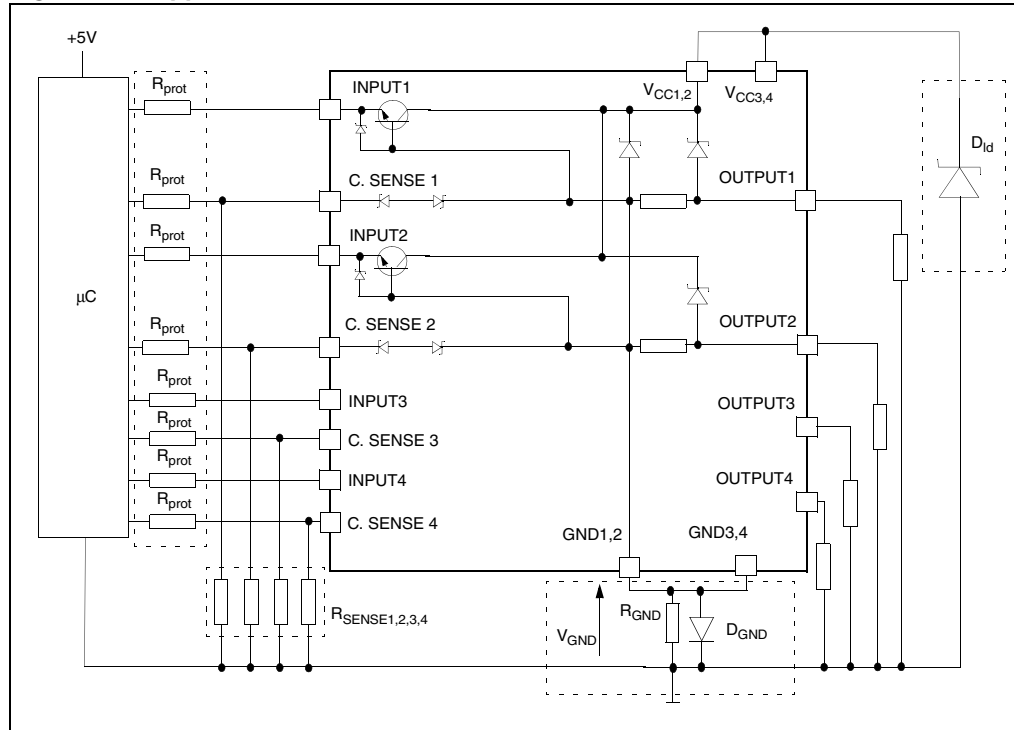
Figure 17. On state resistance vs  $T_{case}$





### 3 Application information

Figure 18. Application schematic



Note: Channels 3 & 4 have the same internal circuit as channel 1 & 2.

#### 3.1 GND protection network against reverse battery

This section provides two solutions for implementing a ground protection network against reverse battery.

##### 3.1.1 Solution 1: a resistor in the ground line ( $R_{GND}$ only)

This can be used with any type of load.

The following show how to dimension the  $R_{GND}$  resistor:

1.  $R_{GND} \leq 600\text{mV} / 2(I_{S(on)max})$
2.  $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where  $-I_{GND}$  is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power dissipation in  $R_{GND}$  (when  $V_{CC} < 0$  during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where  $I_{S(on)max}$  becomes the sum of the maximum on-state currents of the different devices.

Please note that, if the microprocessor ground is not shared by the device ground, then the  $R_{GND}$  will produce a shift ( $I_{S(on)max} * R_{GND}$ ) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same  $R_{GND}$ .

If the calculated power dissipation requires the use of a large resistor, or several devices have to share the same resistor, then ST suggests using solution 2 below.

### 3.1.2 Solution 2: a diode ( $D_{GND}$ ) in the ground line

A resistor ( $R_{GND}=1k\Omega$ ) should be inserted in parallel to  $D_{GND}$  if the device will be driving an inductive load. This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift (j600mV) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network. Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the Absolute Maximum Rating. Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

## 3.2 Load dump protection

$D_{ld}$  is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the  $V_{CC}$  maximum DC rating. The same applies if the device is subject to transients on the  $V_{CC}$  line that are greater than those shown in the ISO T/R 7637/1 table.

## 3.3 MCU I/O protection

If a ground protection network is used and negative transients are present on the  $V_{CC}$  line, the control pins will be pulled negative. ST suggests to insert a resistor ( $R_{prot}$ ) in line to prevent the  $\mu C$  I/O pins from latching up.

The value of these resistors is a compromise between the leakage current of  $\mu C$  and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of  $\mu C$  I/Os:

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

### Example

For the following conditions:

$$V_{CCpeak} = -100V$$

$$I_{latchup} \geq 20mA$$

$$V_{OH\mu C} \geq 4.5V$$

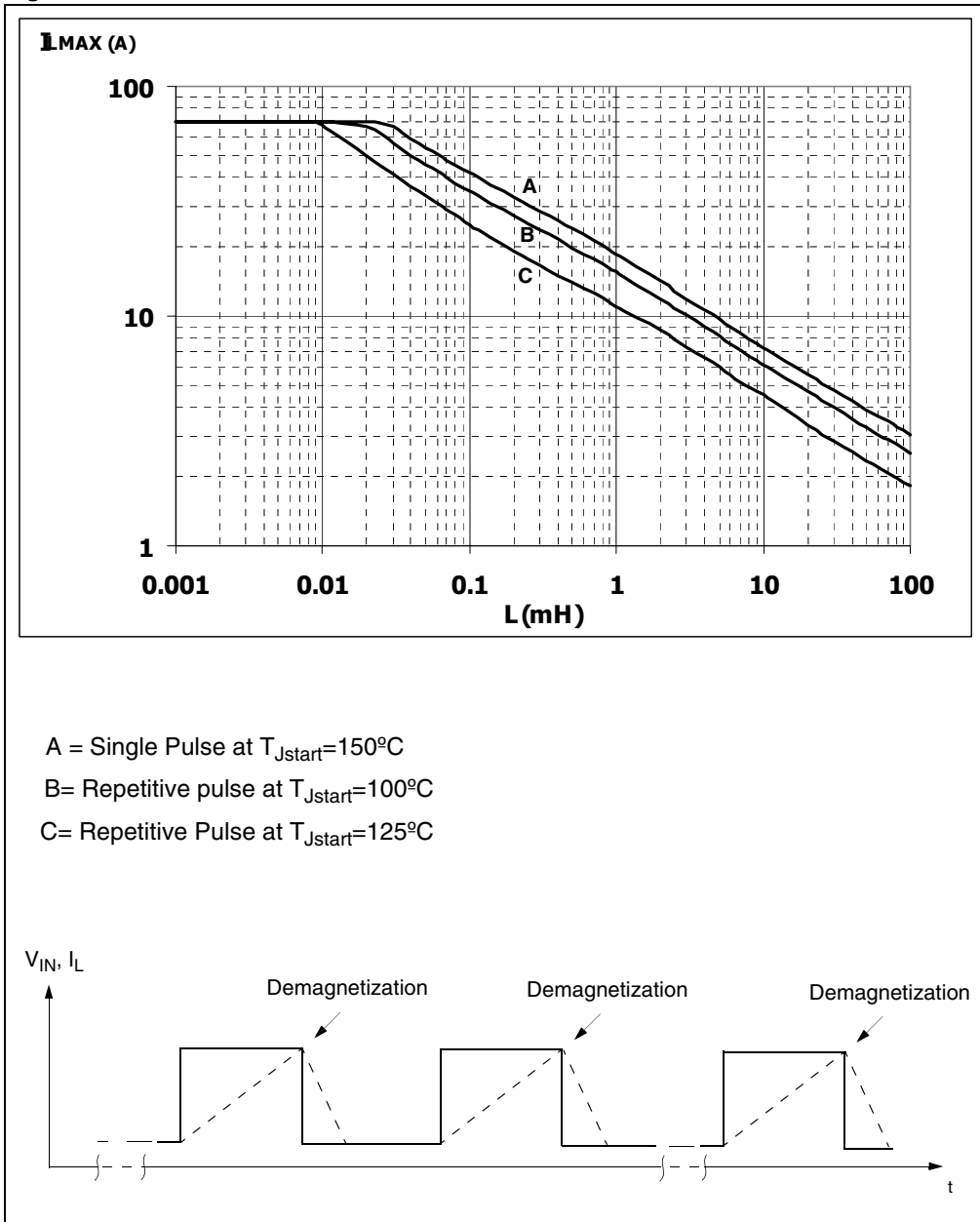
$$5k\Omega \leq R_{prot} \leq 65k\Omega$$

Recommended values are:

$$R_{prot} = 10k\Omega$$

### 3.4 Maximum demagnetization energy (Vcc = 13.5V)

Figure 19. Maximum turn-off current versus load inductance

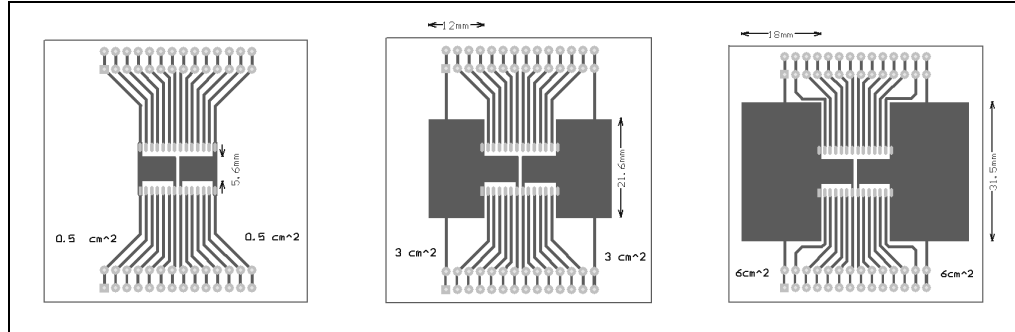


Note: Values are generated with  $R_L=0\Omega$   
 In case of repetitive pulses,  $T_{Jstart}$  (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

## 4 Package and PCB thermal data

### 4.1 SO-28 thermal data

Figure 20. SO-28 PC board



Note: Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB FR4 area= 58mm x 58mm, PCB thickness=2mm, Cu thickness=35 $\mu$ m, Copper areas: 0.5 cm<sup>2</sup>, 3 cm<sup>2</sup>, 6 cm<sup>2</sup>).

Table 13. Thermal calculation according to the PCB heatsink area

Chip 1	Chip 2	$T_{jchip1}$	$T_{jchip2}$	Note
ON	OFF	$R_{thA} \times P_{dchip1} + T_{amb}$	$R_{thC} \times P_{dchip1} + T_{amb}$	
OFF	ON	$R_{thC} \times P_{dchip2} + T_{amb}$	$R_{thA} \times P_{dchip2} + T_{amb}$	
ON	ON	$R_{thB} \times (P_{dchip1} + P_{dchip2}) + T_{amb}$	$R_{thB} \times (P_{dchip1} + P_{dchip2}) + T_{amb}$	$P_{dchip1} = P_{dchip2}$
ON	ON	$(R_{thA} \times P_{dchip1}) + R_{thC} \times P_{dchip2} + T_{amb}$	$(R_{thA} \times P_{dchip2}) + R_{thC} \times P_{dchip1} + T_{amb}$	$P_{dchip1} \neq P_{dchip2}$

$R_{thA}$  = Thermal resistance Junction to Ambient with one chip ON

$R_{thB}$  = Thermal resistance Junction to Ambient with both chips ON and  $P_{dchip1} = P_{dchip2}$

$R_{thC}$  = Mutual thermal resistance

Figure 21.  $R_{thj-amb}$  Vs PCB copper area in open box free air condition

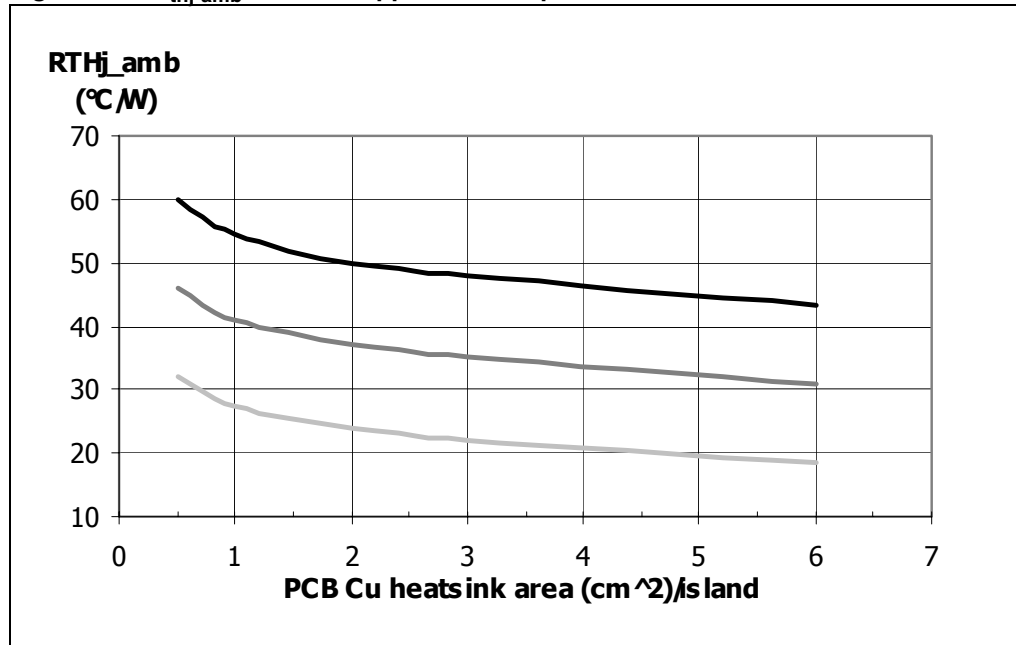
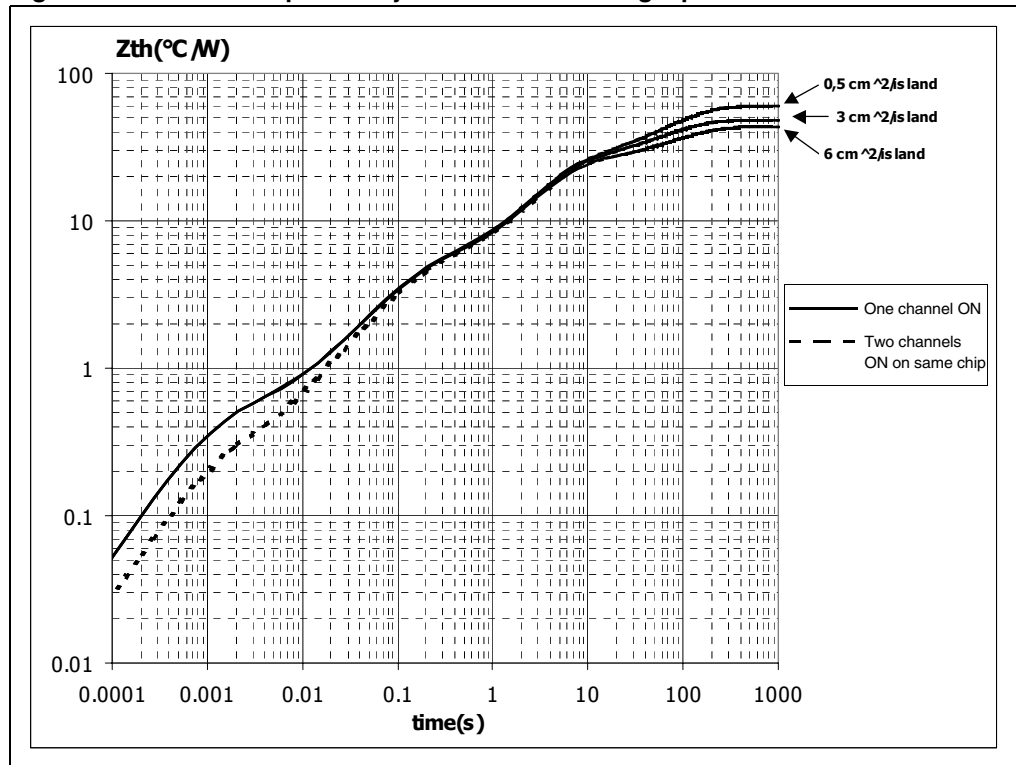


Figure 22. Thermal impedance junction ambient single pulse

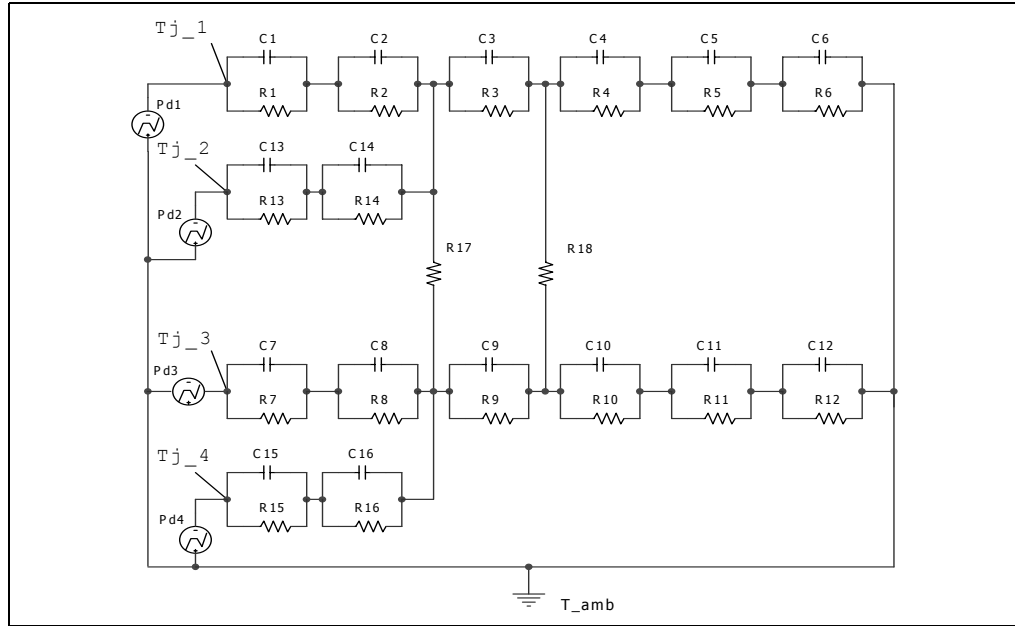


**Equation 1:** pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p / T$

**Figure 23. Thermal fitting model of a quad channel HSD in SO-28**



**Table 14. Thermal parameters**

Area/island (cm <sup>2</sup> )	0.5	6
R1=R7=R13=R15 (°C/W)	0.05	
R2=R8=R14=R16 (°C/W)	0.3	
R3=R9 (°C/W)	3.4	
R4=R10 (°C/W)	11	
R5=R11 (°C/W)	15	
R6=R12 (°C/W)	30	13
C1=C7=C13=C15 (W.s/°C)	0.001	
C2=C8=C14=C16 (W.s/°C)	5.00E-03	
C3=C9 (W.s/°C)	1.00E-02	
C4=C10 (W.s/°C)	0.2	
C5=C11 (W.s/°C)	1.5	
C6=C12 (W.s/°C)	5	8
R17=R18 (°C/W)	150	

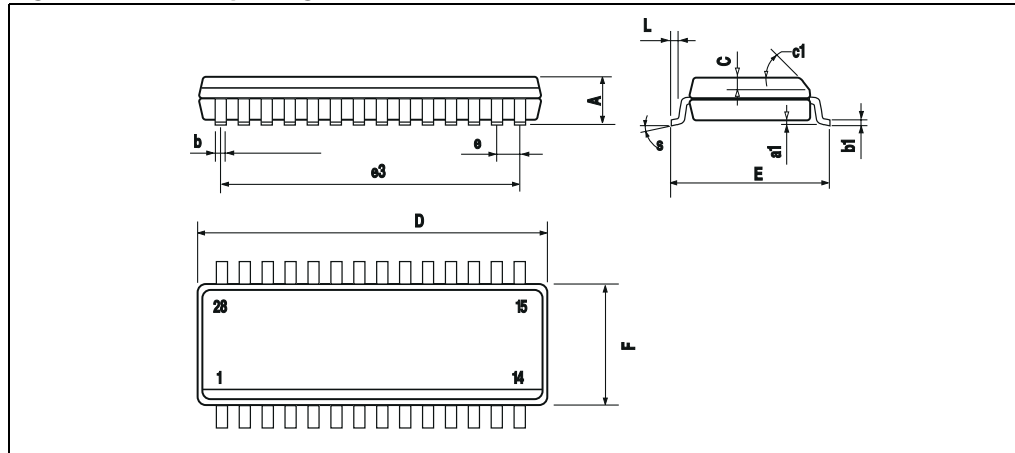
## 5 Package and packing information

### 5.1 ECOPACK<sup>®</sup> packages

In order to meet environmental requirements, ST offers these devices in ECOPACK<sup>®</sup> packages. These packages have a Lead-free second-level interconnect. The category of Second-Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

**Figure 24. SO-28 package dimensions**



**Table 15. SO-28 mechanical data**

Symbol	Millimeters		
	Min.	Typ.	Max.
A			2.65
a1	0.10		0.30
b	0.35		0.49
b1	0.23		0.32
C		0.50	
c1	45° (typ.)		
D	17.7		18.1
E	10.00		10.65
e		1.27	
e3		16.51	
F	7.40		7.60
L	0.40		1.27
S	8° (max.)		

## 5.2 SO-28 packing information

Figure 25. SO-28 tube shipment (no suffix)

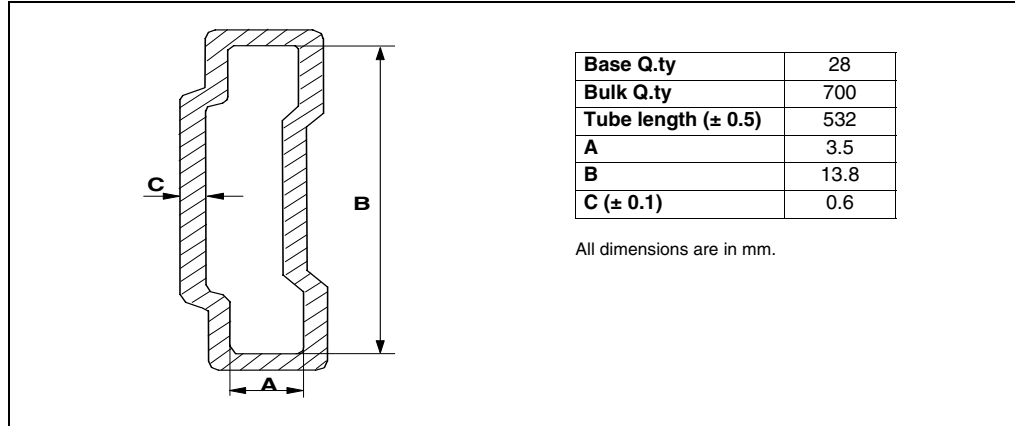
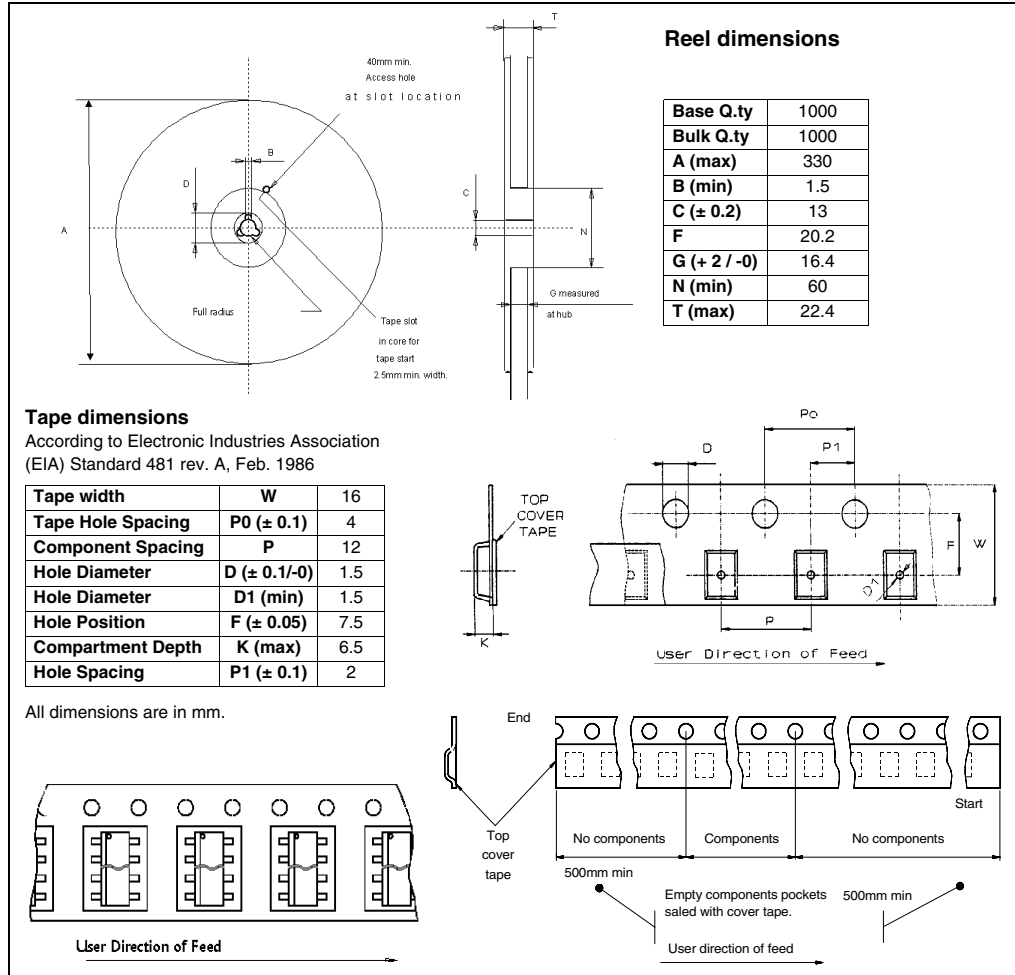


Figure 26. SO-28 tape and reel shipment (suffix “TR”)





## 6 Revision history

Table 16. Document revision history

Date	Revision	Changes
Oct-2004	1	Initial release.
02-Jul-2006	2	Added <a href="#">Table 16: Document revision history</a> .
11-Nov-2008	3	Document converted to corporate template.

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