



# VN820 / VN820SO VN820SP / VN820-B5 / VN820PT

## HIGH SIDE DRIVER

TYPE	$R_{DS(on)}$	$I_{OUT}$	$V_{CC}$
VN820	40 m $\Omega$	9 A	36 V
VN820SP			
VN820-B5			
VN820SO			
VN820PT			
VN820PT			

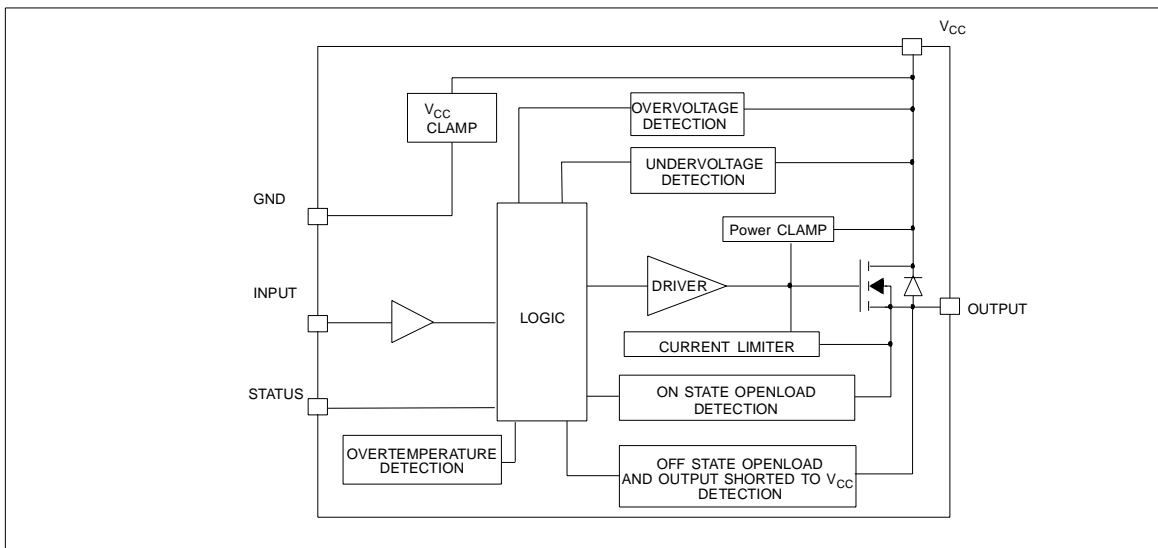
- CMOS COMPATIBLE INPUT
- ON STATE OPEN LOAD DETECTION
- OFF STATE OPEN LOAD DETECTION
- SHORTED LOAD PROTECTION
- UNDERVOLTAGE AND OVERVOLTAGE SHUTDOWN
- PROTECTION AGAINST LOSS OF GROUND
- VERY LOW STAND-BY CURRENT
- REVERSE BATTERY PROTECTION (\*)

### DESCRIPTION

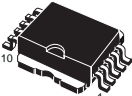
The VN820, VN820SP, VN820-B5, VN820SO, VN820PT are monolithic devices made by using STMicroelectronics VIPower M0-3 Technology, intended for driving any kind of load with one side connected to ground.

Active  $V_{CC}$  pin voltage clamp protects the device against low energy spikes (see ISO7637 transient

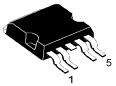
### BLOCK DIAGRAM



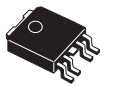
(\*) See application schematic at page 9  
July 2004



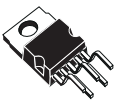
**PowerSO-10™**



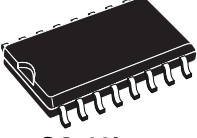
**P<sup>2</sup>PAK**



**PPAK**



**PENTAWATT**



**SO-16L**

ORDER CODES		
PACKAGE	TUBE	T&R
PENTAWATT	VN820	-
PowerSO-10™	VN820SP	VN820SP13TR
P <sup>2</sup> PAK	VN820-B5	VN820-B513TR
SO-16L	VN820SO	VN820SO13TR
PPAK	VN820PT	VN820PT13TR

compatibility table). Active current limitation combined with thermal shutdown and automatic restart protect the device against overload.

The device detects open load condition both in on and off state. Output shorted to  $V_{CC}$  is detected in the off state. Device automatically turns off in case of ground pin disconnection.

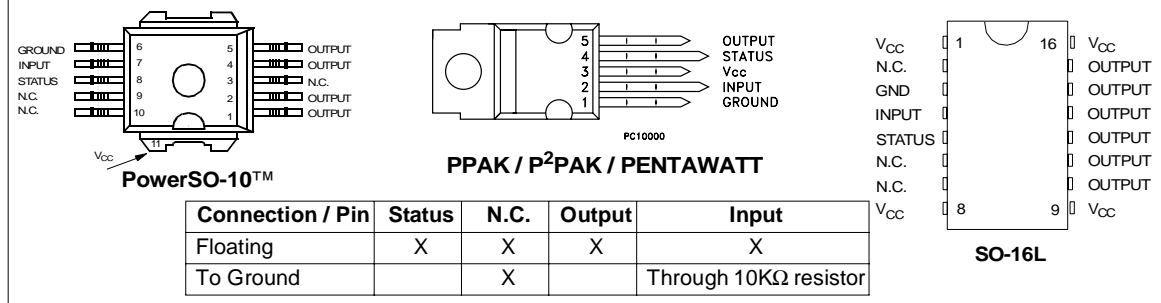
Rev. 1

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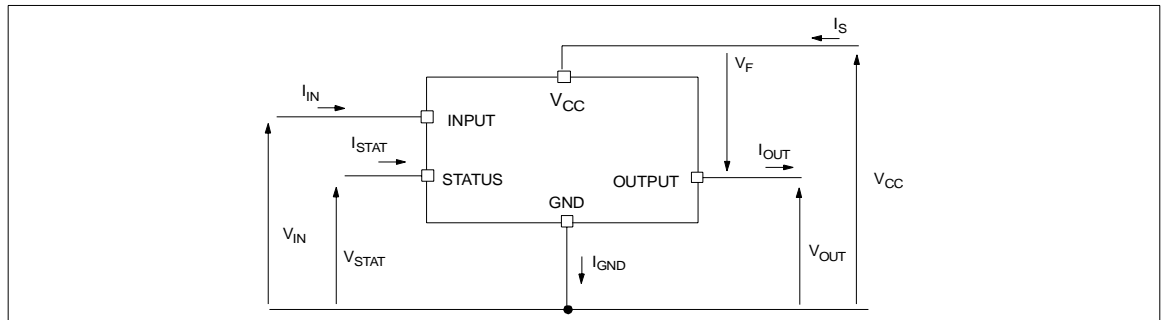
**ABSOLUTE MAXIMUM RATING**

Symbol	Parameter	Value					Unit
		PowerSO-10™	PENTAWATT	P <sup>2</sup> PAK	SO-16L	PPAK	
V <sub>CC</sub>	DC Supply Voltage	41					V
- V <sub>CC</sub>	Reverse DC Supply Voltage	- 0.3					V
- I <sub>GND</sub>	DC Reverse Ground Pin Current	- 200					mA
I <sub>OUT</sub>	DC Output Current	Internally Limited					A
- I <sub>OUT</sub>	Reverse DC Output Current	- 9					A
I <sub>IN</sub>	DC Input Current	+/- 10					mA
I <sub>STAT</sub>	DC Status Current	+/- 10					mA
V <sub>ESD</sub>	Electrostatic Discharge (Human Body Model: R=1.5KΩ; C=100pF)						
	- INPUT	4000					V
	- STATUS	4000					V
	- OUTPUT	5000					V
	- V <sub>CC</sub>	5000					V
E <sub>MAX</sub>	Maximum Switching Energy (L=4mH; R <sub>L</sub> =0Ω; V <sub>bat</sub> =13.5V; T <sub>jstart</sub> =150°C; I <sub>L</sub> =13A)	481		481			mJ
E <sub>MAX</sub>	Maximum Switching Energy (L=3.7mH; R <sub>L</sub> =0Ω; V <sub>bat</sub> =13.5V; T <sub>jstart</sub> =150°C; I <sub>L</sub> =13A)				438		mJ
E <sub>MAX</sub>	Maximum Switching Energy (L=4.48mH; R <sub>L</sub> =0Ω; V <sub>bat</sub> =13.5V; T <sub>jstart</sub> =150°C; I <sub>L</sub> =13A)					526	mJ
P <sub>tot</sub>	Power Dissipation T <sub>C</sub> =25°C	65.8	65.8	65.8	8.3	65.8	W
T <sub>j</sub>	Junction Operating Temperature	Internally Limited					°C
T <sub>C</sub>	Case Operating Temperature	- 40 to 150					°C
T <sub>stg</sub>	Storage Temperature	- 55 to 150					°C

**CONFIGURATION DIAGRAM (TOP VIEW) & SUGGESTED CONNECTIONS FOR UNUSED AND N.C. PINS**



**CURRENT AND VOLTAGE CONVENTIONS**



**THERMAL DATA**

Symbol	Parameter		Value					Unit
			PowerSO-10	PENTAWATT	P <sup>2</sup> PAK	SO-16L	PPAK	
R <sub>thj-case</sub>	Thermal Resistance Junction-case	Max	1.9	1.9	1.9	-	1.9	°C/W
R <sub>thj-lead</sub>	Thermal Resistance Junction-lead	Max	-	-	-	15	-	°C/W
R <sub>thj-amb</sub>	Thermal Resistance Junction-ambient	Max	51.9 <sup>(1)</sup>	61.9 <sup>(1)</sup>	51.9 <sup>(1)</sup>	65 <sup>(2)</sup>	76.9 <sup>(1)</sup>	°C/W
R <sub>thj-amb</sub>	Thermal Resistance Junction-ambient	Max	37 <sup>(3)</sup>	-	37 <sup>(3)</sup>	48 <sup>(4)</sup>	45 <sup>(3)</sup>	°C/W

(1) When mounted on a standard single-sided FR-4 board with 0.5cm<sup>2</sup> of Cu (at least 35µm thick).

(2) When mounted on FR4 printed circuit board with 0.5cm<sup>2</sup> of Cu (at least 35µ thick) connected to all V<sub>CC</sub> pins.

(3) When mounted on a standard single-sided FR-4 board with 6cm<sup>2</sup> of Cu (at least 35µm thick).

(4) When mounted on FR4 printed circuit board with 6cm<sup>2</sup> of Cu (at least 35µ thick) connected to all V<sub>CC</sub> pins.

**ELECTRICAL CHARACTERISTICS** (8V<V<sub>CC</sub><36V; -40°C<T<sub>j</sub><150°C unless otherwise specified)

**POWER**

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	Operating Supply Voltage		5.5	13	36	V
V <sub>USD</sub>	Undervoltage Shut-down		3	4	5.5	V
V <sub>USDhyst</sub>	Undervoltage Shut-down hysteresis			0.5		V
V <sub>OV</sub>	Overvoltage Shut-down		36			V
R <sub>ON</sub>	On State Resistance	I <sub>OUT</sub> =3A; T <sub>j</sub> =25°C; V <sub>CC</sub> >8V			40	mΩ
		I <sub>OUT</sub> =3A; V <sub>CC</sub> >8V			80	mΩ
I <sub>S</sub>	Supply Current	Off State; V <sub>CC</sub> =13V; V <sub>IN</sub> =V <sub>OUT</sub> =0V		10	25	µA
		Off State; V <sub>CC</sub> =13V; V <sub>IN</sub> =V <sub>OUT</sub> =0V; T <sub>j</sub> =25°C		10	20	µA
		On State; V <sub>CC</sub> =13V; V <sub>IN</sub> =5V; I <sub>OUT</sub> =0A		2	3.5	mA
I <sub>L(off1)</sub>	Off State Output Current	V <sub>IN</sub> =V <sub>OUT</sub> =0V	0		50	µA
I <sub>L(off2)</sub>	Off State Output Current	V <sub>IN</sub> =0V; V <sub>OUT</sub> =3.5V	-75		0	µA
I <sub>L(off3)</sub>	Off State Output Current	V <sub>IN</sub> =V <sub>OUT</sub> =0V; V <sub>CC</sub> =13V; T <sub>j</sub> =125°C			5	µA
I <sub>L(off4)</sub>	Off State Output Current	V <sub>IN</sub> =V <sub>OUT</sub> =0V; V <sub>CC</sub> =13V; T <sub>j</sub> =25°C			3	µA

**SWITCHING** (V<sub>CC</sub>=13V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t <sub>d(on)</sub>	Turn-on Delay Time	R <sub>L</sub> =4.3Ω from V <sub>IN</sub> rising edge to V <sub>OUT</sub> =1.3V		30		µs
t <sub>d(off)</sub>	Turn-off Delay Time	R <sub>L</sub> =4.3Ω from V <sub>IN</sub> falling edge to V <sub>OUT</sub> =11.7V		30		µs
dV <sub>OUT</sub> /dt <sub>(on)</sub>	Turn-on Voltage Slope	R <sub>L</sub> =4.3Ω from V <sub>OUT</sub> =1.3 to V <sub>OUT</sub> =10.4V		See relative diagram		V/µs
dV <sub>OUT</sub> /dt <sub>(off)</sub>	Turn-off Voltage Slope	R <sub>L</sub> =4.3Ω from V <sub>OUT</sub> =11.7 to V <sub>OUT</sub> =1.3V		See relative diagram		V/µs

## VN820 / VN820SO / VN820SP / VN820-B5 / VN820PT

### ELECTRICAL CHARACTERISTICS (continued)

#### INPUT PIN

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{IL}$	Input Low Level				1.25	V
$I_{IL}$	Low Level Input Current	$V_{IN}=1.25V$	1			$\mu A$
$V_{IH}$	Input High Level		3.25			V
$I_{IH}$	High Level Input Current	$V_{IN}=3.25V$			10	$\mu A$
$V_{I(hyst)}$	Input Hysteresis Voltage		0.5			V
$V_{ICL}$	Input Clamp Voltage	$I_{IN}=1mA$ $I_{IN}=-1mA$	6	6.8 -0.7	8	V V

#### $V_{CC}$ - OUTPUT DIODE

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_F$	Forward on Voltage	$-I_{OUT}=2A$ ; $T_j=150^\circ C$			0.6	V

#### STATUS PIN

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{STAT}$	Status Low Output Voltage	$I_{STAT}=1.6mA$			0.5	V
$I_{LSTAT}$	Status Leakage Current	Normal Operation $V_{STAT}=5V$			10	$\mu A$
$C_{STAT}$	Status Pin Input Capacitance	Normal Operation $V_{STAT}=5V$			100	pF
$V_{SCL}$	Status Clamp Voltage	$I_{STAT}=1mA$ $I_{STAT}=-1mA$	6	6.8 -0.7	8	V V

#### PROTECTIONS (see note 1)

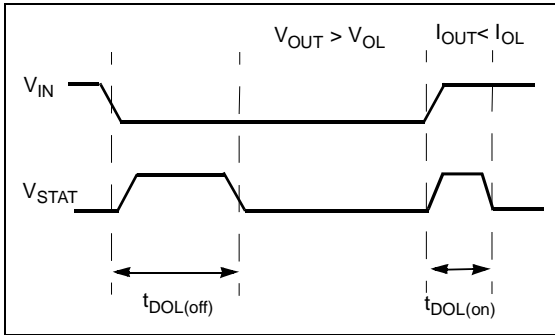
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$T_{TSD}$	Shut-down Temperature		150	175	200	$^\circ C$
$T_R$	Reset Temperature		135			$^\circ C$
$T_{hyst}$	Thermal Hysteresis		7	15		$^\circ C$
$t_{SDL}$	Status delay in overload condition	$T_j > T_{TSD}$			20	$\mu s$
$I_{lim}$	Current limitation	$5.5V < V_{CC} < 36V$	9	13	20 20	A A
$V_{demag}$	Turn-off Output Clamp Voltage	$I_{OUT}=3A$ ; $V_{IN}=0V$ ; $L=6mH$	$V_{CC}-41$	$V_{CC}-48$	$V_{CC}-55$	V

Note 1: To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles

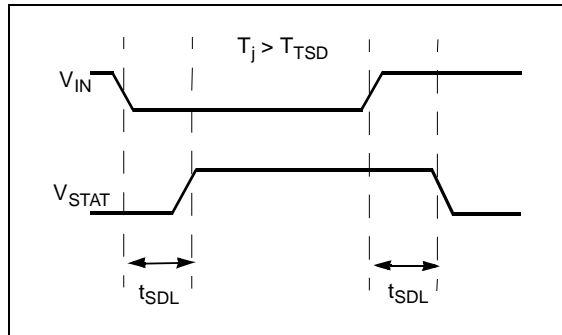
#### OPENLOAD DETECTION

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$I_{OL}$	Openload ON State Detection Threshold	$V_{IN}=5V$	70	150	300	mA
$t_{DOL(on)}$	Openload ON State Detection Delay	$I_{OUT}=0A$			200	$\mu s$
$V_{OL}$	Openload OFF State Voltage Detection Threshold	$V_{IN}=0V$	1.5	2.5	3.5	V
$t_{DOL(off)}$	Openload Detection Delay at Turn Off				1000	$\mu s$

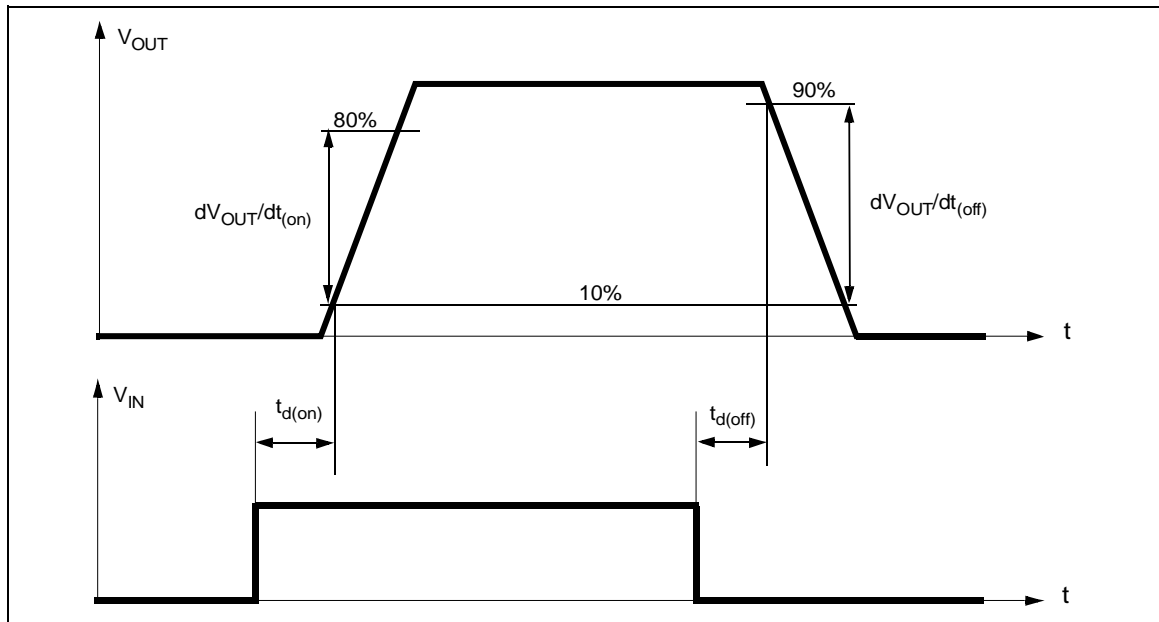
**OPEN LOAD STATUS TIMING (with external pull-up)**



**OVERTEMP STATUS TIMING**



**SWITCHING TIME WAVEFORMS**



**TRUTH TABLE**

CONDITIONS	INPUT	OUTPUT	STATUS
Normal Operation	L	L	H
	H	H	H
Current Limitation	L	L	H
	H	X	( $T_j < T_{TSD}$ ) H ( $T_j > T_{TSD}$ ) L
Overtemperature	L	L	H
	H	L	L
Undervoltage	L	L	X
	H	L	X
Overvoltage	L	L	H
	H	L	H
Output Voltage > $V_{OL}$	L	H	L
	H	H	H
Output Current < $I_{OL}$	L	L	H
	H	H	L

**OPEN LOAD DETECTION IN OFF STATE**

Off state open load detection requires an external pull-up resistor ( $R_{PU}$ ) connected between OUTPUT pin and a positive supply voltage ( $V_{PU}$ ) like the +5V line used to supply the microprocessor.

The external resistor has to be selected according to the following requirements:

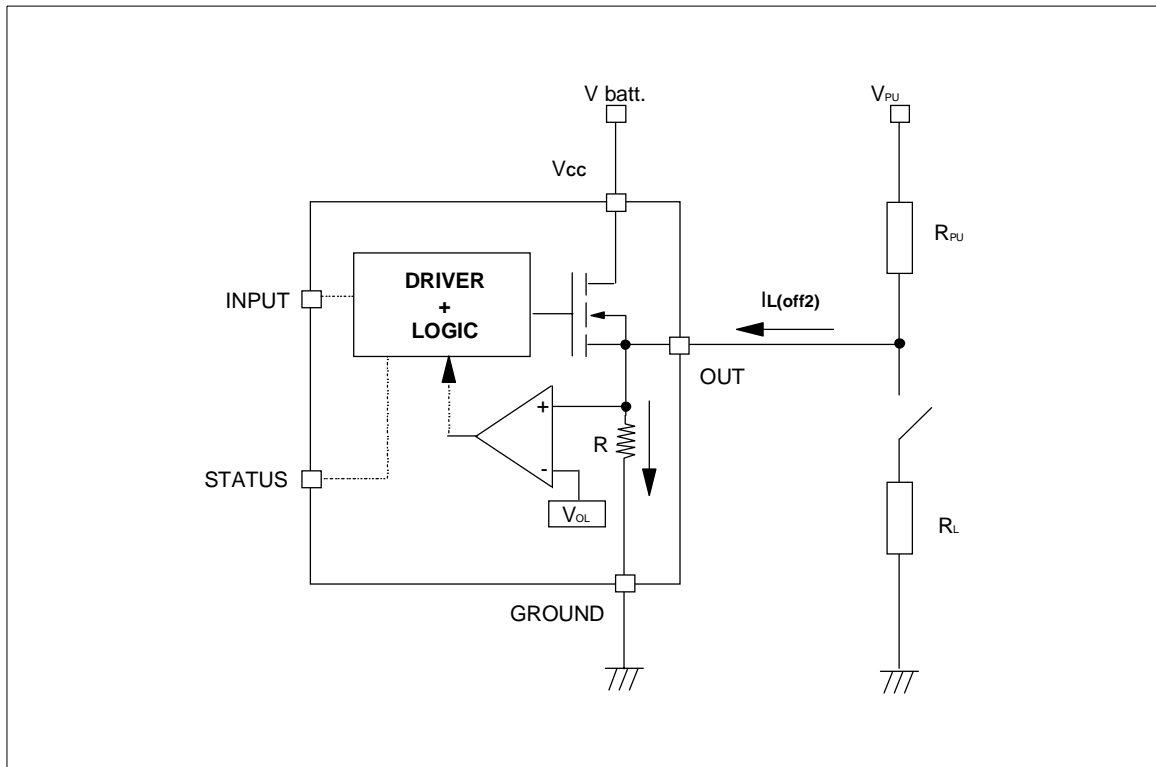
- 1) no false open load indication when load is connected: in this case we have to avoid  $V_{OUT}$  to be higher than  $V_{OLmin}$ ; this results in the following condition  $V_{OUT} = (V_{PU} / (R_L + R_{PU})) R_L < V_{OLmin}$ .

- 2) no misdetection when load is disconnected: in this case the  $V_{OUT}$  has to be higher than  $V_{OLmax}$ ; this results in the following condition  $R_{PU} < (V_{PU} - V_{OLmax}) / I_{L(off2)}$ .

Because  $I_{s(OFF)}$  may significantly increase if  $V_{out}$  is pulled high (up to several mA), the pull-up resistor  $R_{PU}$  should be connected to a supply that is switched OFF when the module is in standby.

The values of  $V_{OLmin}$ ,  $V_{OLmax}$  and  $I_{L(off2)}$  are available in the Electrical Characteristics section.

**Open Load detection in off state**



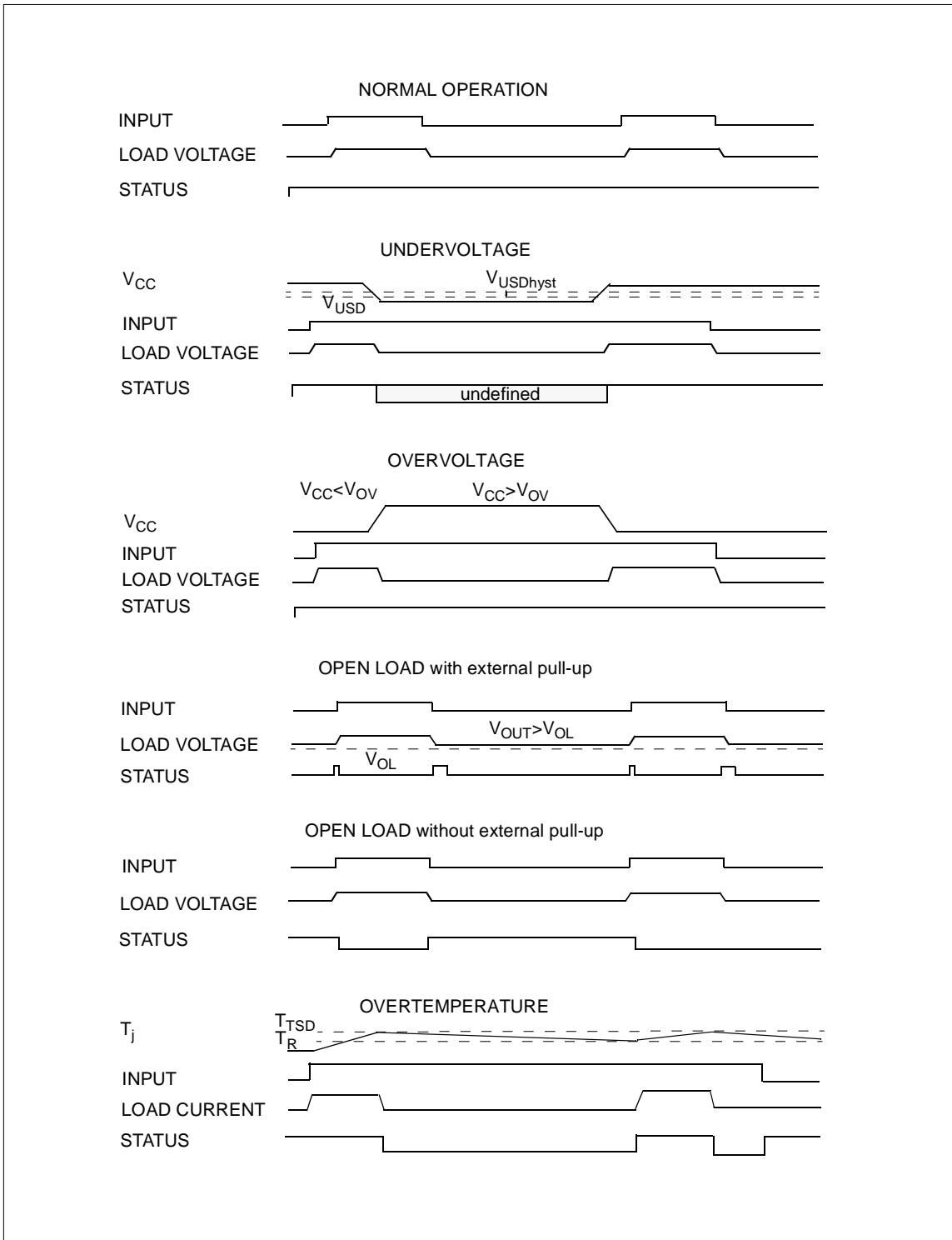
**ELECTRICAL TRANSIENT REQUIREMENTS ON V<sub>CC</sub> PIN**

ISO T/R 7637/1 Test Pulse	TEST LEVELS				
	I	II	III	IV	Delays and Impedance
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 μs 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 μs 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

ISO T/R 7637/1 Test Pulse	TEST LEVELS RESULTS			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

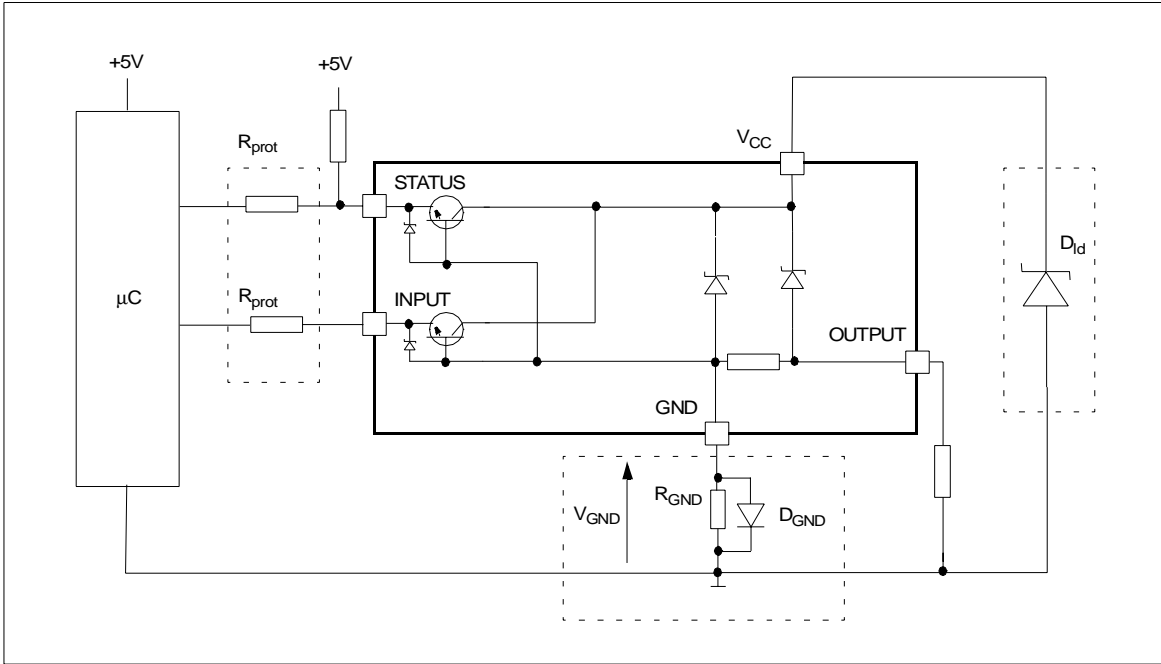
CLASS	CONTENTS
<b>C</b>	All functions of the device are performed as designed after exposure to disturbance.
<b>E</b>	One or more functions of the device is not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 1: Waveforms





**APPLICATION SCHEMATIC**



**GND PROTECTION NETWORK AGAINST REVERSE BATTERY**

**Solution 1:** Resistor in the ground line (R<sub>GND</sub> only). This can be used with any type of load.

The following is an indication on how to dimension the R<sub>GND</sub> resistor.

- 1)  $R_{GND} \leq 600mV / (I_{S(on)max})$ .
- 2)  $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where -I<sub>GND</sub> is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in R<sub>GND</sub> (when V<sub>CC</sub><0: during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where I<sub>S(on)max</sub> becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the R<sub>GND</sub> will produce a shift (I<sub>S(on)max</sub> \* R<sub>GND</sub>) in the input thresholds and the status output values. This shift will vary depending on many devices are ON in the case of several high side drivers sharing the same R<sub>GND</sub>.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2 (see below).

**Solution 2:** A diode (D<sub>GND</sub>) in the ground line.

A resistor (R<sub>GND</sub>=1kΩ) should be inserted in parallel to D<sub>GND</sub> if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift (≈600mV) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the Absolute Maximum Rating.

Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

**LOAD DUMP PROTECTION**

D<sub>Id</sub> is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds V<sub>CC</sub> max DC rating. The same applies if the device will be subject to transients on the V<sub>CC</sub> line that are greater than the ones shown in the ISO T/R 7637/1 table.

**µC I/Os PROTECTION:**

If a ground protection network is used and negative transient are present on the V<sub>CC</sub> line, the control pins will be pulled negative. ST suggests to insert a resistor (R<sub>prot</sub>) in line to prevent the µC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of µC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of µC I/Os.

$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OHµC} - V_{IH} - V_{GND}) / I_{IHmax}$$

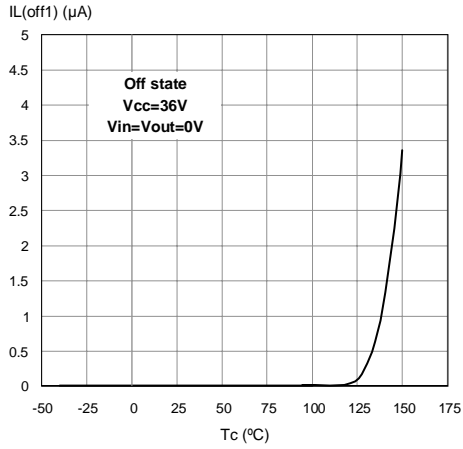
Calculation example:

For V<sub>CCpeak</sub> = -100V and I<sub>latchup</sub> ≥ 20mA; V<sub>OHµC</sub> ≥ 4.5V  
 $5k\Omega \leq R_{prot} \leq 65k\Omega$ .

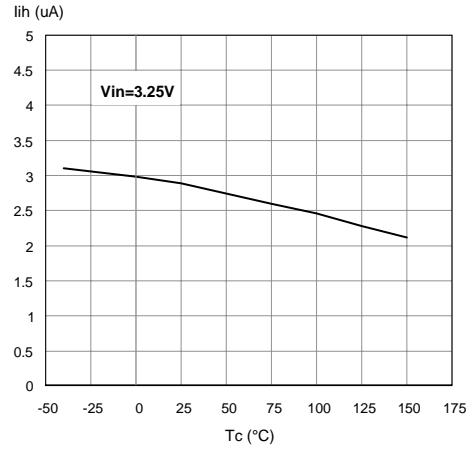
Recommended R<sub>prot</sub> value is 10kΩ.



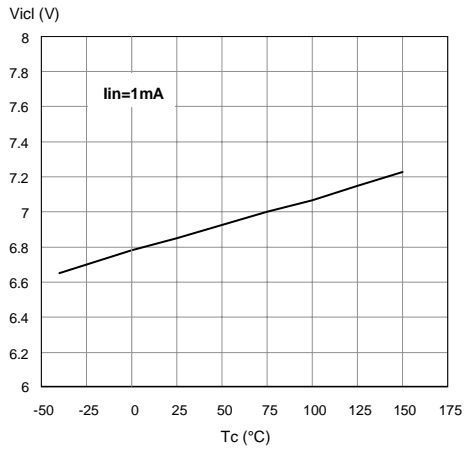
Off State Output Current



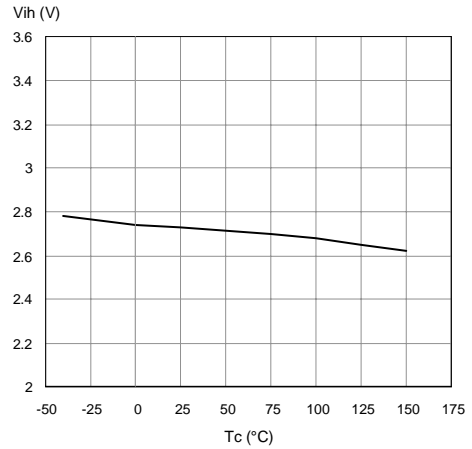
High Level Input Current



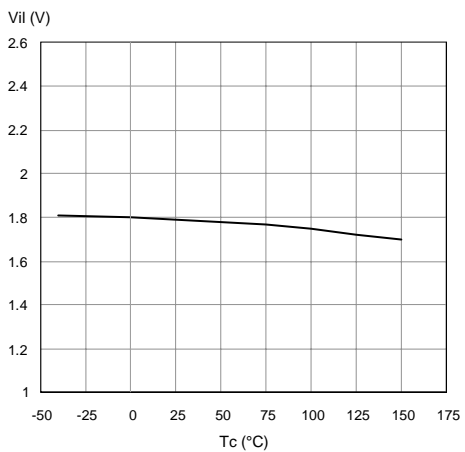
Input Clamp Voltage



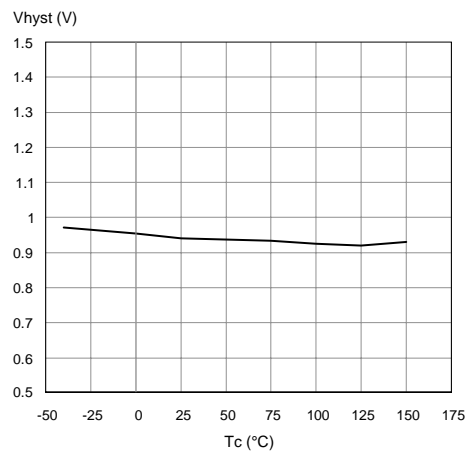
Input High Level



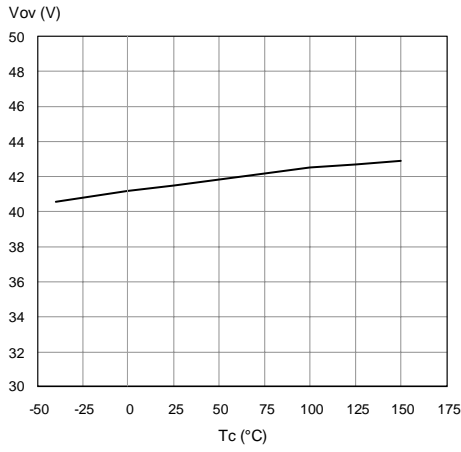
Input Low Level



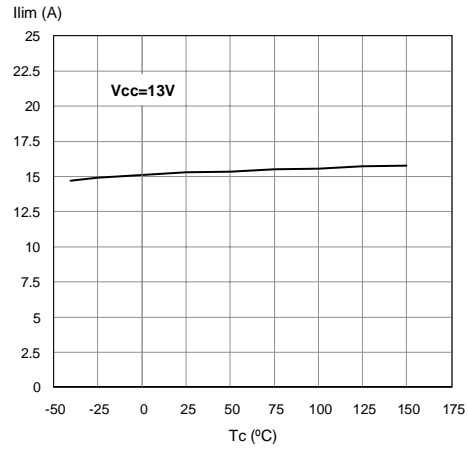
Input Hysteresis Voltage



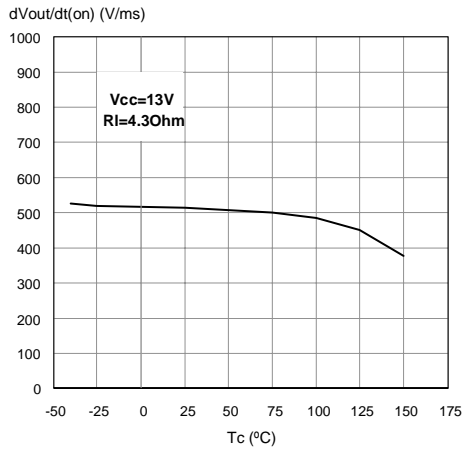
Overvoltage Shutdown



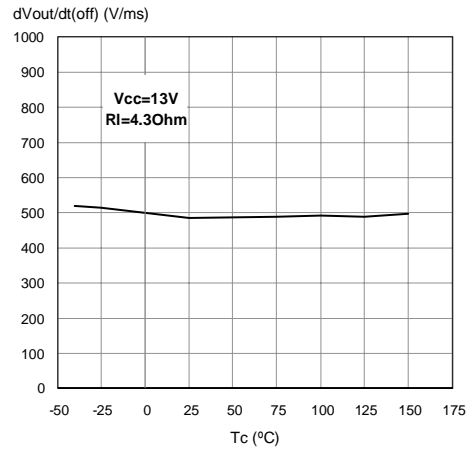
I<sub>LIM</sub> Vs T<sub>case</sub>



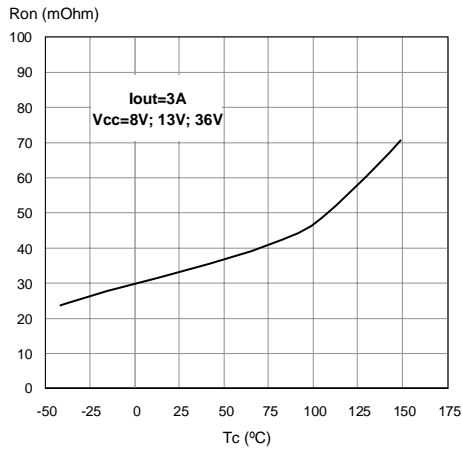
Turn-on Voltage Slope



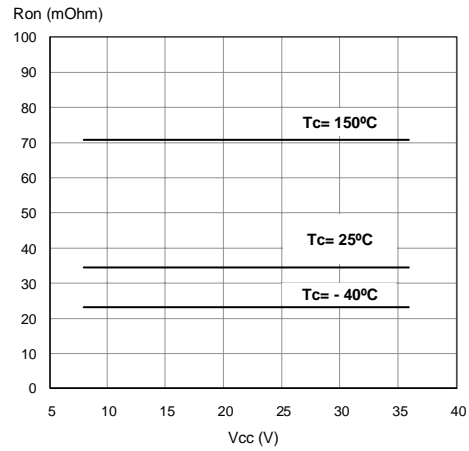
Turn-off Voltage Slope



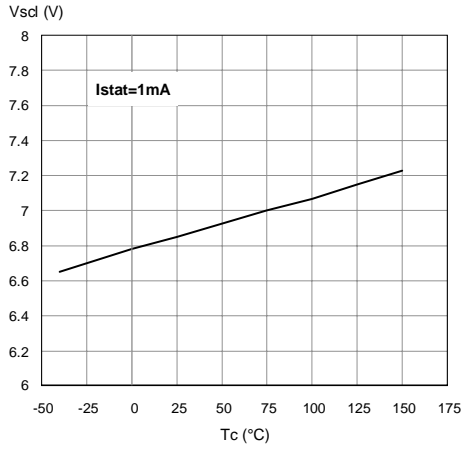
On State Resistance Vs T<sub>case</sub>



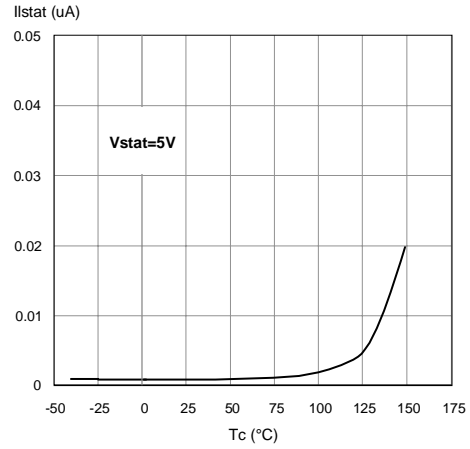
On State Resistance Vs V<sub>CC</sub>



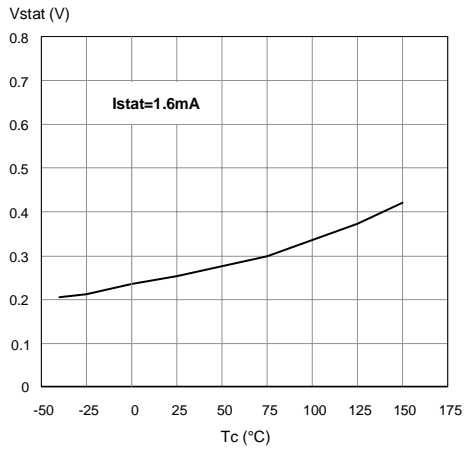
Status Clamp Voltage



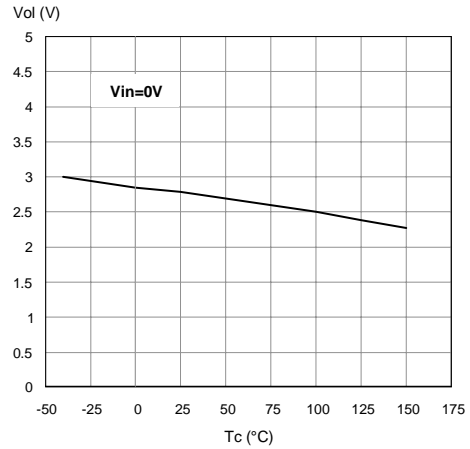
Status Leakage Current



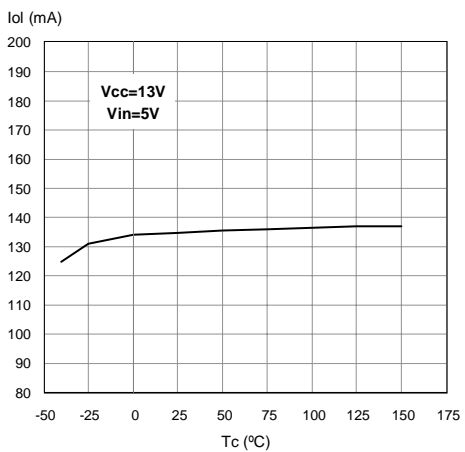
Status Low Output Voltage



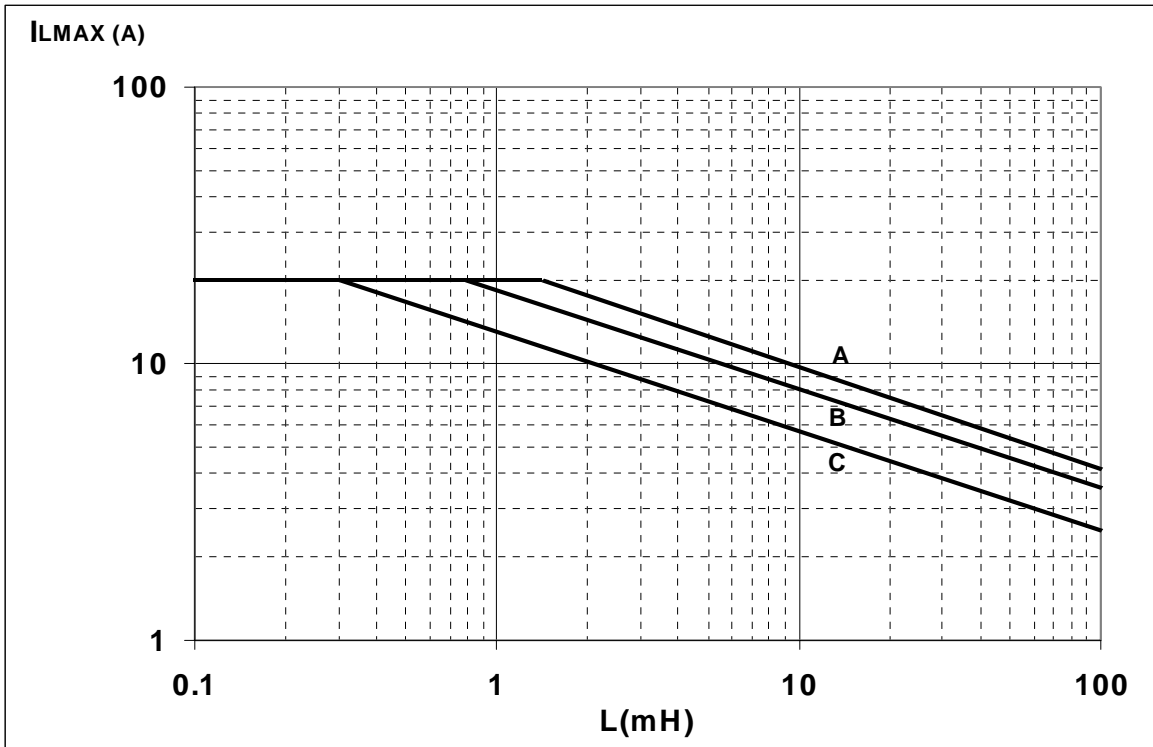
Open Load Off State Voltage Detection Threshold



Open Load On State Detection Threshold



PowerSO-10, P<sup>2</sup>PAK, PENTAWATT Maximum turn off current versus load inductance



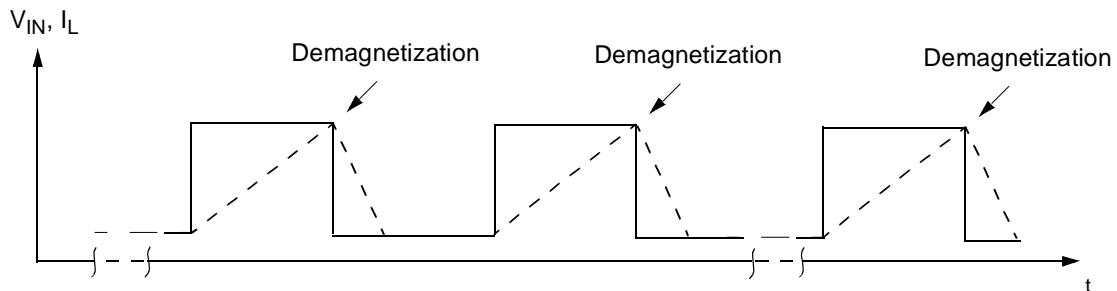
- A = Single Pulse at  $T_{Jstart}=150^{\circ}C$
- B = Repetitive pulse at  $T_{Jstart}=100^{\circ}C$
- C = Repetitive Pulse at  $T_{Jstart}=125^{\circ}C$

Conditions:

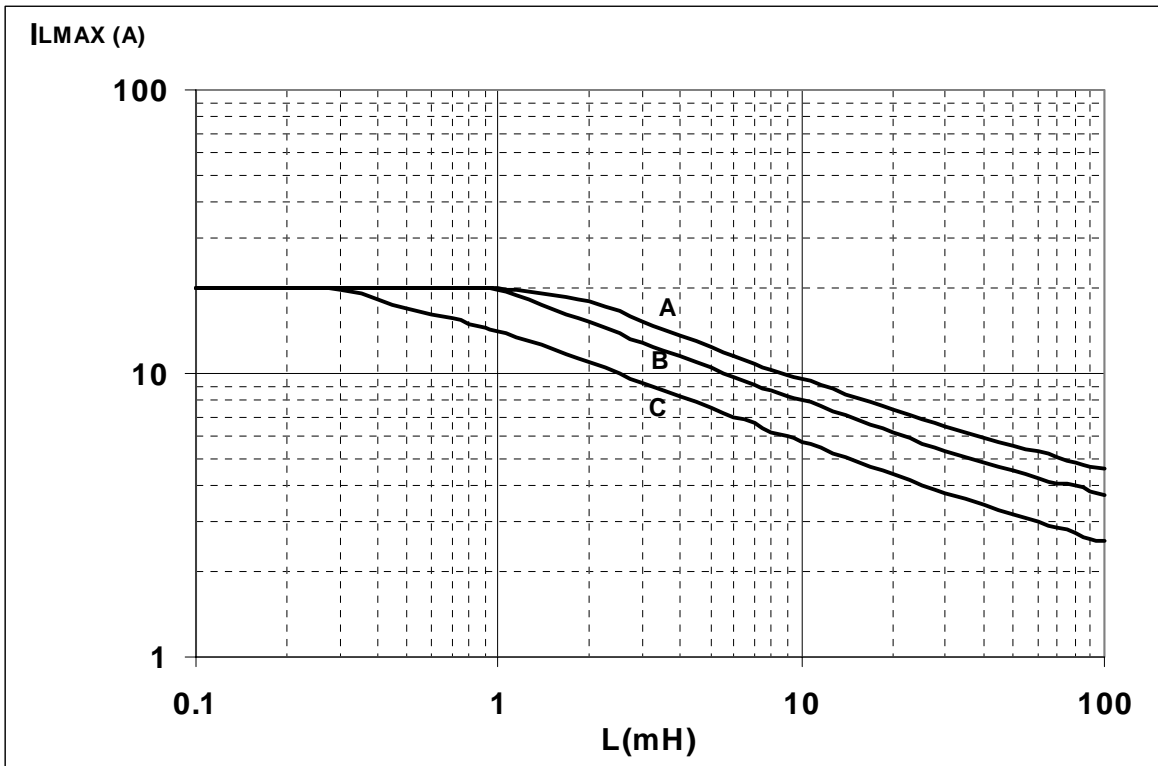
$V_{CC}=13.5V$

Values are generated with  $R_L=0\Omega$

In case of repetitive pulses,  $T_{jstart}$  (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.



PPAK Maximum turn off current versus load inductance



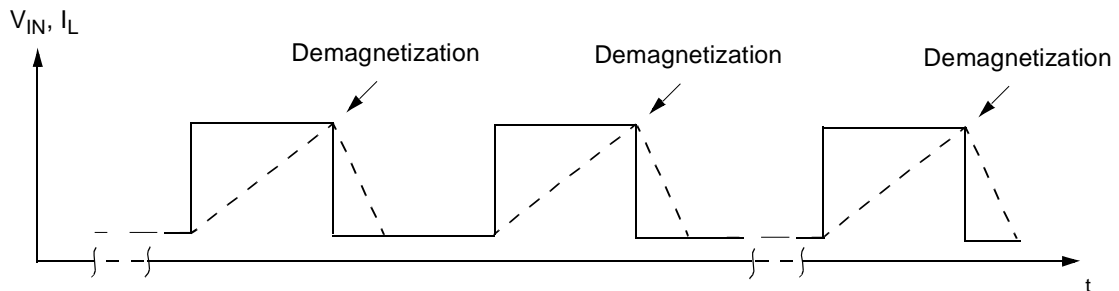
- A = Single Pulse at  $T_{Jstart} = 150^\circ\text{C}$
- B = Repetitive pulse at  $T_{Jstart} = 100^\circ\text{C}$
- C = Repetitive Pulse at  $T_{Jstart} = 125^\circ\text{C}$

Conditions:

$V_{CC} = 13.5\text{V}$

Values are generated with  $R_L = 0\Omega$

In case of repetitive pulses,  $T_{Jstart}$  (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.



SO-16L Maximum turn off current versus load inductance



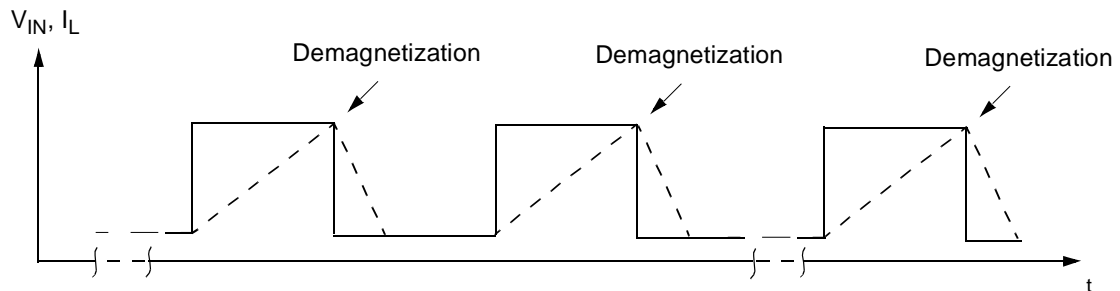
- A = Single Pulse at  $T_{Jstart}=150^{\circ}C$
- B = Repetitive pulse at  $T_{Jstart}=100^{\circ}C$
- C = Repetitive Pulse at  $T_{Jstart}=125^{\circ}C$

Conditions:

$V_{CC}=13.5V$

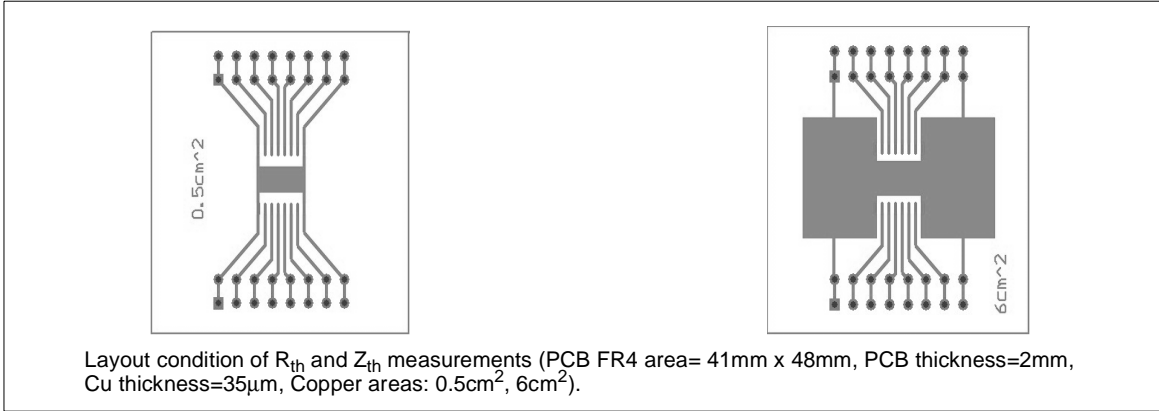
Values are generated with  $R_L=0\Omega$

In case of repetitive pulses,  $T_{jstart}$  (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

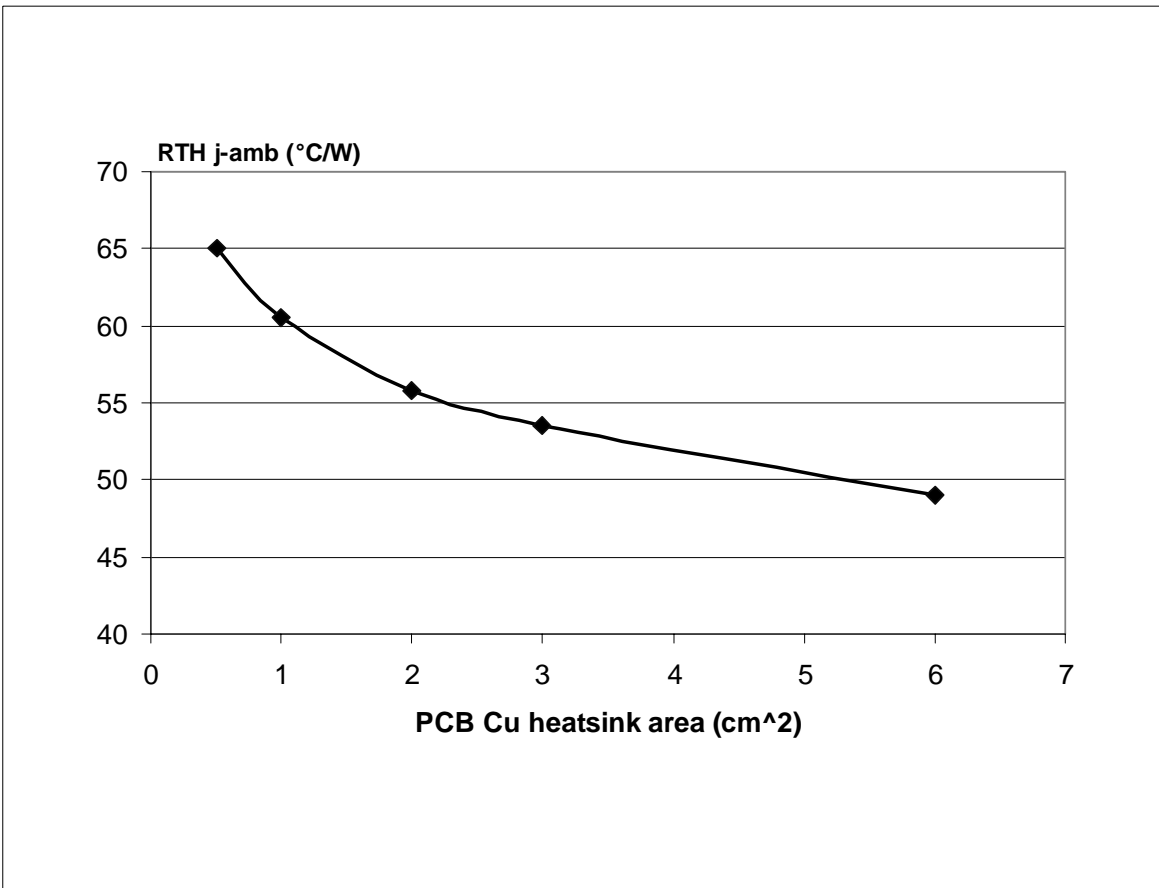


**SO-16L THERMAL DATA**

**SO-16L PC Board**



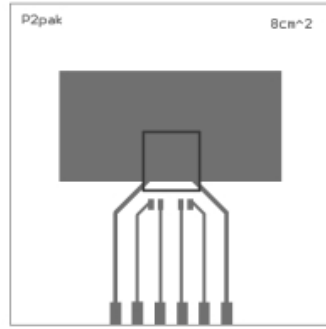
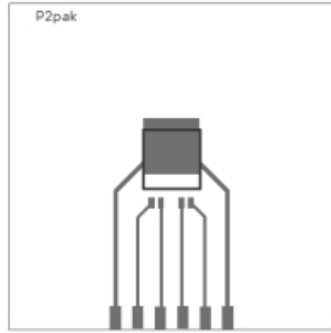
**$R_{thj-amb}$  Vs PCB copper area in open box free air condition**





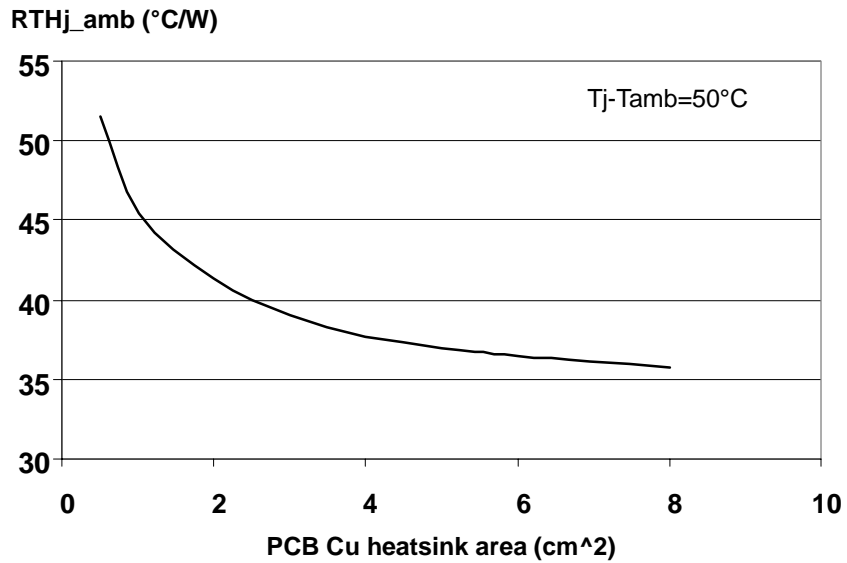
**P<sup>2</sup>PAK THERMAL DATA**

**P<sup>2</sup>PAK PC Board**



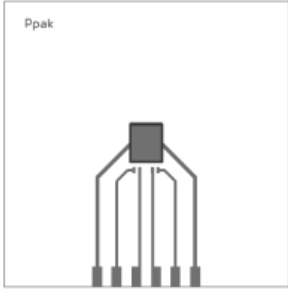
Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB FR4 area= 60mm x 60mm, PCB thickness=2mm, Cu thickness=35 $\mu$ m, Copper areas: 0.97cm<sup>2</sup>, 8cm<sup>2</sup>).

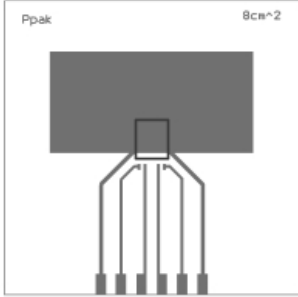
**$R_{thj-amb}$  Vs PCB copper area in open box free air condition**



**PPAK THERMAL DATA**

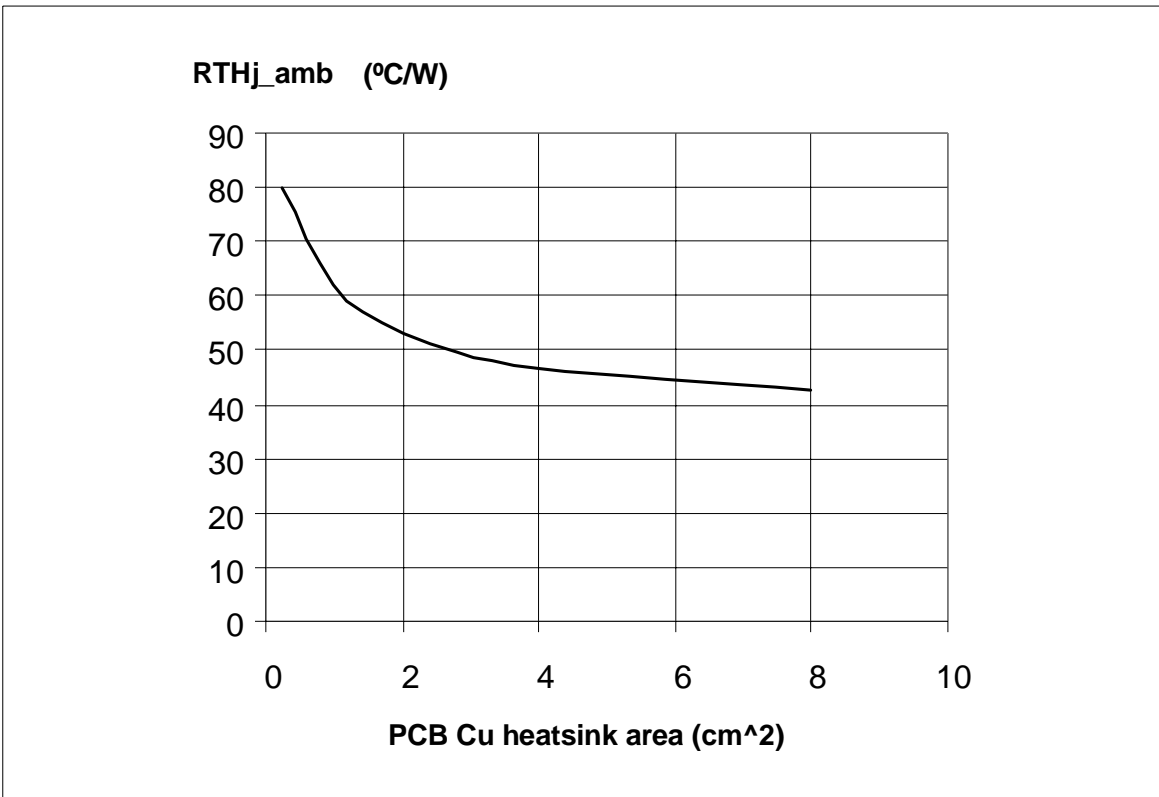
**PPAK PC Board**





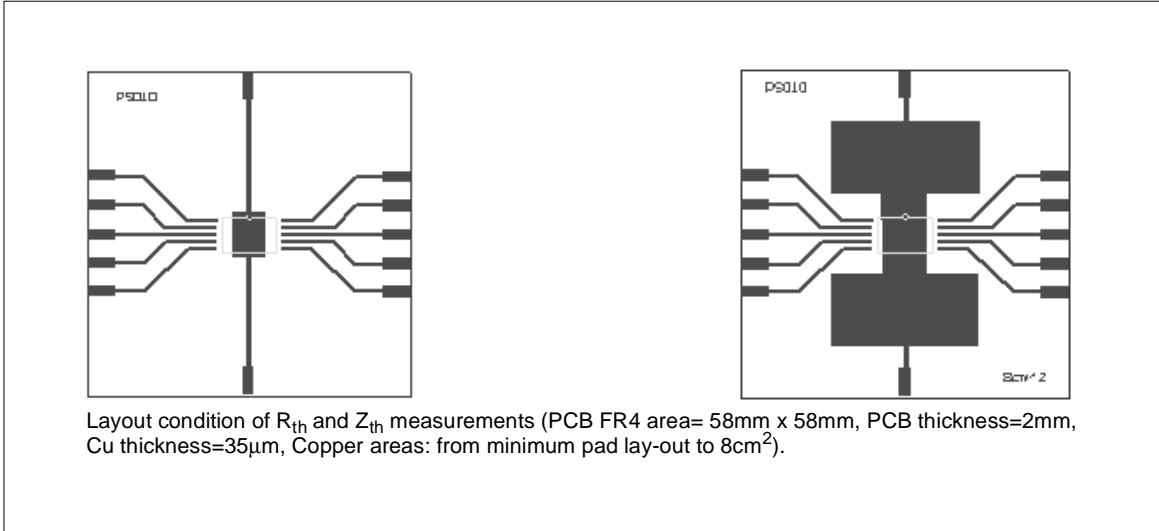
Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB FR4 area= 60mm x 60mm, PCB thickness=2mm, Cu thickness=35 $\mu$ m, Copper areas: 0.44cm<sup>2</sup>, 8cm<sup>2</sup>).

**$R_{thj-amb}$  Vs PCB copper area in open box free air condition**

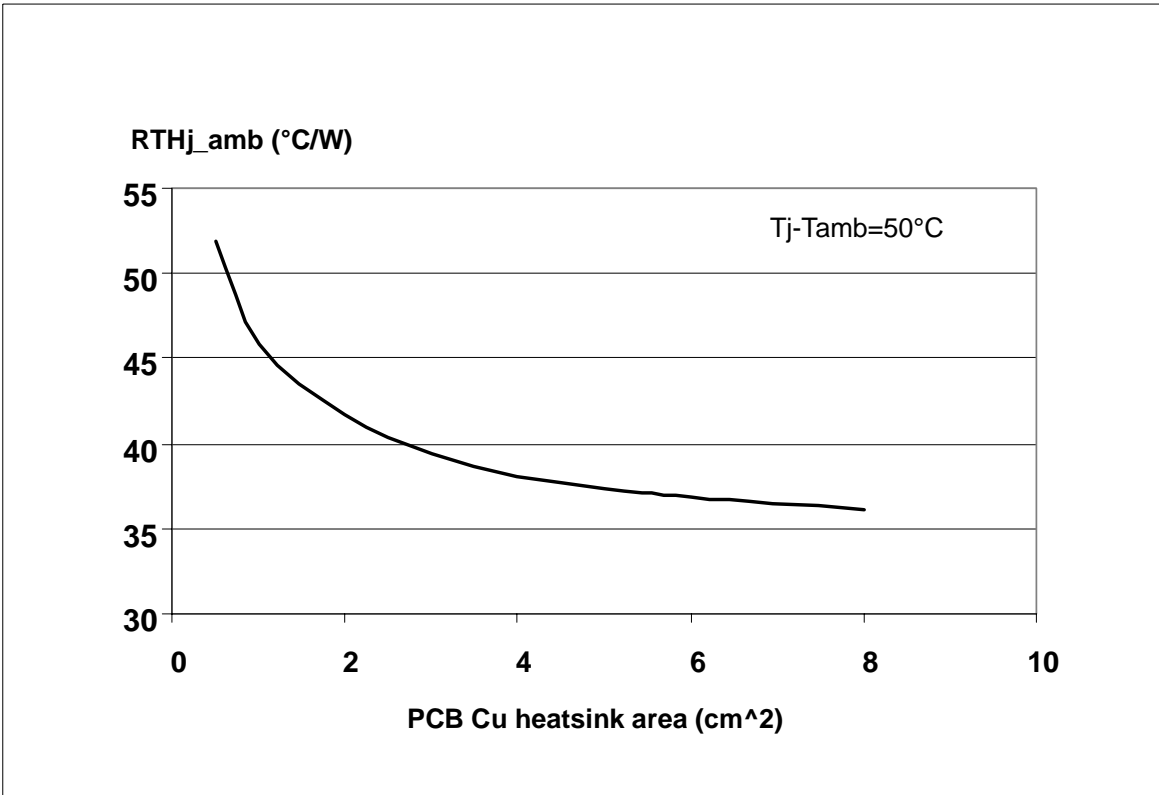


**PowerSO-10™ THERMAL DATA**

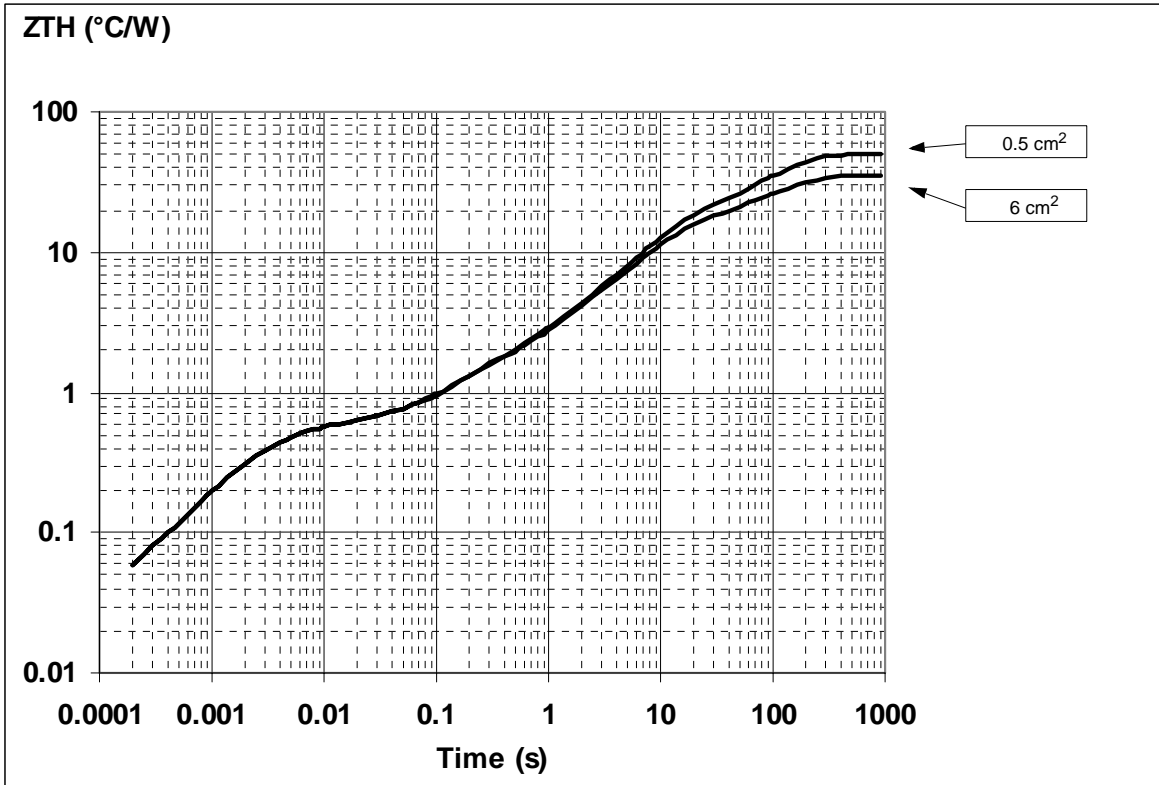
**PowerSO-10™ PC Board**



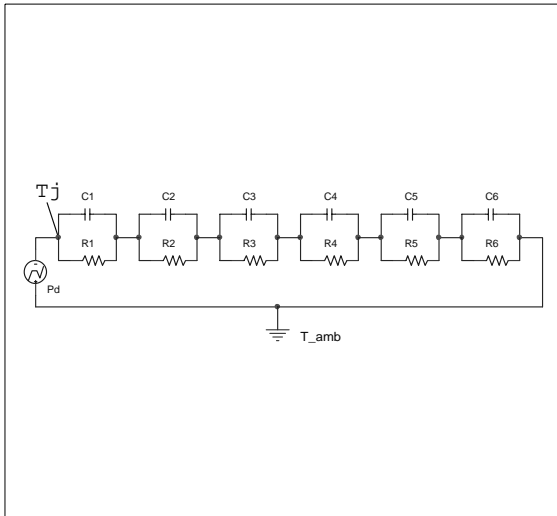
**$R_{thj-amb}$  Vs PCB copper area in open box free air condition**



PowerSO-10 Thermal Impedance Junction Ambient Single Pulse



Thermal fitting model of a single channel HSD in PowerSO-10



Pulse calculation formula

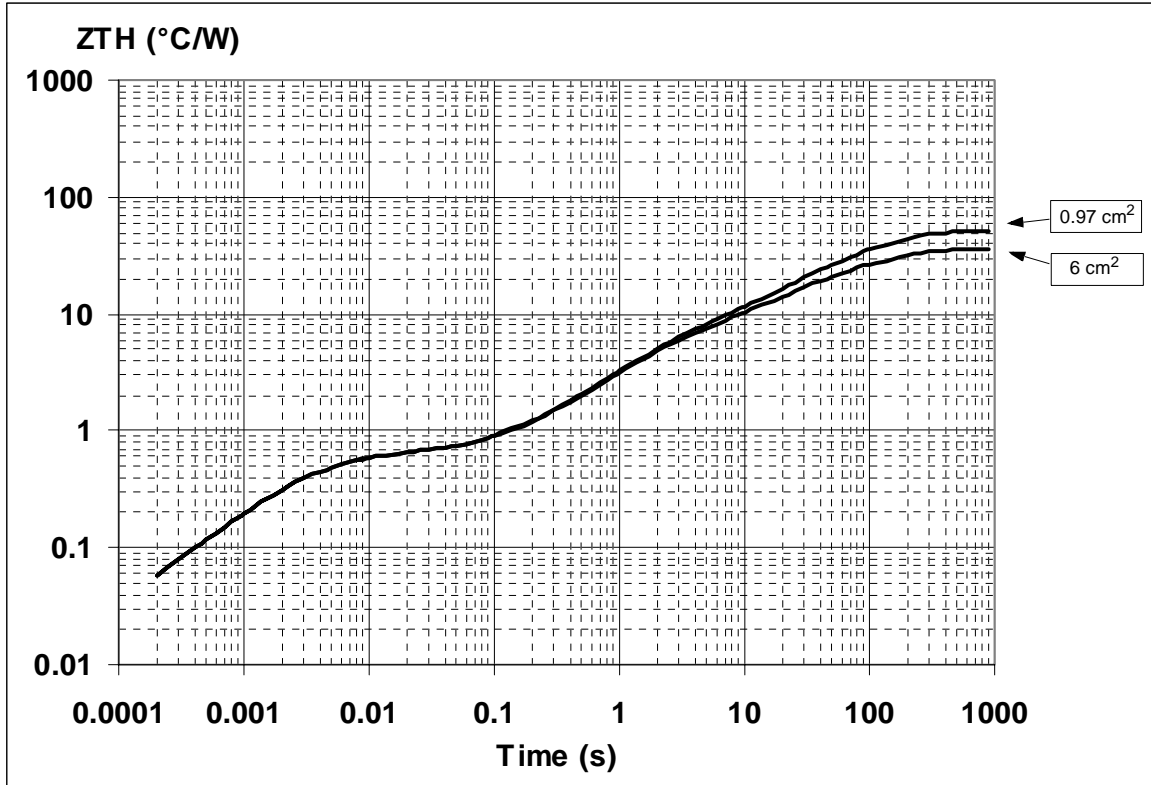
$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

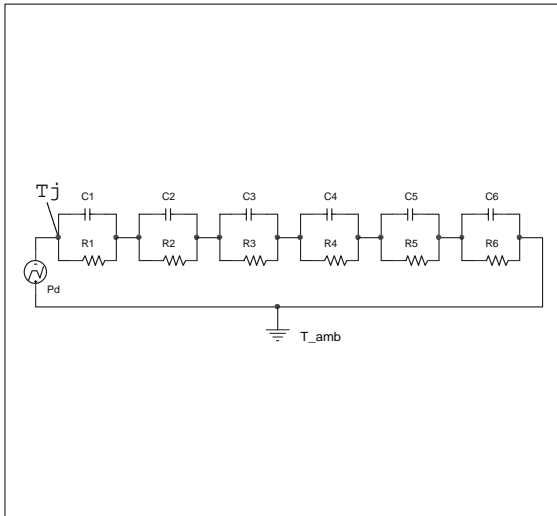
Thermal Parameter

Area/island (cm <sup>2</sup> )	0.5	6
R1 (°C/W)	0.04	
R2 (°C/W)	0.25	
R3 (°C/W)	0.25	
R4 (°C/W)	0.8	
R5 (°C/W)	12	
R6 (°C/W)	37	22
C1 (W.s/°C)	0.0008	
C2 (W.s/°C)	7.00E-03	
C3 (W.s/°C)	0.015	
C4 (W.s/°C)	0.3	
C5 (W.s/°C)	0.75	
C6 (W.s/°C)	3	5

P<sup>2</sup>PAK Thermal Impedance Junction Ambient Single Pulse



Thermal fitting model of a single channel HSD in P<sup>2</sup>PAK



Pulse calculation formula

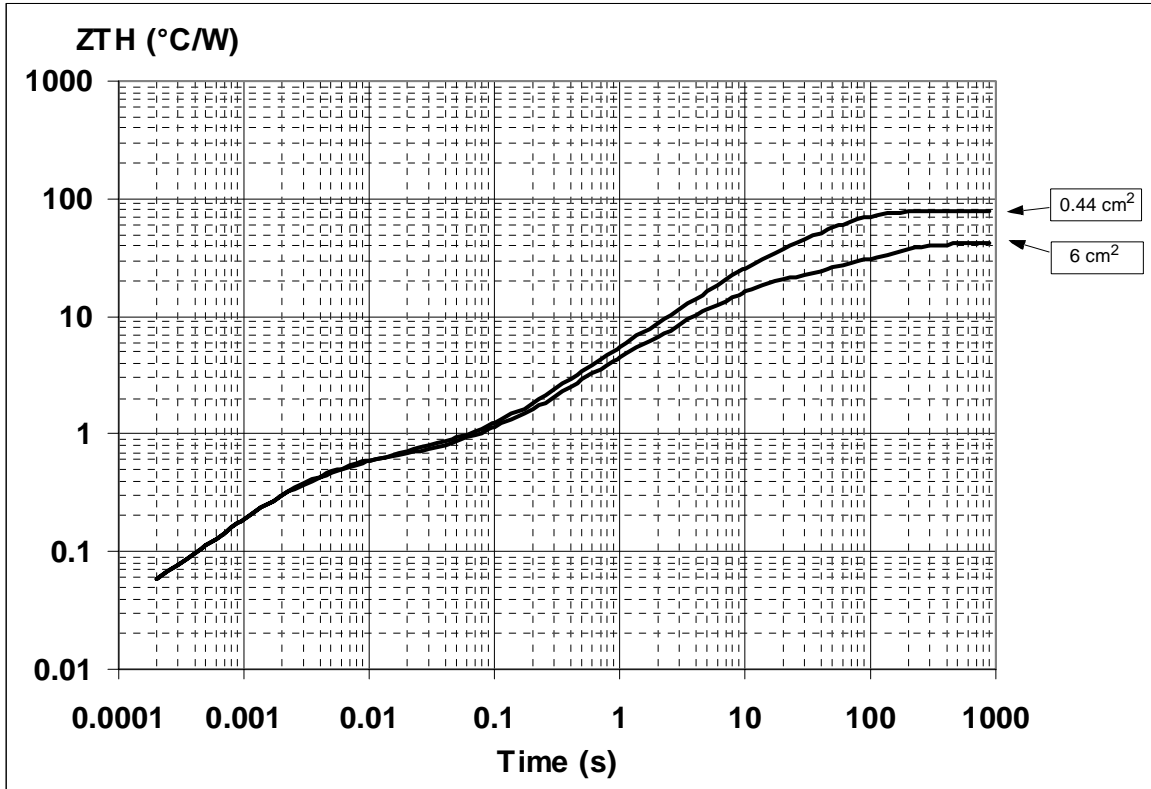
$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

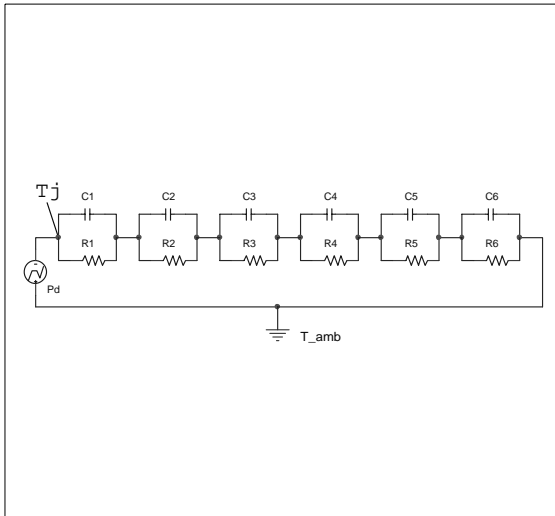
Thermal Parameter

Area/island (cm <sup>2</sup> )	0.97	6
R1 (°C/W)	0.04	
R2 (°C/W)	0.25	
R3 (°C/W)	0.3	
R4 (°C/W)	4	
R5 (°C/W)	9	
R6 (°C/W)	37	22
C1 (W.s/°C)	0.0008	
C2 (W.s/°C)	0.007	
C3 (W.s/°C)	0.015	
C4 (W.s/°C)	0.4	
C5 (W.s/°C)	2	
C6 (W.s/°C)	3	5

PPAK Thermal Impedance Junction Ambient Single Pulse



Thermal fitting model of a single channel HSD in PPAK



Pulse calculation formula

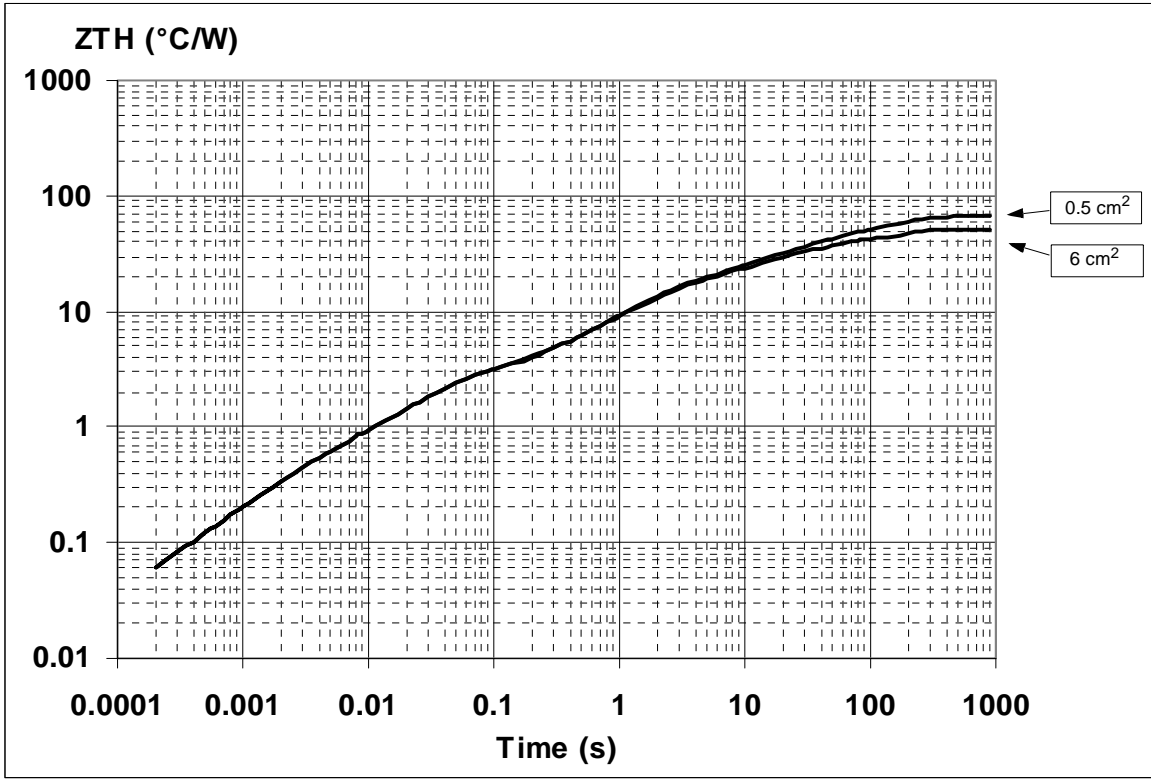
$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

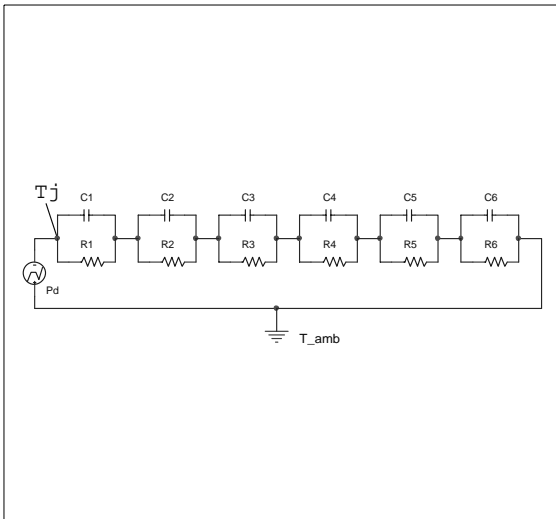
Thermal Parameter

Area/island (cm <sup>2</sup> )	0.44	6
R1 (°C/W)	0.04	
R2 (°C/W)	0.25	
R3 (°C/W)	0.3	
R4 (°C/W)	2	
R5 (°C/W)	15	
R6 (°C/W)	61	24
C1 (W.s/°C)	0.0008	
C2 (W.s/°C)	0.007	
C3 (W.s/°C)	0.02	
C4 (W.s/°C)	0.3	
C5 (W.s/°C)	0.45	
C6 (W.s/°C)	0.8	5

SO-16L Thermal Impedance Junction Ambient Single Pulse



Thermal fitting model of a single channel HSD in SO-16L



Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

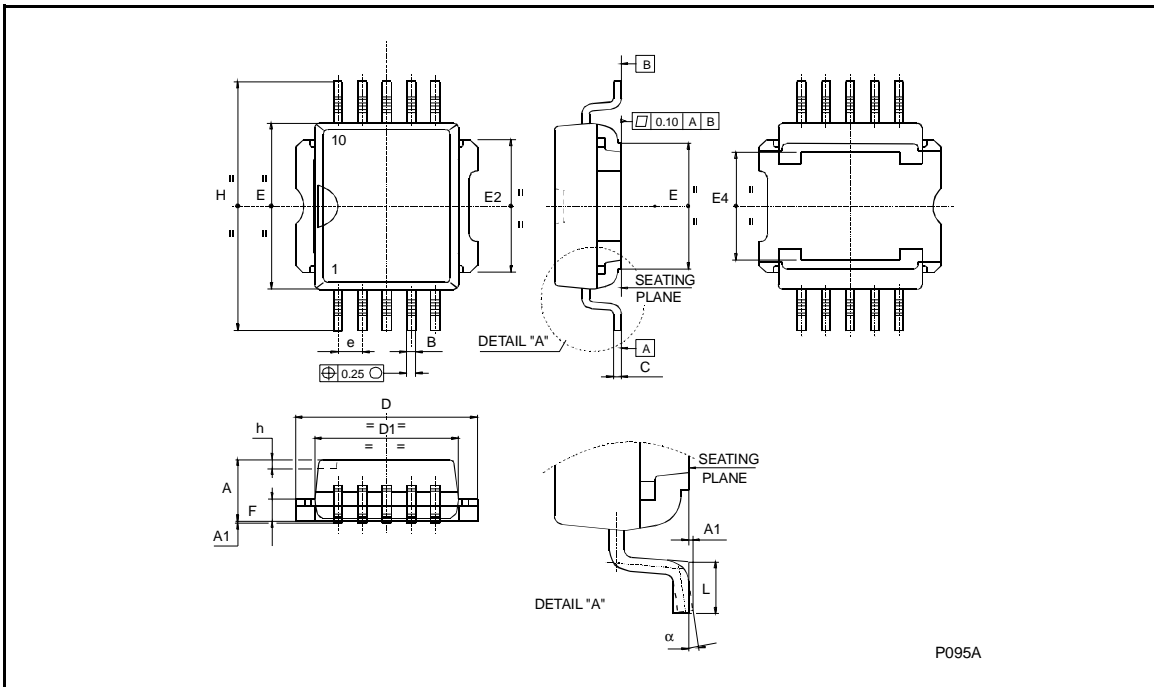
Thermal Parameter

Area/island (cm <sup>2</sup> )	0.5	6
R1 (°C/W)	0.04	
R2 (°C/W)	0.25	
R3 (°C/W)	2.2	
R4 (°C/W)	12	
R5 (°C/W)	15	
R6 (°C/W)	37	22
C1 (W.s/°C)	0.0008	
C2 (W.s/°C)	7.00E-03	
C3 (W.s/°C)	1.50E-02	
C4 (W.s/°C)	0.14	
C5 (W.s/°C)	1	
C6 (W.s/°C)	3	5

**PowerSO-10™ MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	3.35		3.65	0.132		0.144
A (*)	3.4		3.6	0.134		0.142
A1	0.00		0.10	0.000		0.004
B	0.40		0.60	0.016		0.024
B (*)	0.37		0.53	0.014		0.021
C	0.35		0.55	0.013		0.022
C (*)	0.23		0.32	0.009		0.0126
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.300
E	9.30		9.50	0.366		0.374
E2	7.20		7.60	0.283		300
E2 (*)	7.30		7.50	0.287		0.295
E4	5.90		6.10	0.232		0.240
E4 (*)	5.90		6.30	0.232		0.248
e		1.27			0.050	
F	1.25		1.35	0.049		0.053
F (*)	1.20		1.40	0.047		0.055
H	13.80		14.40	0.543		0.567
H (*)	13.85		14.35	0.545		0.565
h		0.50			0.002	
L	1.20		1.80	0.047		0.070
L (*)	0.80		1.10	0.031		0.043
α	0°		8°	0°		8°
α (*)	2°		8°	2°		8°

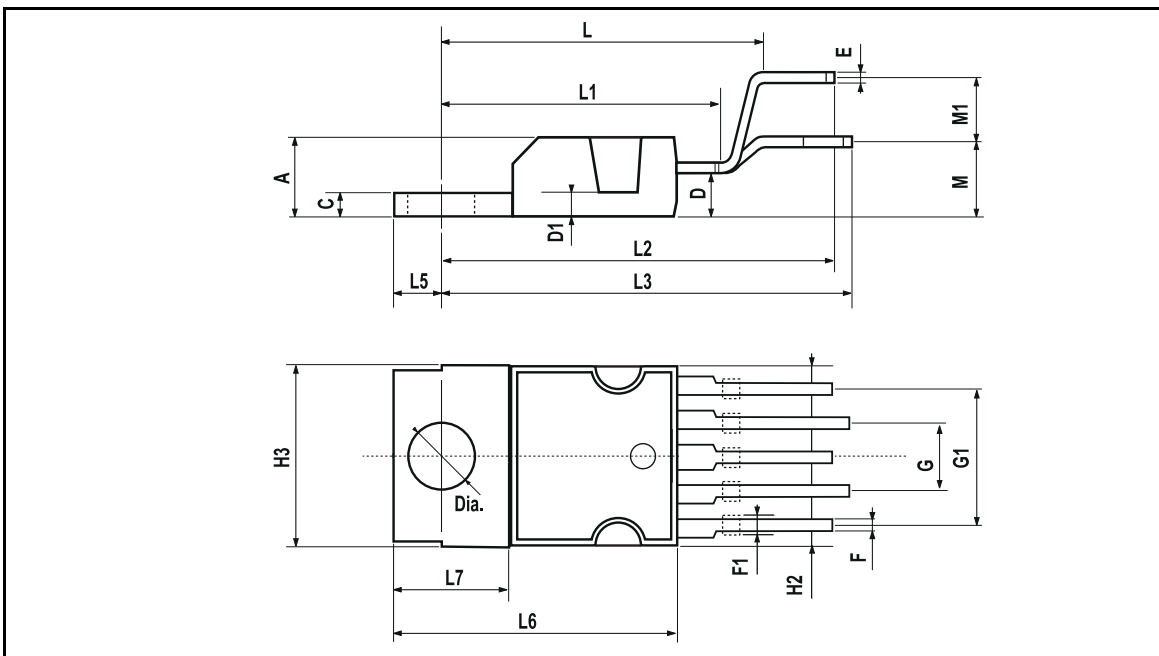
(\*) Muar only POA P013P





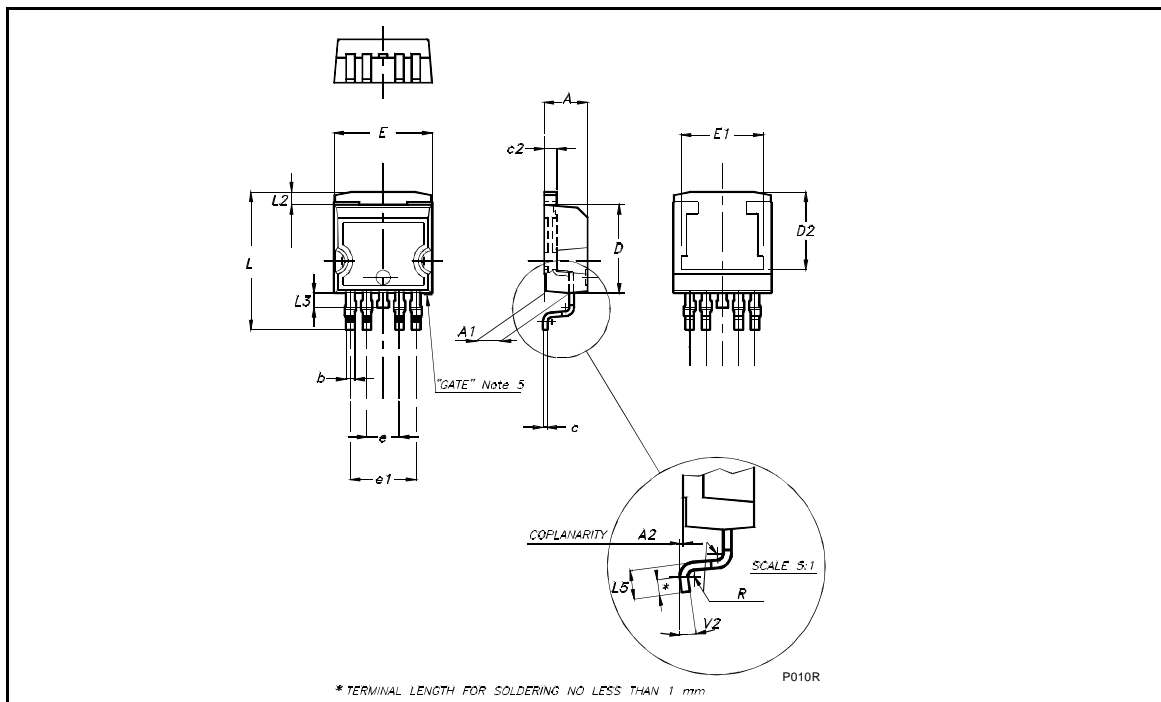
**PENTAWATT (VERTICAL) MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.8		1.05	0.031		0.041
F1	1		1.4	0.039		0.055
G	3.2	3.4	3.6	0.126	0.134	0.142
G1	6.6	6.8	7	0.260	0.268	0.276
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L		17.85			0.703	
L1		15.75			0.620	
L2		21.4			0.843	
L3		22.5			0.886	
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
M		4.5			0.177	
M1		4			0.157	
Diam.	3.65		3.85	0.144		0.152



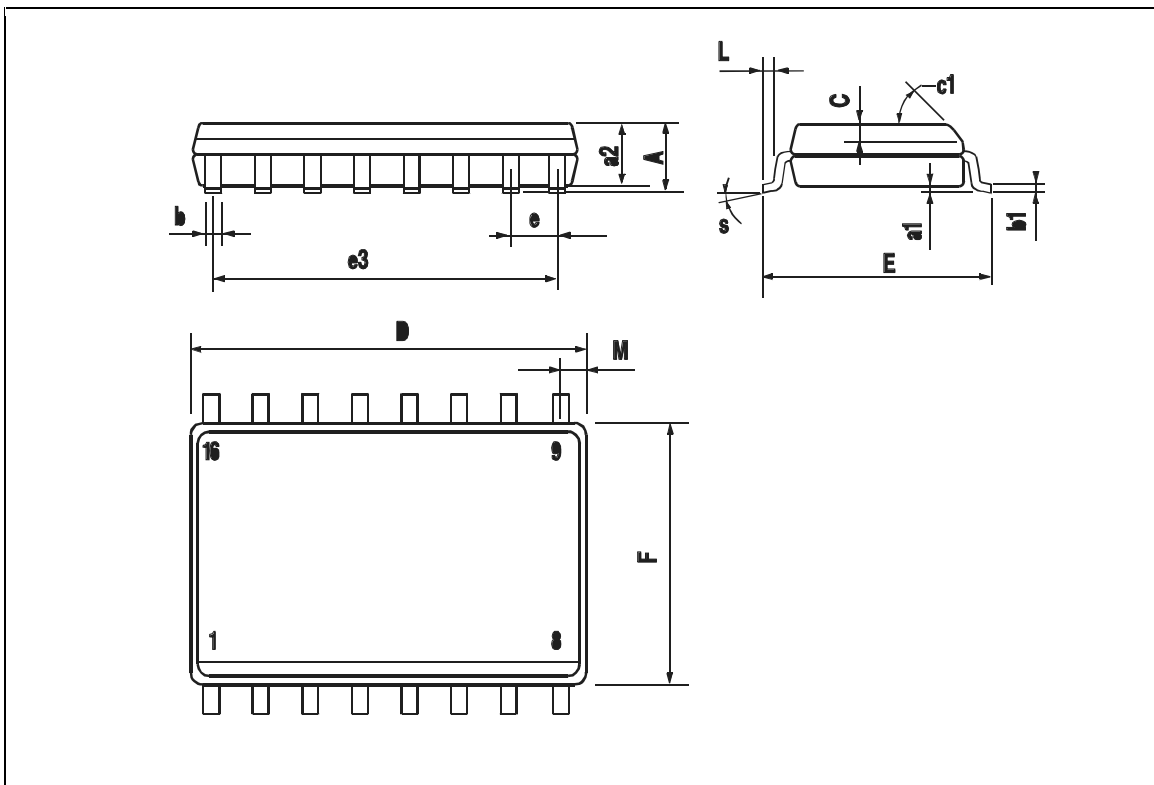
## P<sup>2</sup>PAK MECHANICAL DATA

DIM.	mm.		
	MIN.	TYP	MAX.
A	4.30		4.80
A1	2.40		2.80
A2	0.03		0.23
b	0.80		1.05
c	0.45		0.60
c2	1.17		1.37
D	8.95		9.35
D2		8.00	
E	10.00		10.40
E1		8.50	
e	3.20		3.60
e1	6.60		7.00
L	13.70		14.50
L2	1.25		1.40
L3	0.90		1.70
L5	1.55		2.40
R		0.40	
V2	0°		8°
Package Weight	1.40 Gr (typ)		



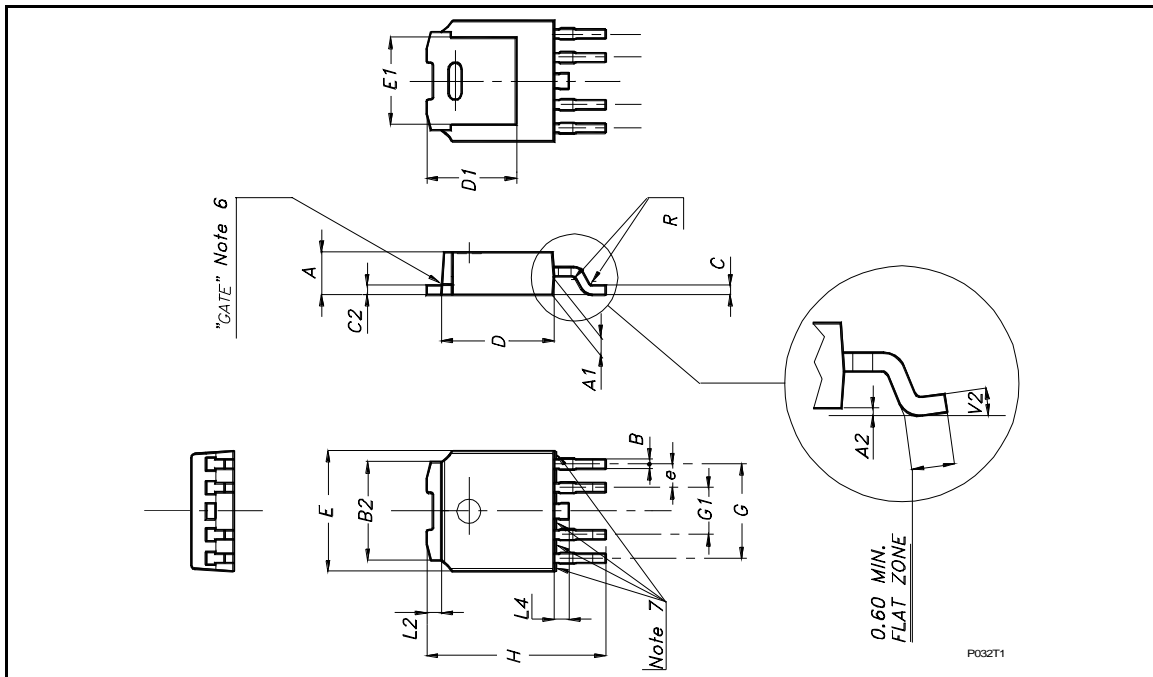
**SO-16L MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45° (typ.)					
D	10.1		10.5	0.397		0.413
E	10.0		10.65	0.393		0.419
e		1.27			0.050	
e3		8.89			0.350	
F	7.4		7.6	0.291		0.300
L	0.5		1.27	0.020		0.050
M			0.75			0.029
S	8° (max.)					

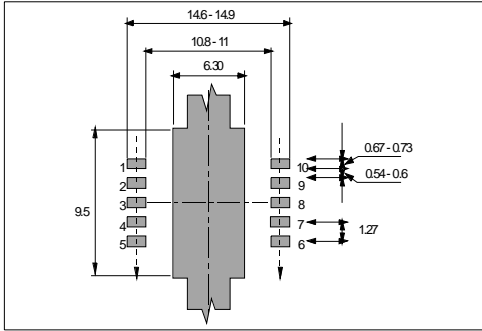


**PPAK MECHANICAL DATA**

DIM.	MIN.	TYP	MAX.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
B	0.40		0.60
B2	5.20		5.40
C	0.45		0.60
C2	0.48		0.60
D1		5.1	
D	6.00		6.20
E	6.40		6.60
E1		4.7	
e		1.27	
G	4.90		5.25
G1	2.38		2.70
H	9.35		10.10
L2		0.8	1.00
L4	0.60		1.00
R		0.2	
V2	0°		8°
Package Weight	Gr. 0.3		



**PowerSO-10™ SUGGESTED PAD LAYOUT**



**TUBE SHIPMENT (no suffix)**

All dimensions are in mm.

	Base Q.ty	Bulk Q.ty	Tube length (± 0.5)	A	B	C (± 0.1)
<b>Casablanca</b>	50	1000	532	10.4	16.4	0.8
<b>Muar</b>	50	1000	532	4.9	17.2	0.8

**TAPE AND REEL SHIPMENT (suffix "13TR")**

**REEL DIMENSIONS**

Base Q.ty	600
Bulk Q.ty	600
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	60
T (max)	30.4

All dimensions are in mm.

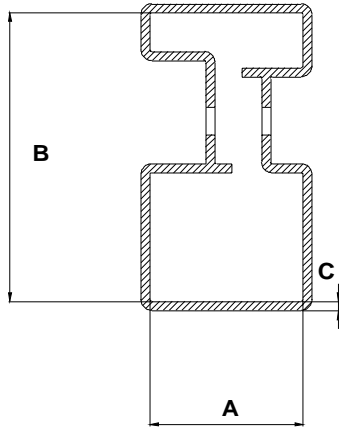
**TAPE DIMENSIONS**  
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	W	24
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	24
Hole Diameter	D (± 0.1/-0)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.05)	11.5
Compartment Depth	K (max)	6.5
Hole Spacing	P1 (± 0.1)	2

All dimensions are in mm.

User Direction of Feed

**PENTAWATT TUBE SHIPMENT (no suffix)**

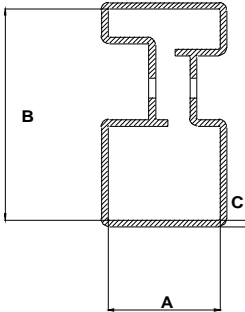


<b>Base Q.ty</b>	50
<b>Bulk Q.ty</b>	1000
<b>Tube length (<math>\pm 0.5</math>)</b>	532
<b>A</b>	18
<b>B</b>	33.1
<b>C (<math>\pm 0.1</math>)</b>	1

All dimensions are in mm.

VN820 / VN820SO / VN820SP / VN820-B5 / VN820PT

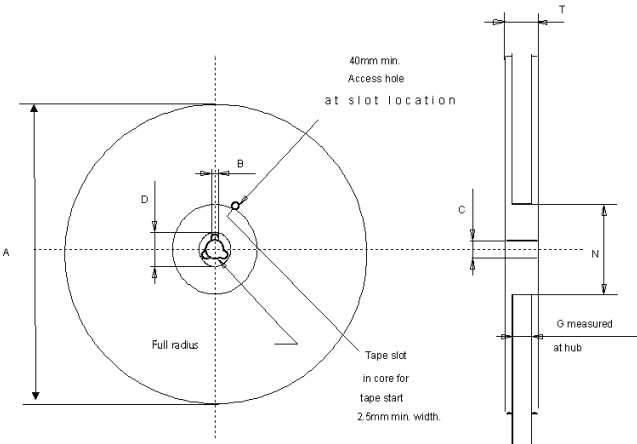
P<sup>2</sup>PAK TUBE SHIPMENT (no suffix)



Base Q.ty	50
Bulk Q.ty	1000
Tube length (± 0.5)	532
A	18
B	33.1
C (± 0.1)	1

All dimensions are in mm.

TAPE AND REEL SHIPMENT (suffix "13TR")



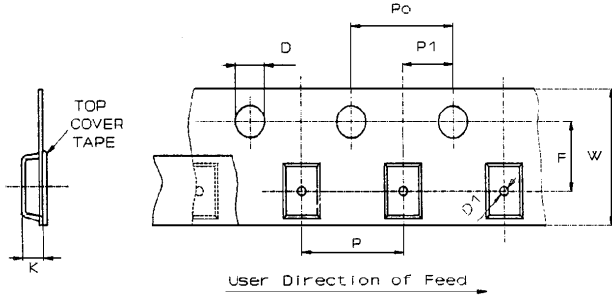
Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	60
T (max)	30.4

All dimensions are in mm.

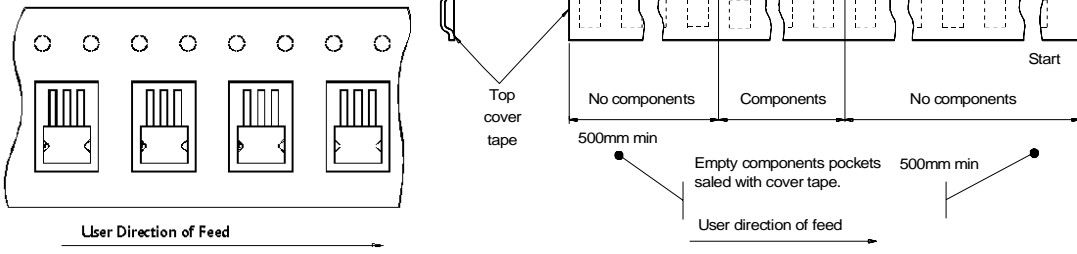
**TAPE DIMENSIONS**

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

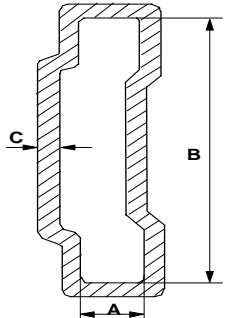
Tape width	W	24
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	16
Hole Diameter	D (± 0.1/-0)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.05)	11.5
Compartment Depth	K (max)	6.5
Hole Spacing	P1 (± 0.1)	2



All dimensions are in mm.



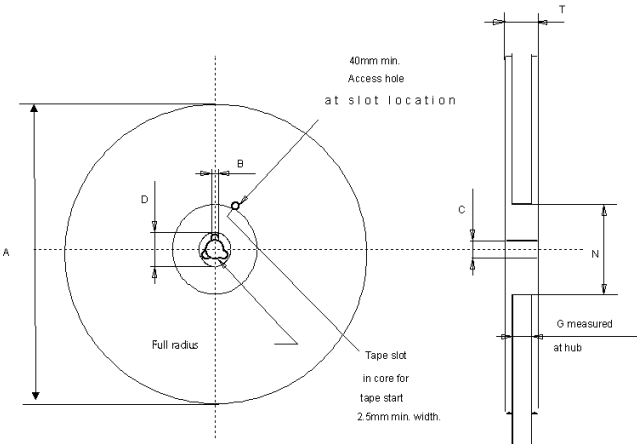
**SO-16L TUBE SHIPMENT (no suffix)**



<b>Base Q.ty</b>	50
<b>Bulk Q.ty</b>	1000
<b>Tube length (± 0.5)</b>	532
<b>A</b>	3.5
<b>B</b>	13.8
<b>C (± 0.1)</b>	0.6

All dimensions are in mm.

**TAPE AND REEL SHIPMENT (suffix "13TR")**



<b>Base Q.ty</b>	1000
<b>Bulk Q.ty</b>	1000
<b>A (max)</b>	330
<b>B (min)</b>	1.5
<b>C (± 0.2)</b>	13
<b>F</b>	20.2
<b>G (+ 2 / -0)</b>	16.4
<b>N (min)</b>	60
<b>T (max)</b>	22.4

40mm min. Access hole at slot location

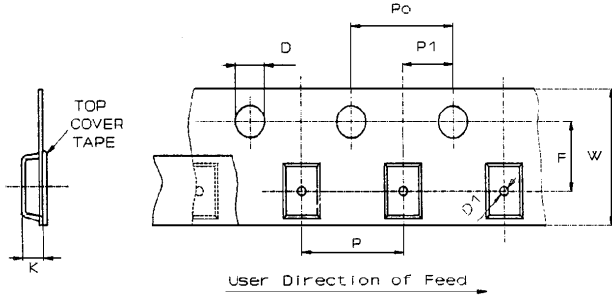
Tape slot in core for tape start 2.5mm min. width.

G measured at hub

**TAPE DIMENSIONS**

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

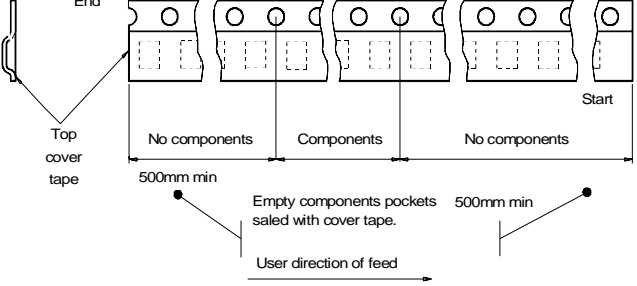
<b>Tape width</b>	<b>W</b>	16
<b>Tape Hole Spacing</b>	<b>P0 (± 0.1)</b>	4
<b>Component Spacing</b>	<b>P</b>	12
<b>Hole Diameter</b>	<b>D (± 0.1/-0)</b>	1.5
<b>Hole Diameter</b>	<b>D1 (min)</b>	1.5
<b>Hole Position</b>	<b>F (± 0.05)</b>	7.5
<b>Compartment Depth</b>	<b>K (max)</b>	6.5
<b>Hole Spacing</b>	<b>P1 (± 0.1)</b>	2



TOP COVER TAPE

User Direction of Feed

All dimensions are in mm.



User Direction of Feed

500mm min

Empty components pockets sealed with cover tape.

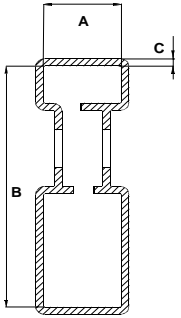
500mm min

User direction of feed



VN820 / VN820SO / VN820SP / VN820-B5 / VN820PT

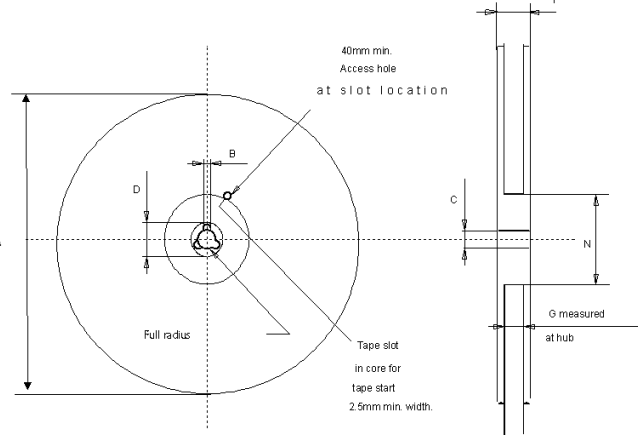
PPAK TUBE SHIPMENT (no suffix)



<b>Base Q.ty</b>	75
<b>Bulk Q.ty</b>	3000
<b>Tube length (<math>\pm 0.5</math>)</b>	532
<b>A</b>	6
<b>B</b>	21.3
<b>C (<math>\pm 0.1</math>)</b>	0.6

All dimensions are in mm.

TAPE AND REEL SHIPMENT (suffix "13TR")



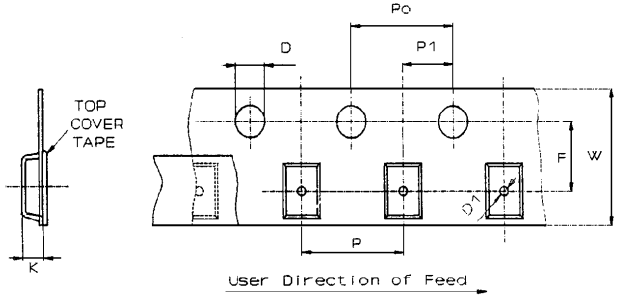
<b>Base Q.ty</b>	2500
<b>Bulk Q.ty</b>	2500
<b>A (max)</b>	330
<b>B (min)</b>	1.5
<b>C (<math>\pm 0.2</math>)</b>	13
<b>F</b>	20.2
<b>G (+ 2 / -0)</b>	16.4
<b>N (min)</b>	60
<b>T (max)</b>	22.4

All dimensions are in mm.

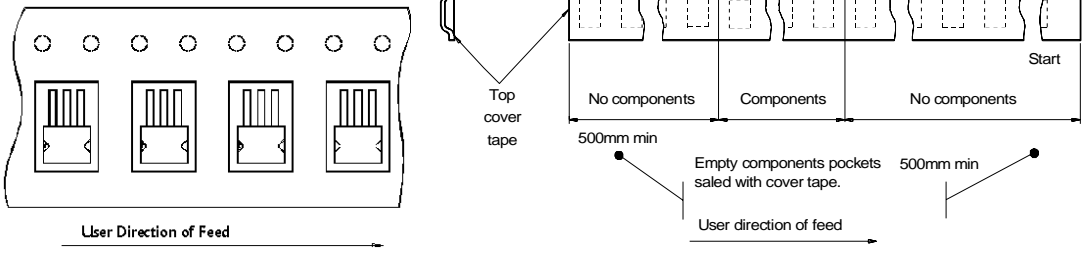
**TAPE DIMENSIONS**

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

<b>Tape width</b>	<b>W</b>	16
<b>Tape Hole Spacing</b>	<b>P0 (<math>\pm 0.1</math>)</b>	4
<b>Component Spacing</b>	<b>P</b>	8
<b>Hole Diameter</b>	<b>D (<math>\pm 0.1/-0</math>)</b>	1.5
<b>Hole Diameter</b>	<b>D1 (min)</b>	1.5
<b>Hole Position</b>	<b>F (<math>\pm 0.05</math>)</b>	7.5
<b>Compartment Depth</b>	<b>K (max)</b>	6.5
<b>Hole Spacing</b>	<b>P1 (<math>\pm 0.1</math>)</b>	2



All dimensions are in mm.




**REVISION HISTORY**

Date	Revision	Description of Changes
Jul 2004	1	<ul style="list-style-type: none"><li>- Minor changes</li><li>- Current and voltage convention update (page 2).</li><li>- "Configuration diagram (top view) &amp; suggested connections for unused and n.c. pins" insertion (page 2).</li><li>- 6 cm<sup>2</sup> Cu condition insertion in Thermal Data table (page 3).</li><li>- V<sub>CC</sub> - OUTPUT DIODE section update (page 4).</li><li>- PROTECTIONS note insertion (page 3)</li><li>- Revision History table insertion (page 34).</li><li>- Disclaimers update (page 35).</li></ul>

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