

General Description

The MIC94001 is a silicon gate P-channel MOSFET designed for low on-resistance, high-side switch applications. The MIC94001 has a maximum on-resistance of 0.4Ω at 4.5V gate-to-source voltage.

Improved ESD protection is provided by the gate protection network shown in the schematic diagram.

The MIC94001 is supplied in a low-profile version of the 8-lead SOIC package.

The MIC94001 die can be assembled in a 4-terminal configuration with the body not shorted to the source for use in analog switch applications. Contact the factory for more information.

Features

- 15V minimum drain-to-source breakdown
- 0.4Ω maximum on-resistance at 4.5V gate-to-source
- Functional at 2.7V gate-to-source
- 0.063" maximum height

Applications

- High-side switch
- Power management
- Stepper motor control
- 1.8" PCMCIA disk-drive V_{CC} switch

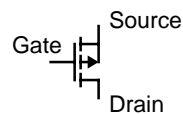
Ordering Information

Part Number	Temperature Range*	Package
MIC94001BLM	-55°C to +150°C	8-lead SOIC†

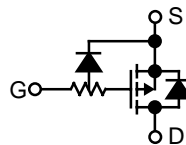
* Operating Junction Temperature

† Low Profile Leads, see Package Information

Schematic Information

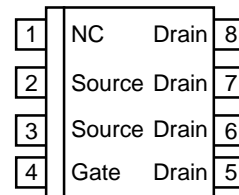


Schematic Symbol



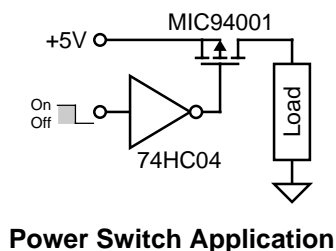
Schematic Diagram

Pin Configuration

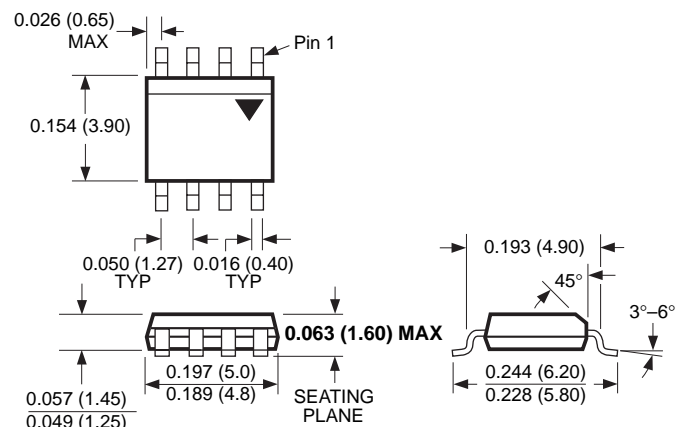


8-lead Low-Profile SOIC Package (LM)

Typical Application



Package Information



Absolute Maximum Ratings

Voltage and current values are negative. Signs not shown for clarity.

Drain-to-Source Voltage	15V
Gate-to-Source Voltage	15V
Continuous Drain Current	
$T_A = 25^\circ\text{C}$	1.6A
$T_A = 100^\circ\text{C}$	1A
Operating Junction Temperature	-55°C to +150°
Storage Temperature	-55°C to +150°C

Total Power Dissipation

$T_A = 25^\circ\text{C}$	1W
$T_A = 100^\circ\text{C}$	0.4W

Thermal Resistance

θ_{JA}	125°C/W
θ_{JC}	76°C/W

Lead Temperature

1/16" from case, 10s	+300°C
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Electrical Characteristics $T_A = 25^\circ\text{C}$ unless noted. All values are negative. Signs not shown for clarity.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{BDSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	15			V
V_{GS}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	1		3	V
I_{GSS}	Gate-Body Leakage	$V_{DS} = 0V, V_{GS} = 15V, \text{Note 2}$			100	nA
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 15V, V_{GS} = 0V$			25	μA
		$V_{DS} = 15V, V_{GS} = 0V, T_J = 125^\circ\text{C}$			250	μA
$I_{D(ON)}$	On-State Drain Current	$V_{DS} \geq 10V, V_{GS} = 10V, \text{Note 1}$		5.5		A
$R_{DS(ON)}$	Drain-Source On-State Resist.	$V_{GS} = 4.5V, I_D = 50mA$		0.35	0.40	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 15V, I_D = 1A, \text{Note 1}$		0.7		S

Note 1: Pulse Test: Pulse Width $\leq 300\mu\text{sec}$, Duty Cycle $\leq 2\%$

Note 2: ESD gate protection diode conducts during positive gate-to-source voltage excursions.

