

- STRUCTURE Silicon Monolithic Integrated Circuit
- PRODUCT SERIES 5ch Stepping Motor Driver
- TYPE **BD6754KN**
- FEATURES • Built in 4 PWM Constant-Current Drivers
 • Built in 1 Linear Constant-Current Driver

●Absolute maximum ratings (Ta=25°C)

| Parameter | Symbol | Limit | Unit |
|-----------------------------|--------|----------------------------|-------|
| Power supply voltage | VCC | -0.5 to +7.0 | V |
| Motor power supply voltage | VM | -0.5 to +7.0 | V |
| Control input voltage | VIN | -0.5 to VCC+0.5 | V |
| Power dissipation | Pd | 875* ¹ | mW |
| Operating temperature range | Topr | -20 to +75 | °C |
| Junction temperature | Tjmax | 150 | °C |
| Storage temperature range | Tstg | -55 to +150 | °C |
| H-bridge output current | Iout | -800 to +800* ² | mA/ch |

*¹ Reduced by 7.0mW/°C over 25°C, when mounted on a glass epoxy board (70mm × 70mm × 1.6mm).

*² Must not exceed Pd, ASO, or Tjmax of 150°C.

●Operating Conditions (Ta= -25°C to +75°C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|------------------------------|--------|------|------|--------------------|-------|
| Power supply voltage | VCC | 2.7 | 3.3 | 5.5 | V |
| Motor power supply voltage | VM | 2.7 | 3.3 | 5.5 | V |
| Control input voltage | VIN | 0 | - | VCC | V |
| PWM signal input frequency | FPWM | 0 | - | 0.1 | MHz |
| Serial clock input frequency | FSCLK | 0 | - | 10 | MHz |
| Master clock input frequency | FMCLK | 0 | - | 2 | MHz |
| H-bridge output current | Iout | - | - | ±500* ³ | mA/ch |

*³ Must not exceed Pd or ASO.

The product described in this specification is a strategic product (and/or service) subject to COCOM regulations. It should not be exported without authorization from the appropriate government authorities. This product isn't designed for protection against radioactive rays.

●Package Outline

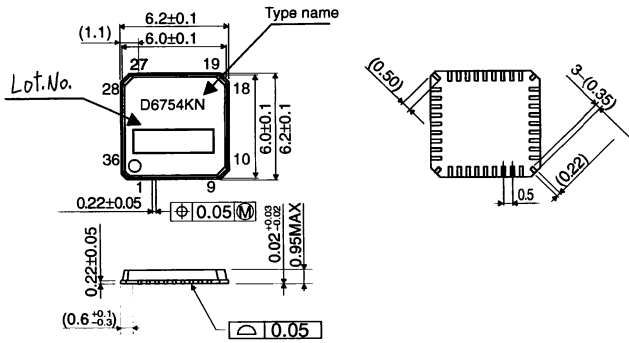


Fig.1 VQFN36 Package (Unit: mm)

●Pin Arrangement (Top View)

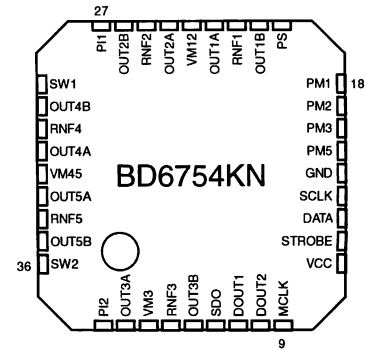


Fig.2 BD6754KN Pin Arrangement (Top View)

●Block Diagram

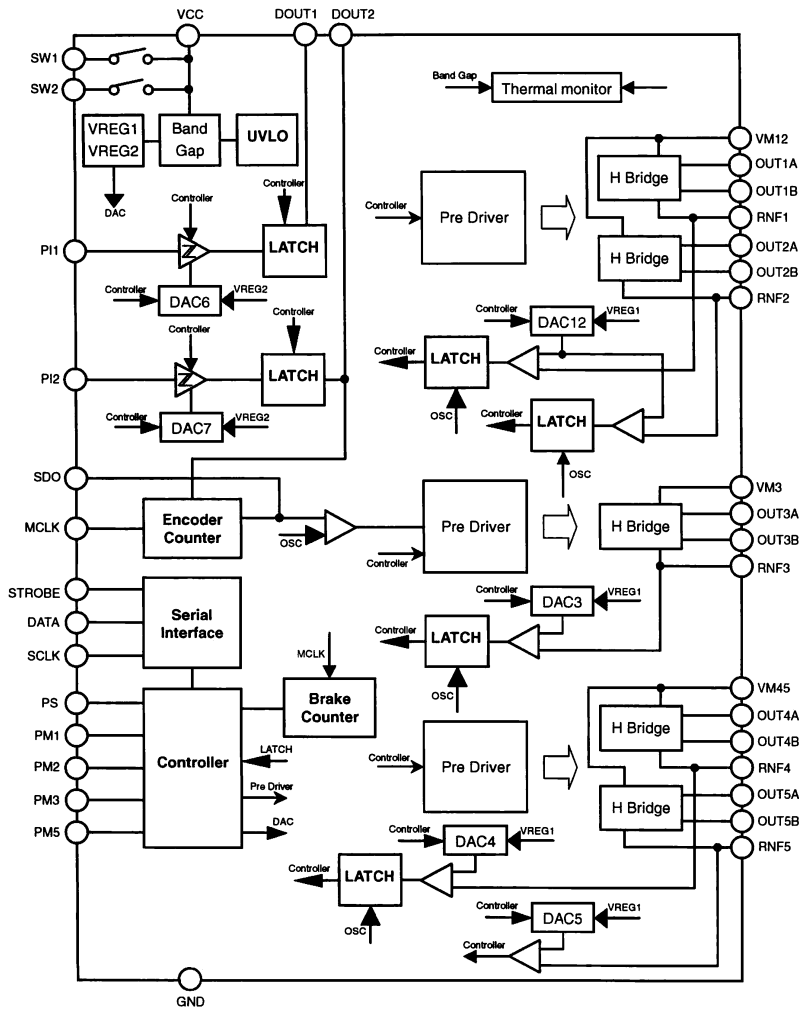


Fig.3 BD6754KN Block Diagram

●Pin No. and Pin Name

| No. | Pin name | No. | Pin name |
|-----|----------|-----|----------|
| 1 | PI2 | 19 | PS |
| 2 | OUT3A | 20 | OUT1B |
| 3 | VM3 | 21 | RNF1 |
| 4 | RNF3 | 22 | OUT1A |
| 5 | OUT3B | 23 | VM12 |
| 6 | SDO | 24 | OUT2A |
| 7 | DOUT1 | 25 | RNF2 |
| 8 | DOUT2 | 26 | OUT2B |
| 9 | MCLK | 27 | PI1 |
| 10 | VCC | 28 | SW1 |
| 11 | STROBE | 29 | OUT4B |
| 12 | DATA | 30 | RNF4 |
| 13 | SCLK | 31 | OUT4A |
| 14 | GND | 32 | VM45 |
| 15 | PM5 | 33 | OUT5A |
| 16 | PM3 | 34 | RNF5 |
| 17 | PM2 | 35 | OUT5B |
| 18 | PM1 | 36 | SW2 |

●BD6754KN Electrical Characteristics (Unless otherwise specified, Ta=25°C, VCC=3.3V, VM=3.3V)

| Parameter | Symbol | Limit | | | Unit | Conditions |
|--|---------|-------|---------|---------|------|--|
| | | Min. | Typ. | Max. | | |
| Overall | | | | | | |
| Circuit current during standby operation | ICCST | - | 0 | 1 | μA | PS=L |
| Circuit current | ICC | 2.0 | 4.0 | 7.5 | mA | PS=H with no signal |
| Control input | | | | | | |
| High level input voltage | VINH | 2.0 | - | VCC | V | |
| Low level input voltage | VINL | 0 | - | 0.7 | V | |
| High level input current 1 | IINH1 | 16.5 | 33 | 66 | μA | PM1~PM5, MCLK, PS; VIN=3.3V |
| High level input current 2 | IINH2 | 8.2 | 16.5 | 33 | μA | STROBE, DATA, SCLK; VIN=3.3V |
| Low level input current | IINL | -3 | 0 | 3 | μA | PM1~PM5, MCLK, PS, STROBE, DATA, SCLK; VIN=0V |
| Pull-down resistor 1 | RIN1 | 50 | 100 | 200 | kΩ | PM1~PM5, MCLK, PS |
| Pull-down resistor 2 | RIN2 | 100 | 200 | 400 | kΩ | STROBE, DATA, SCLK |
| UVLO | | | | | | |
| UVLO voltage | VUVLO | 1.75 | - | 2.25 | V | |
| PWM Constant-Current Drive block (ch1 to ch4) | | | | | | |
| Output ON-Resistance | RON | - | 1.4 | 1.7 | Ω | Io=±400mA on high and low sides in total |
| Output limit voltage 1 | VLIM1 | 94 | 104 | 114 | mV | DAC=4'b0101(ch1~ch2), DAC=6'b010101(ch3~ch4) |
| Output limit voltage 2 | VLIM2 | 250 | 290 | 330 | mV | DAC=4'b1111(ch1~ch2), DAC=6'b111111(ch3~ch4) |
| Output OFF time 1 | TOFF1 | 0.5 | 1.0 | 2.0 | μs | off-t=1 |
| Output OFF time 2 | TOFF2 | 1.0 | 2.0 | 4.0 | μs | off-t=0 |
| Output minimum ON time | TMINON | 0.1 | 0.2 | 0.4 | μs | |
| Linear Constant-Current Drive block (ch5) | | | | | | |
| Output ON-Resistance | RON | - | 1.4 | 1.7 | Ω | Io=±400mA on high and low sides in total |
| Output limit voltage 1 | VLIM1 | 98 | 104 | 110 | mV | DAC=6'b010101 |
| Output limit voltage 2 | VLIM2 | 255 | 290 | 325 | mV | DAC=6'b111111 |
| PI comparator | | | | | | |
| In-phase input voltage range | VLOPI | 0 | - | VCC-1.5 | V | |
| Input bias current | IBIPI | -3 | 0 | 3 | μA | When PI1=PI2=0V |
| Input offset voltage | VOFPI | -30 | 0 | 30 | mV | |
| Output low level voltage | VLOPI | 0 | 0.5 | 1.0 | V | With 1mA sink current |
| Output high level voltage | VHIPI | VCC-1 | VCC-0.5 | VCC | V | With 1mA source current |
| Threshold voltage 1 | VTHPI1 | 0.8 | 1.0 | 1.2 | V | DAC=4'b1000 |
| Threshold voltage 2 | VTHPI2 | 1.5 | 1.875 | 2.25 | V | DAC=4'b1111 |
| Upper hysteresis width 9 | VHYS9PI | +0.22 | +0.44 | +0.66 | V | PI hysteresis setting 1 and 2=4'b1000 (VTHPI center) |
| Lower hysteresis width 9 | VHYS9PI | -0.19 | -0.36 | -0.53 | V | PI hysteresis setting 1 and 2=4'b1000 (VTHPI center) |
| Speed discriminator | | | | | | |
| PWM oscillating frequency | FPWM | 50 | 100 | 200 | kHz | |
| SDO charge current 5 | ISDOD5 | -75 | -50 | -25 | μA | Charge pump setting=3b'100 |
| SDO discharge current 5 | ISDOD5 | +25 | +50 | +75 | μA | Charge pump setting=3b'100 |
| Analog Switch | | | | | | |
| ON-Resistance | RONSW | - | 250 | 500 | Ω | With 1mA source current |

●Operation Notes

(1) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range (Topr) may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. The implementation of a physical safety measure such as a fuse should be considered when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

(2) Power supply lines

Regenerated current may flow as a result of the motor's back electromotive force. Insert capacitors between the power supply and ground pins to serve as a route for regenerated current. Determine the capacitance in full consideration of all the characteristics of the electrolytic capacitor, because the electrolytic capacitor may lose some capacitance at low temperatures. If the connected power supply does not have sufficient current absorption capacity, regenerative current will cause the voltage on the power supply line to rise, which combined with the product and its peripheral circuitry may exceed the absolute maximum ratings. It is recommended to implement a physical safety measure such as the insertion of a voltage clamp diode between the power supply and GND pins.

(3) Ground potential

Ensure a minimum GND pin potential in all operating conditions.

(4) Setting of heat

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

(5) Actions in strong magnetic field

Use caution when using the IC in the presence of a strong magnetic field as doing so may cause the IC to malfunction.

(6) ASO

When using the IC, set the output transistor for the motor so that it does not exceed absolute maximum ratings or ASO.

(7) Thermal shutdown circuit

This IC incorporates a TSD (thermal shutdown) circuit (TSD circuit). If the temperature of the chip reaches the following temperature, the motor coil output will be opened. The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

| TSD ON temperature [°C] (Typ.) | Hysteresis temperature [°C] (Typ.) |
|-----------------------------------|---------------------------------------|
| 175 | 20 |

(8) Ground Wiring Pattern

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

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