Data Sheet | February 18, 2009 | FN6845.0

Synchronous Step-Down MOSFET Drivers

Description

The ZL1505 is an integrated high-speed, high-current N-channel MOSFET driver for synchronous step-down DC-DC conversion applications. When used with Zilker Labs Digital-DC™ PWM controllers, the ZL1505 enables dynamically adaptive dead-time control that optimizes efficiency under all operating conditions. A dual input PWM configuration enables this efficiency optimization while minimizing complexity within the driver.

Operating from a 4.5 V to 7.5 V input, the ZL1505 combines a 5 A, 0.5 Ω low-side driver and a 3 A, 0.8 Ω high-side driver to support high step-down buck applications. A unique adjustable gate drive current scheme allows the user to adjust the drive current on both drivers to optimize performance for a wide rage of input/output voltages, load currents, power MOSFETs and switching frequencies up to 1.4 MHz. An integrated 30 V bootstrap Schottky diode is used to charge the external bootstrap capacitor. An internal watchdog circuit prevents excessive shoot-through currents and protects the external MOSFET switches.

The ZL1505 is specified over a wide -40 °C to 125 °C junction temperature range and is available in an exposed pad DFN-10 package.

Features

- High-speed, high-current drivers for synchronous N-channel MOSFETs
- Adaptive dead-time control optimizes efficiency when used with Digital-DC controllers
- Adjustable gate drive voltage: 4.5 V to 7.5 V
- Integrated 30 V bootstrap Schottky diode
- Capable of driving ≥ 40 A per phase
- Supports switching frequency up to 1.4 MHz
  - >4 A source, >5 A sink low-side driver
  - >3 A source/sink high-side driver
  - <10 ns rise/fall times, low propagation delay
- Adjustable gate drive strength optimizes efficiency for different V_{IN}, V_{OUT}, I_{OUT}, F_{SW} and MOSFET combinations
- Internal non-overlap watchdog prevents shoot-through currents
- Exposed pad 3 x 3 mm DFN-10 package
- RoHS-compliant, Pb-free

Applications

- High efficiency, high-current DC-DC buck converters with digital control and PMBus™
- Multi-phase digital DC-DC converters with phase adding/dropping
- Power train modules
- Synchronous rectification for secondary side isolated power converters

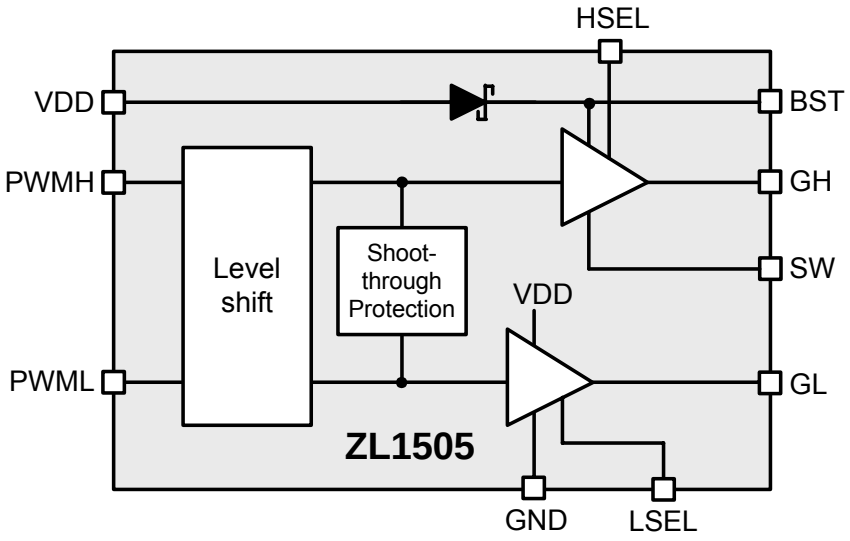


Figure 1. ZL1505 Block Diagram

1. Electrical Characteristics

Table 1. Absolute Maximum Ratings

Voltage measured with respect to GND. Operating beyond these limits may cause permanent damage to the device. Functional operation beyond the Recommended Operating Conditions is not implied.

Parameter	Pin	Value	Unit
DC supply voltage	VDD	- 0.3 to 8	V
Logic I/O voltages	PWMH, PWML, LSEL	- 0.3 to 8	V
	HSEL	(V_{SW} - 0.3) to (V_{BST} + 0.3)	V
High-side supply voltage	BST	- 0.3 to 30	V
High-side drive voltage	GH	(V_{SW} - 0.3) to (V_{BST} + 0.3)	V
Low-side drive voltage	GL	(GND - 0.3) to (V_{IN} + 0.3)	V
Boost to switch differential V_{BST} - V_{SW}	BST, SW	- 0.3 to 8	V
Switch voltage, continuous Switch voltage, < 100ns	SW	(GND - 0.3) to 30 (GND - 5) to 30	V V
Junction temperature		- 55 to 150	°C
Storage temperature		- 55 to 150	°C
Lead temperature	Soldering, 10s	300	°C

Table 2. Recommended Operating Conditions and Thermal Information

Parameter	Symbol	Min	Typ	Max	Unit
Gate Drive Bias Supply Voltage Range	V_{DD}	4.5	–	7.5	V
Input Supply Voltage Range	V_{IN}	3.0	–	30 - V_{DD}	V
Operating Junction Temperature Range	T_J	- 40	–	125	°C
Junction to Ambient Thermal Impedance[1]	Θ_{JA}	–	50	–	°C/W
Junction to Case Thermal Impedance[1]	Θ_{JC}	–	7	–	°C/W

Notes: 1. Θ_{JA} measured in free air with device mounted on a 4-layer FR4 board and exposed pad soldered to low impedance ground plane using multiple vias. For Θ_{JC}, the “case” temperature is measured at the center of the exposed metal pad.

Table 3. Electrical Specifications

V_{DD} = 6.5 V, T_J = - 40 °C to 125 °C unless otherwise noted. Typical values are at T_A = 25 °C.

Parameter	Conditions	Min	Typ	Max	Unit
Bias Current Characteristics					
I_{DD} supply current	Not switching	–	110	180	µA
PWM Input Characteristics					
PWM input bias current	V_{PWM} = 5 V	–	5	–	µA
	V_{PWM} = 0 V	–	–	1	µA
PWM input logic low, V_{IL}	PWMH or PWML V_{DD} = 6.5 V V_{DD} = 5.0 V	 1.7 1.5	 2 1.7	 2.2 1.9	V
PWM input logic high, V_{IH}	PWMH or PWML V_{DD} = 6.5 V V_{DD} = 5.0 V	 2.8 2.2	 3.1 2.5	 3.4 2.7	V
Hysteresis	PWMH or PWML V_{DD} = 6.5 V V_{DD} = 5.0 V	 – –	 1.1 0.8	 – –	V
Minimum PWMH on-time to produce GH pulse, $t_{PWMH,ON}$ [1]	C_{GH} = 0	–	8.5	12	ns
Minimum GH on-time pulse, $t_{GH,ON}$ [2]	C_{GH} = 0 C_{GH} = 3 nF, V_{HSEL} = V_{BST}	– –	10 14	14 20	ns
Minimum PWMH off-time to produce valid GH pulse, $t_{PWMH,OFF}$	C_{GH} = 0	–	13	17	ns
Bootstrap Diode Characteristics					
Forward Voltage (V_F)	Forward bias current 100 mA	–	0.8	–	V
Thermal protection					
Thermal trip point		–	150	–	°C
Thermal reset point		–	134	–	°C
Upper Gate Driver Characteristics					
Driver voltage (V_{BST} – V_{SW})		–	6	–	V
High-side driver peak gate drive current (pull-up)	(V_{GH} – V_{SW}) = 2.5 V, HSEL connected to BST HSEL connected to SW	 2.0 1.0	 3.2 1.7	 – –	 A A
High-side driver peak gate drive current (pull-down)	(V_{GH} – V_{SW}) = 2.5 V, HSEL connected to BST HSEL connected to SW	 2.0 1.0	 3.2 1.6	 – –	 A A
High-side driver pull-up resistance	(V_{BST} – V_{GH}) = 50 mV, HSEL connected to BST HSEL connected to SW	 – –	 0.7 0.9	 0.9 1.2	 Ω Ω
High-side driver pull-down resistance	(V_{GH} – V_{SW}) = 50 mV, HSEL connected to BST HSEL connected to SW	 – –	 0.8 1.1	 1.1 1.5	 Ω Ω

Notes:

1. The minimum PWMH on-time pulse ($t_{PWMH,ON}$) is specified from V_{PWM} = 2.5 V on the rise edge to V_{PWM} = 2.5 V on the falling edge.
2. The minimum GH on-time pulse ($t_{GH,ON}$) is specified at V_{GH} = 2.5 V.

Table 3. Electrical Specifications (Cont'd)

V_{DD} = 6.5 V, T_J = - 40 °C to 125 °C unless otherwise noted. Typical values are at T_A = 25 °C.

Parameter	Conditions	Min	Typ	Max	Unit
Lower Gate Driver Characteristics					
Driver voltage (V_{DD})		–	6.5	–	V
Low-side driver peak gate drive current (pull-up)	(V_{GL} - V_{GNG}) = 2.5 V, LSEL connected to VDD LSEL connected to GND	 3.0 1.5	 4.5 2.4	 – –	 A A
Low-side driver peak gate drive current (pull-down)	(V_{GL} – V_{GND}) = 2.5 V, LSEL connected to VDD LSEL connected to GND	 3.5 1.8	 5.4 2.8	 – –	 A A
Low-side driver pull-up resistance	(V_{DD} - V_{GL}) = 50 mV, LSEL connected to VDD LSEL connected to GND	 – –	 0.7 1.0	 0.9 1.3	 Ω Ω
Low-side driver pull-down resistance	(V_{GL} – GND) = 50 mV LSEL connected to VDD LSEL connected to GND	 – –	 0.5 0.7	 0.7 1.0	 Ω Ω
Switching Characteristics					
GH rise time, t_{RH}	C_{GH} = 3 nF, HSEL connected to BST HSEL connected to SW	 – –	 5.3 10.5	 8.5 16.5	 ns ns
GH fall time, t_{FH}	C_{GH} = 3 nF, HSEL connected to BST HSEL connected to SW	 – –	 4.8 9.5	 7.5 15	 ns ns
GL rise time, t_{RL}	C_{GL} = 3 nF LSEL connected to VDD LSEL connected to GND	 – –	 4.0 7.8	 6.0 12	 ns ns
GL fall time, t_{FL}	C_{GL} = 3 nF LSEL connected to VDD LSEL connected to GND	 – –	 3.0 5.5	 4.5 8.5	 ns ns
GH turn-on propagation delay, t_{DHR}	HSEL connected to BST HSEL connected to SW	– –	30.0 31.5	– –	ns ns
GH turn-off propagation delay, t_{DHF}	HSEL connected to BST HSEL connected to SW	– –	37.5 39.0	– –	ns ns
GL turn-on propagation delay, t_{DLR}	LSEL connected to VDD LSEL connected to GND	– –	26.5 28.0	– –	ns ns
GL turn-off propagation delay, t_{DLF}	LSEL connected to VDD LSEL connected to GND	– –	30.0 31.5	– –	ns ns

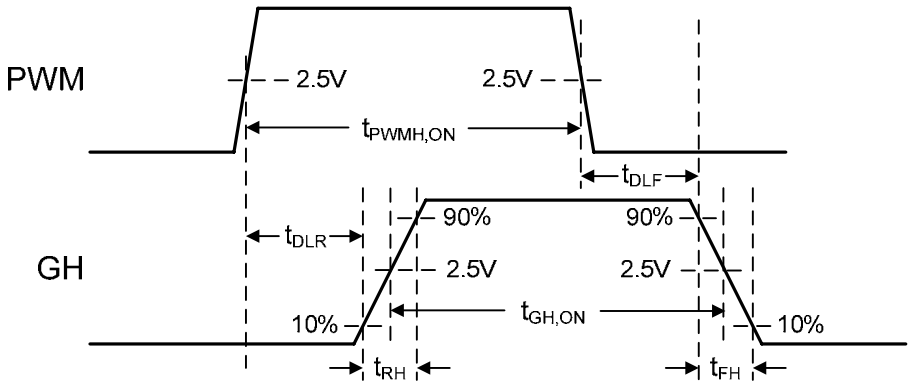


Figure 2. Timing Diagram

3. Typical Performance Curves [1]

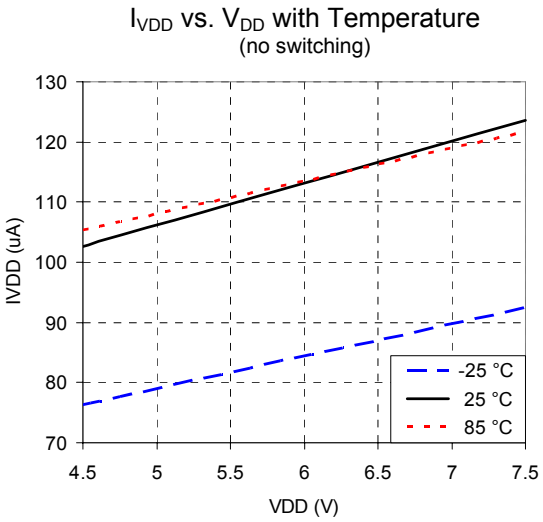


Figure 3

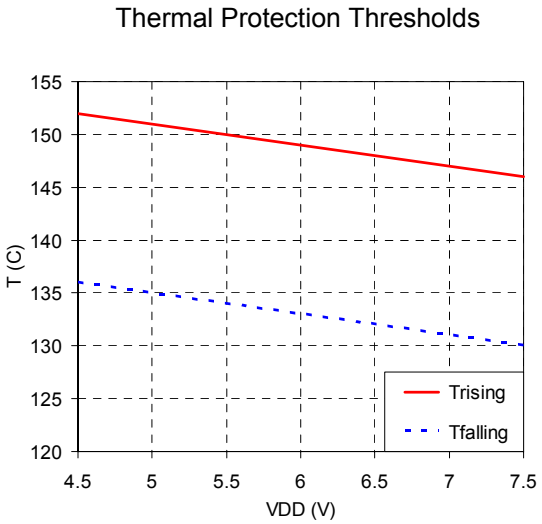


Figure 4

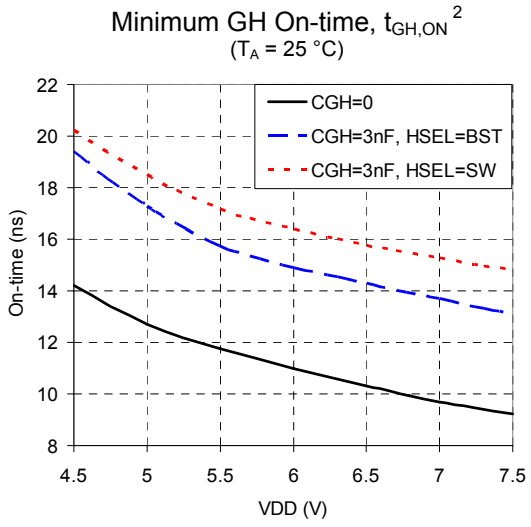


Figure 5

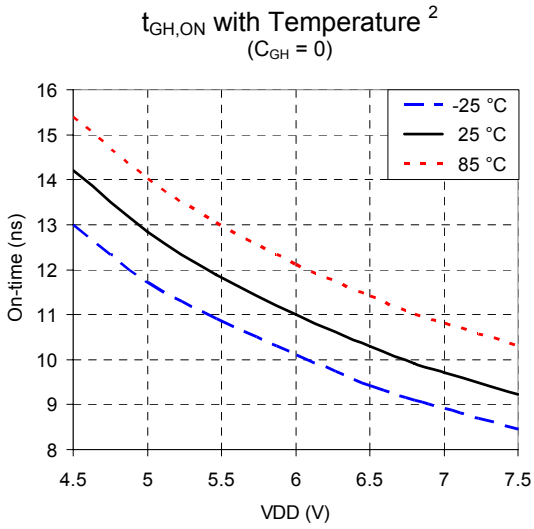


Figure 6

Notes:
1. Performance curves with temperature are measured at ambient temperatures (T_A) of 85 °C, 25 °C and -25 °C.
2. $t_{GH,ON}$ timing is shown in Figure 2.

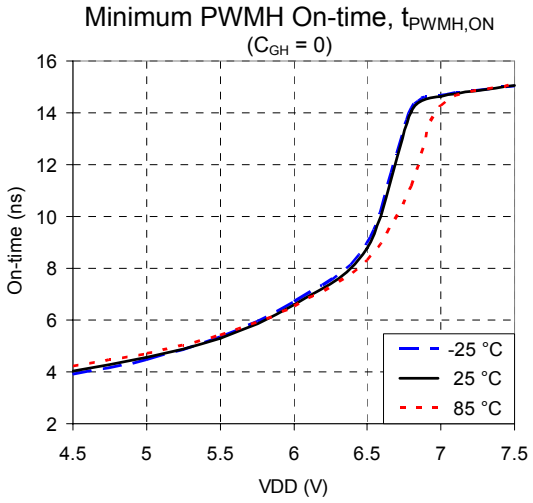


Figure 7

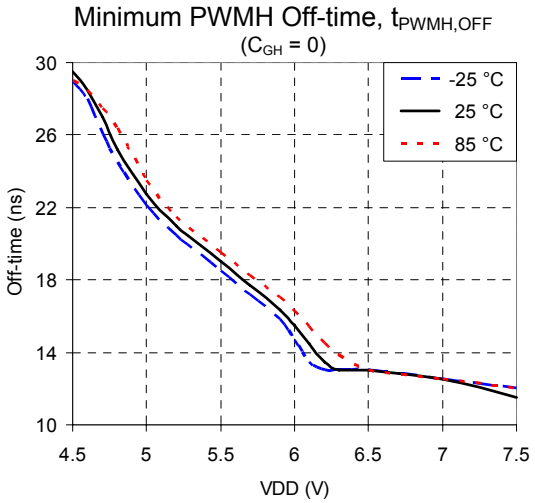


Figure 8

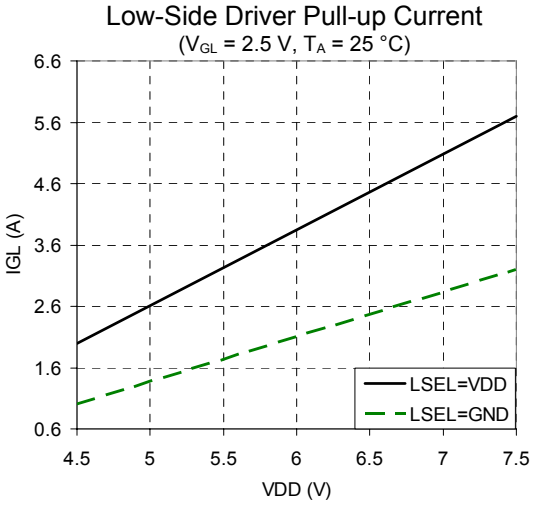
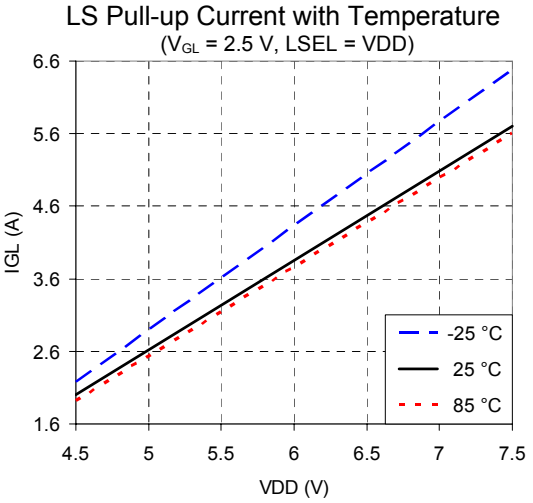


Figure 9



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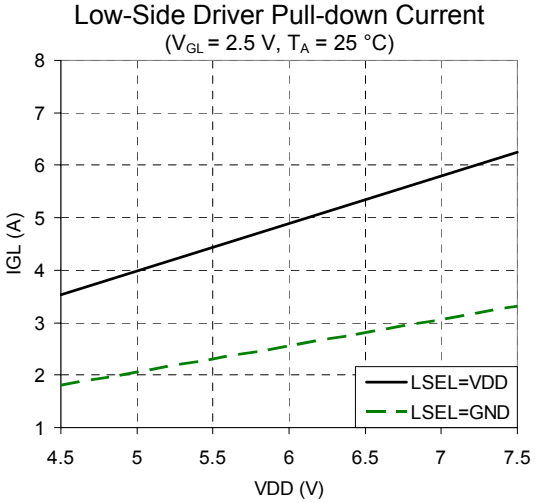
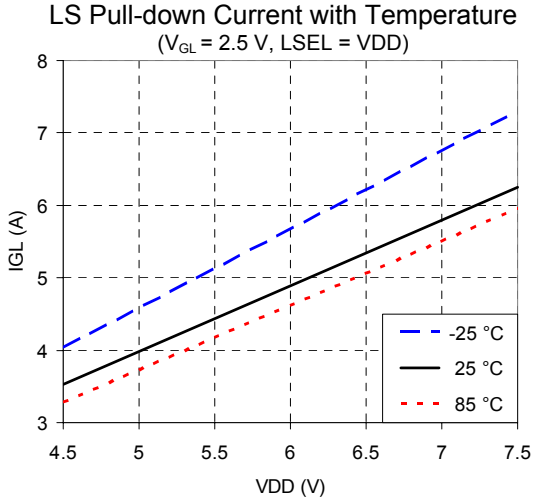


Figure 11



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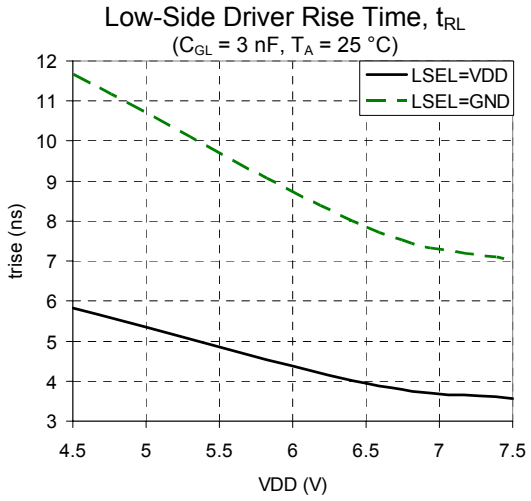


Figure 13

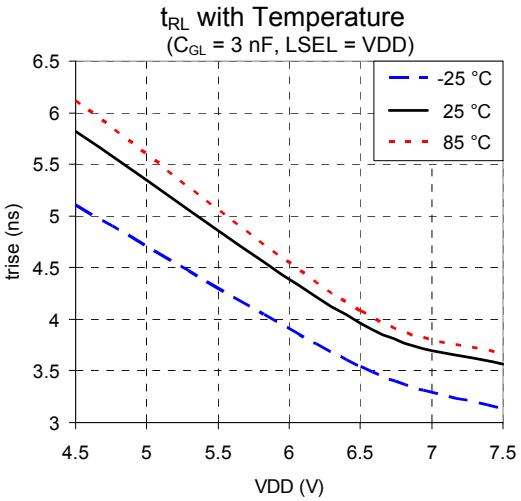


Figure 14

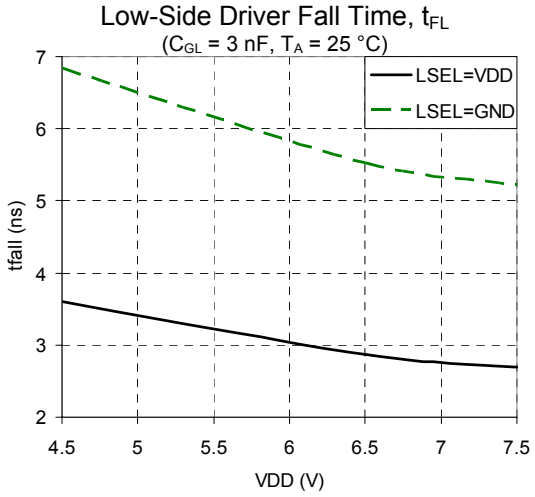


Figure 15

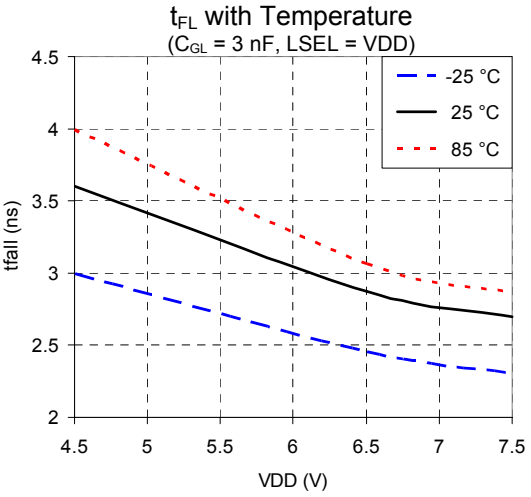


Figure 16

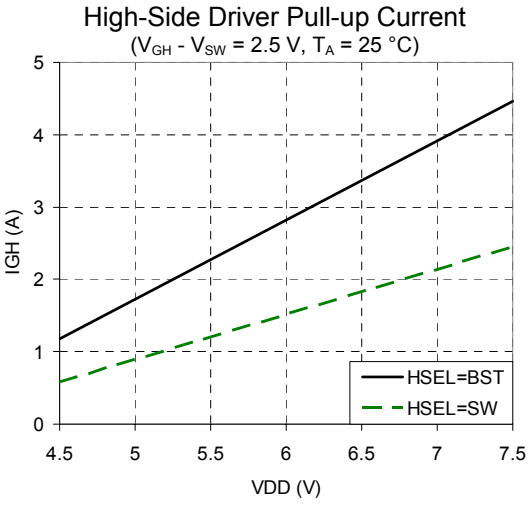


Figure 17

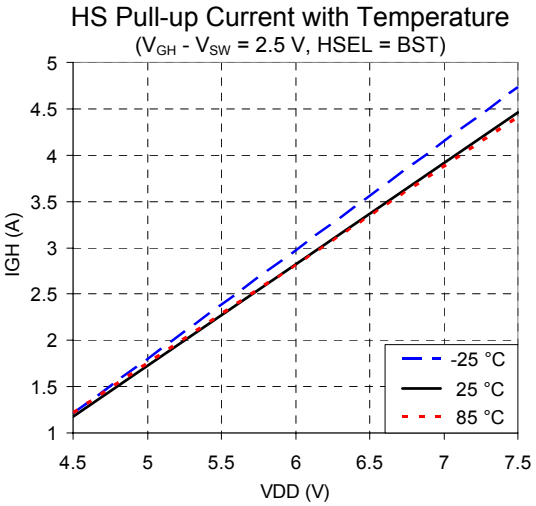


Figure 18

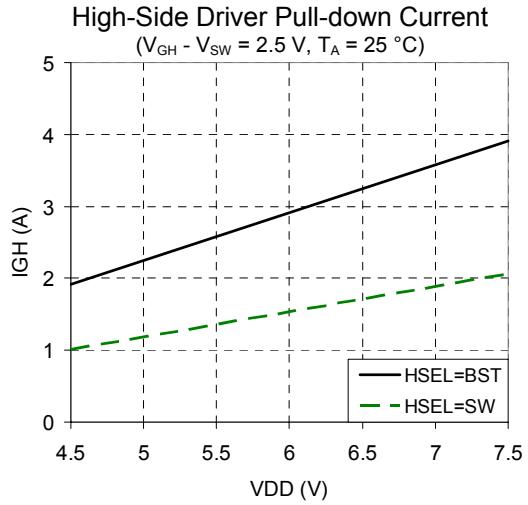


Figure 19

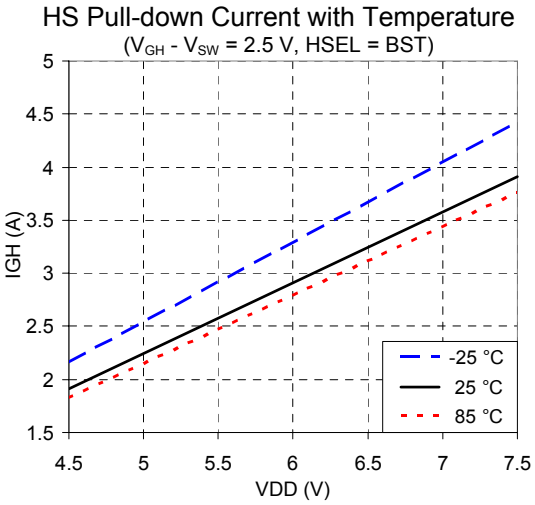


Figure 20

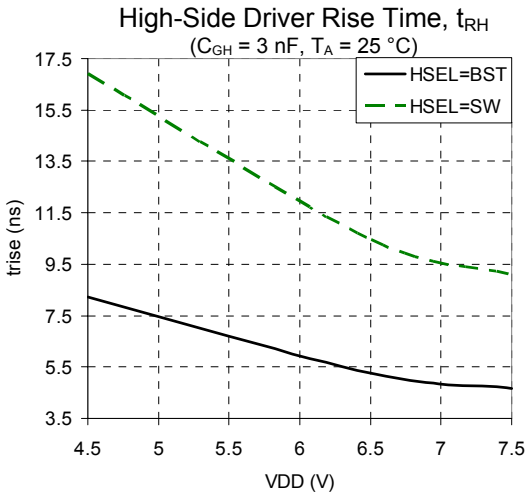


Figure 21

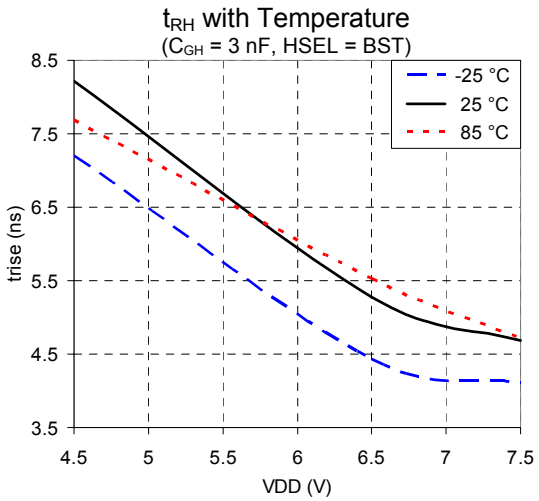


Figure 22

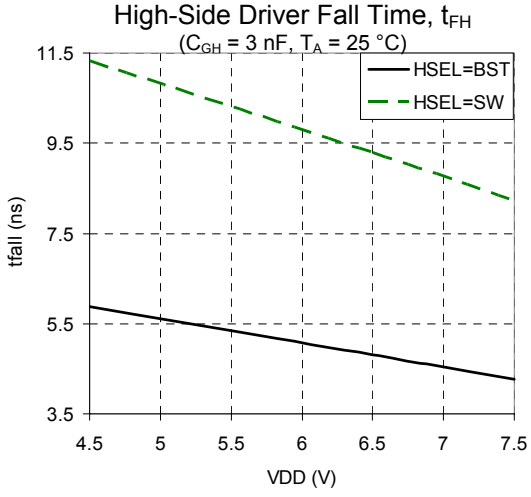


Figure 23

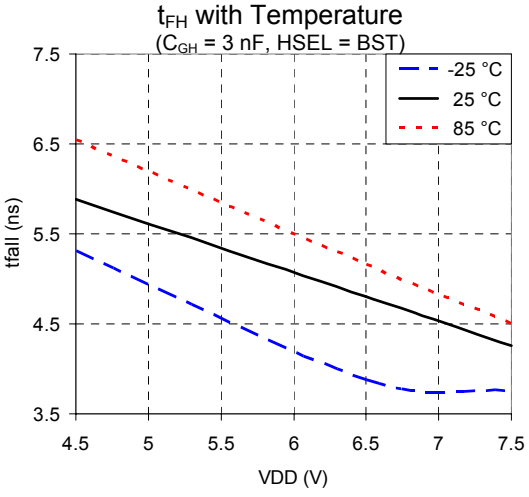


Figure 24

4. Pin Descriptions

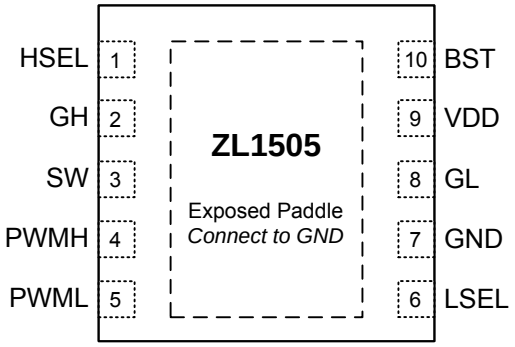


Figure 25. ZL1505 Pin Configurations (top view)

Table 4. Pin Descriptions

Pin	Label	Type [1]	Description
1	HSEL	I	High-side gate drive current selector. Connect to BST for maximum gate drive current; Connect to SW for 50% of maximum gate drive current.
2	GH	O	Output of high-side gate driver. Connect to the gate of high-side FET.
3	SW	I/O	Phase node. Return path for high-side driver. Connect to source of high-side FET and drain of low-side FET.
4	PWMH	I	High-side PWM control input.
5	PWML	I	Low-side PWM control input.
6	LSEL	I	Low-side gate drive current selector. Connect to VDD for maximum gate drive current; Connect to GND for 50% of maximum gate drive current.
7	GND	PWR	Ground. All signals return to this pin.
8	GL	O	Output of low-side gate driver. Connect to the gate of low-side FET.
9	VDD	PWR	Gate drive bias supply. Connect a high quality bypass capacitor from this pin to GND.
10	BST	PWR	Bootstrap supply. Connect external capacitor to SW node.
ePad	GND	PWR	Ground.

Notes:

1. I = Input, O = Output, PWR = Power or Ground.

5. Typical Applications Circuit

The following application circuit represents the typical implementation of the ZL1505.[1,2]

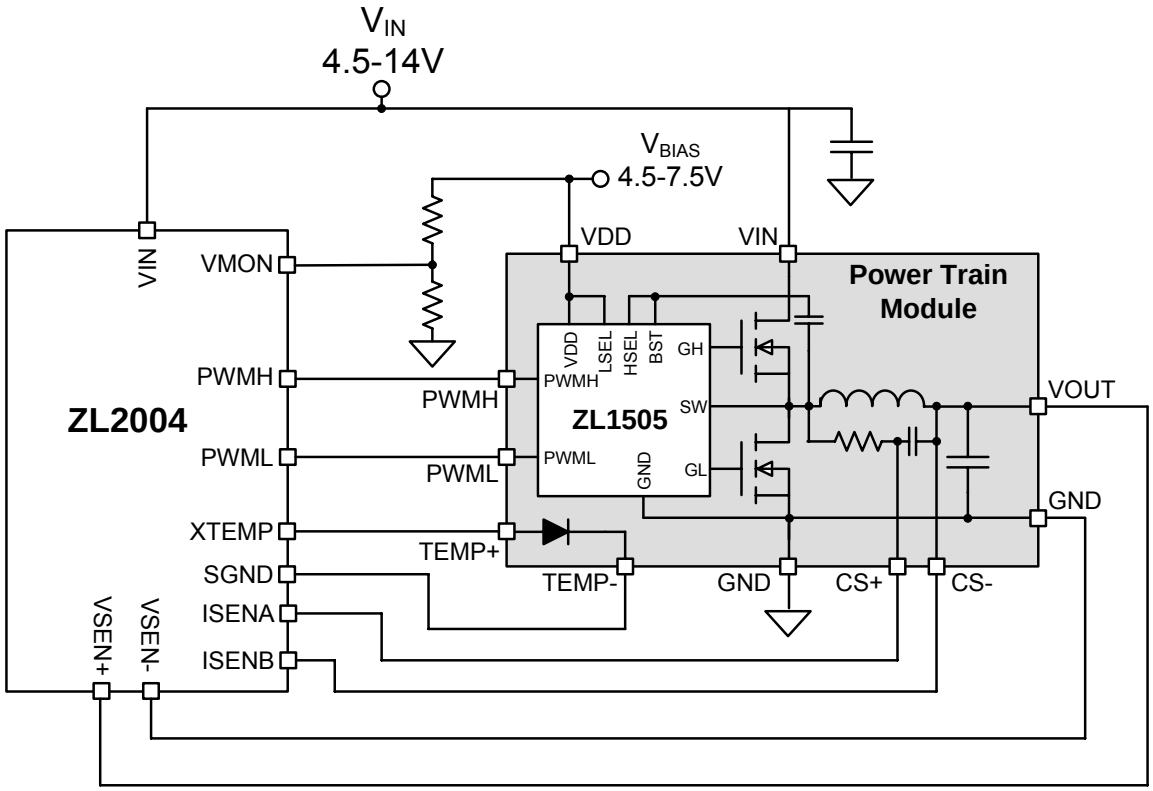


Figure 26. ZL1505 Application Circuit – Power Train Module using ZL2004 PWM Controller

Notes:

1. For V_{DD} of 4.5 to 7.5 V, the maximum V_{IN} of the ZL1505 is 22.5 to 25.5 V. ZL1505 input supply voltage range (V_{IN}) is specified in Table 2.
2. V_{IN} for this application circuit is limited by the ZL2004 V_{IN} of 4.5 to 14 V.

6. ZL1505 Overview

6.1 Theory of Operation

The ZL1505 is a synchronous N-channel MOSFET driver that is intended for use with Zilker Labs Digital-DC PWM controllers to enable a high-efficiency DC-DC conversion scheme. The patented Digital-DC control scheme utilizes a closed-loop algorithm to optimize the dead-time applied between the gate drive signals for the high-side and low-side MOSFETs. By monitoring the duty cycle of the resulting DC-DC converter circuit, this dynamic routine continuously varies the MOSFET dead times to optimize conversion efficiency in response to varying circuit conditions. The ZL1505's dual PWM input configuration enables this optimization scheme to be applied while minimizing the complexity within the driver device. Please refer to the ZL2004 data sheet for details on the dynamic dead-time optimization routine.

The ZL1505 integrates two powerful gate drivers that have been optimized for step-down DC-DC conversion circuit configurations whose output current can exceed 40 A per phase. The ZL1505 also integrates a 30 V bootstrap Schottky diode to minimize the external components and provide a high drive voltage to the high-side driver device.

6.2 Variable Gate Drive Current

The ZL1505 incorporates an innovative variable drive current scheme that enables the user to optimize the gate drive current levels to the requirements of the external MOSFETs used over a wide range of operating frequencies. Each of the gate drivers incorporates a logic input (HSEL and LSEL) that allows the user to select the gate drive strength to 50% or 100% of the total rated drive current.

With the HSEL pin connected to the BST pin, the high-side driver can deliver the full rated gate drive current; with the HSEL pin connected to the SW pin, the output current will be limited to 50% of the full rated output capability. With the LSEL pin is connected to VDD, the low-side driver can deliver the full rated gate drive current; with the LSEL pin connected to GND, the output current will be limited to 50% of the full rated output capability. Using HSEL and LSEL, the ZL1505 can be used across a wide range of applications using only a simple PCB layout change.

Also, the VDD pin is the gate drive bias supply for the external MOSFETs. VDD can be used to vary the gate drive strength as shown for the low-side driver in Figure 9 to Figure 12 and for the high-side driver in Figure 17 to Figure 20.

6.3 Overlap Protection Circuit

The ZL1505 includes an internal watchdog circuit that prevents excessive shoot-through current from occurring in the unlikely event that the PWM converter places both switches in the ON position. If the overlap time between the PWMH and PWML pulses exceeds 30 ns, the PWMH signal will be forced to the LOW state until the overlap condition ceases, allowing normal switching operation to continue.

6.4 Start-up Requirements

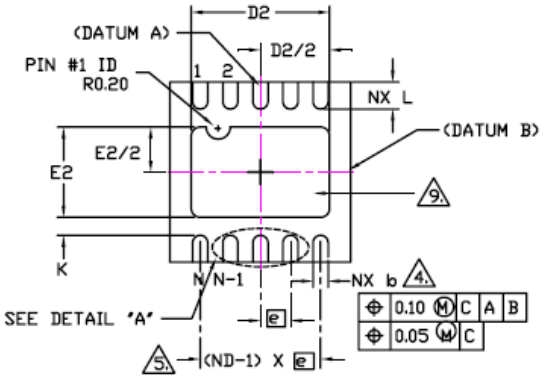
During power-up, the ZL1505 maintains both GH and GL outputs in the LOW state while the V_{IN} voltage is ramping up. Once the VDD supply is within specification, the GH and GL pins may be operated using the PWMH and PWML logic inputs respectively.

In the case where the PWM controller is powered from a supply other than the ZL1505's VDD supply, and the PWM controller is powered up first, the PWM controller gate outputs should be kept in low or in high-impedance state until the VDD supply is within specification. Additionally, if the ZL1505 begins its power-down sequence prior to the PWM controller then the PWM controller gate outputs should be set in low or in high-impedance state before the VDD voltage supply drops below its specified range.

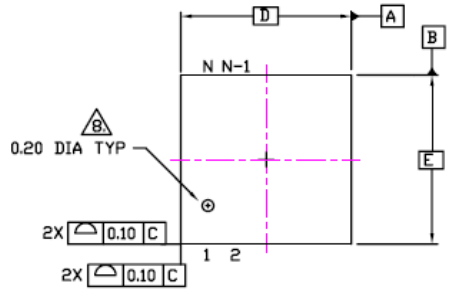
6.5 Thermal protection

When the junction temperature exceeds 150 °C the high-side driver output GH is forced to logic low state. The driver output is allowed to switch logic states again once the junction temperature drops below 134 °C.

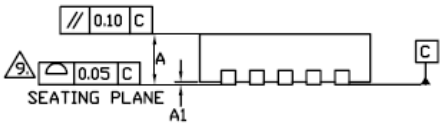
7. Package Dimensions



BOTTOM VIEW



TOP VIEW

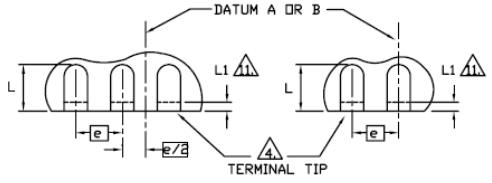


SIDE VIEW

NOTES :

1. DIMENSIONING AND TOLERANCING CONFORME TO ASME Y14.5M - 1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS, θ IS IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND REFER TO THE NUMBER OF TERMINALS ON D SIDE.
6. MAX. PACKAGE WARPAGE IS 0.05 mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LASER MARKED.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. THIS DRAWING CONFORMES TO JEDEC REGISTERED OUTLINE MO-229.
11. DEPENDING ON THE METHOD OF LEAD TERMINATION AT THE EDGE OF THE PACKAGE, PULLBACK (L1) MAYBE PRESENT.
12. PULLBACK DESIGN OPTION IS FOR 0.50mm NOMINAL LANDLENGTH ONLY

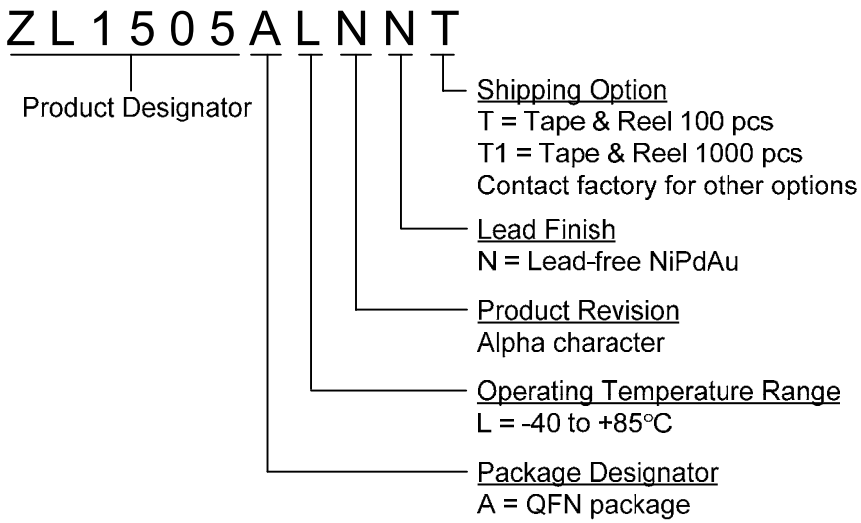
SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	0.80	0.85	0.90	
A1	0.00	0.02	0.05	
A3		0.20 REF.		
θ	0	—	12	2
K		0.20 MIN.		
D		3.0 BSC		
E		3.0 BSC		
L1		0.15 mm MAX		11
e		0.50 BSC.		
N		10		3
ND		5		5
L	0.35	0.40	0.45	12
b	0.18	0.25	0.30	4
D2	2.20	2.30	2.40	
E2	1.50	1.60	1.70	



EVEN TERMINAL/SIDE ODD TERMINAL/SIDE

DETAIL "A"

8. Ordering Information



9. Revision History

Rev #	Description	Date
1.0	Initial Release	Feb 2008
1.1	Title change	Mar 2008
1.2	Specified Input Supply Voltage Range V_{IN} (Table 2) Added Typical Performance Curves (Section 2) Updated Typical Application Circuit (Figure 26)	May 2008
1.3	Updated Ordering Information	May 2008
1.4	Table 3: Corrected Upper Gate Driver and Lower Gate Driver test conditions.	January 2009
FN6845.0	Assigned file number FN6845 to datasheet as this will be the first release with an Intersil file number. Replaced header and footer with Intersil header and footer. Updated disclaimer information to read “Intersil and it’s subsidiaries including Zilker Labs, Inc.” No changes to datasheet content	February 2009

Zilker Labs, Inc.
4301 Westbank Drive
Building A-100
Austin, TX 78746

Tel: 512-382-8300
Fax: 512-382-8329

www.zilkerlabs.com

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