IXYS | IX6R11

6A Half-Bridge Driver

Features

- Floating High Side Driver with boot-strap Power supply along with a Low Side Driver.
- Fully operational to 650V
- ± 50V/ns dV/dt immunity
- Gate drive power supply range: 10 - 35V
- Undervoltage lockout for both output drivers
- Separate Logic power supply range: 3.3V to V_{CL}
- Built using the advantages and compatibility of CMOS and IXYS HDMOS™ processes
- Latch-Up protected over entire operating range
- High peak output current: 6A
- Matched propagation delay for both outputs
- Low output impedance
- Low power supply current
- Immune to negative voltage transients

Warning: The IX6R11 is ESD sensitive.

General Description

The IX6R11 Bridge Driver for N-channel MOSFETs and IGBTs with a high side and low side output, whose input signals reference the low side. The High Side driver can control a MOSFET or IGBT connected to a positive buss voltage up to 650V. The logic input stages are compatible with TTL or CMOS, have built-in hysteresis and are fully immune to latch up over the entire operating range. The IX6R11 can withstand dV/dt on the output side up to ± 50V/ns.

The IX6R11 comes in either the 14-PIN DIP package (IX6R11P7), the 16-PIN SOIC package (IX6R11S3) or the 18-PIN, heat sinkable, SOIC package (IX6R11S6).

Applications

- Driving MOSFETs and IGBTs in half-bridge circuits
- High voltage, high side and low side drivers
- Motor Controls
- Switch Mode Power Supplies (SMPS)
- DC to DC Converters
- Class D Switching Amplifiers

Figure 1. Typical Circuit Connection

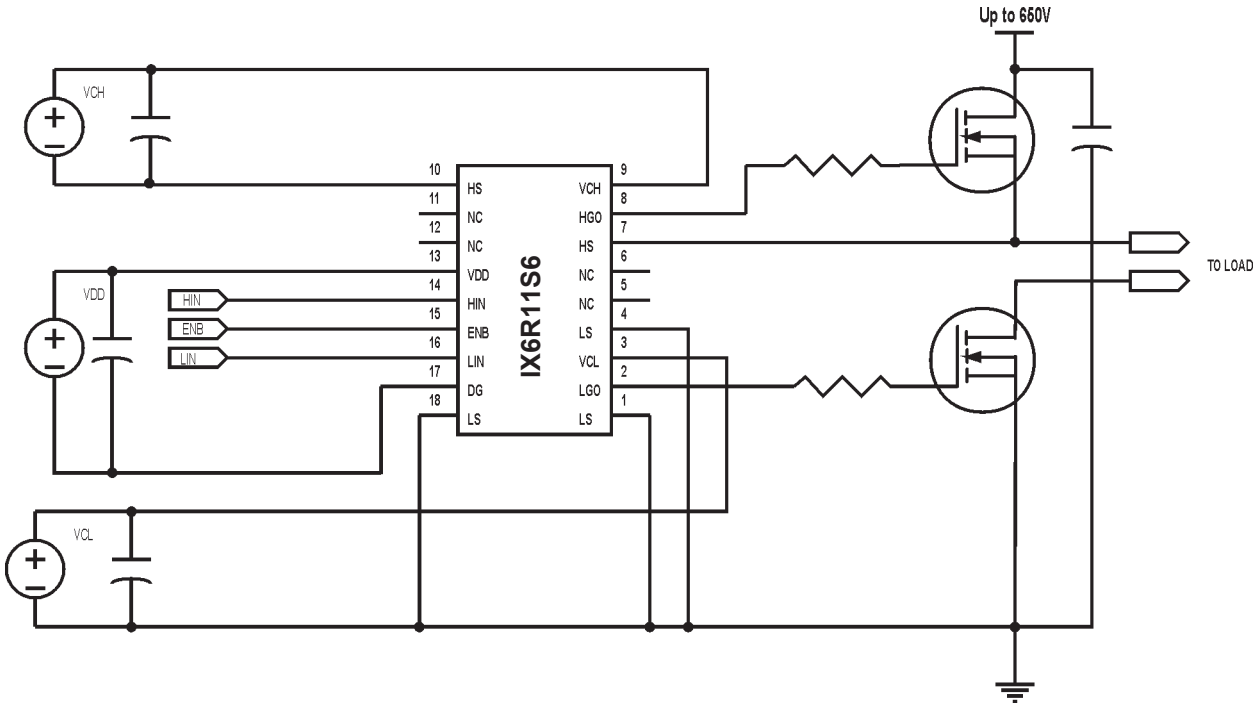
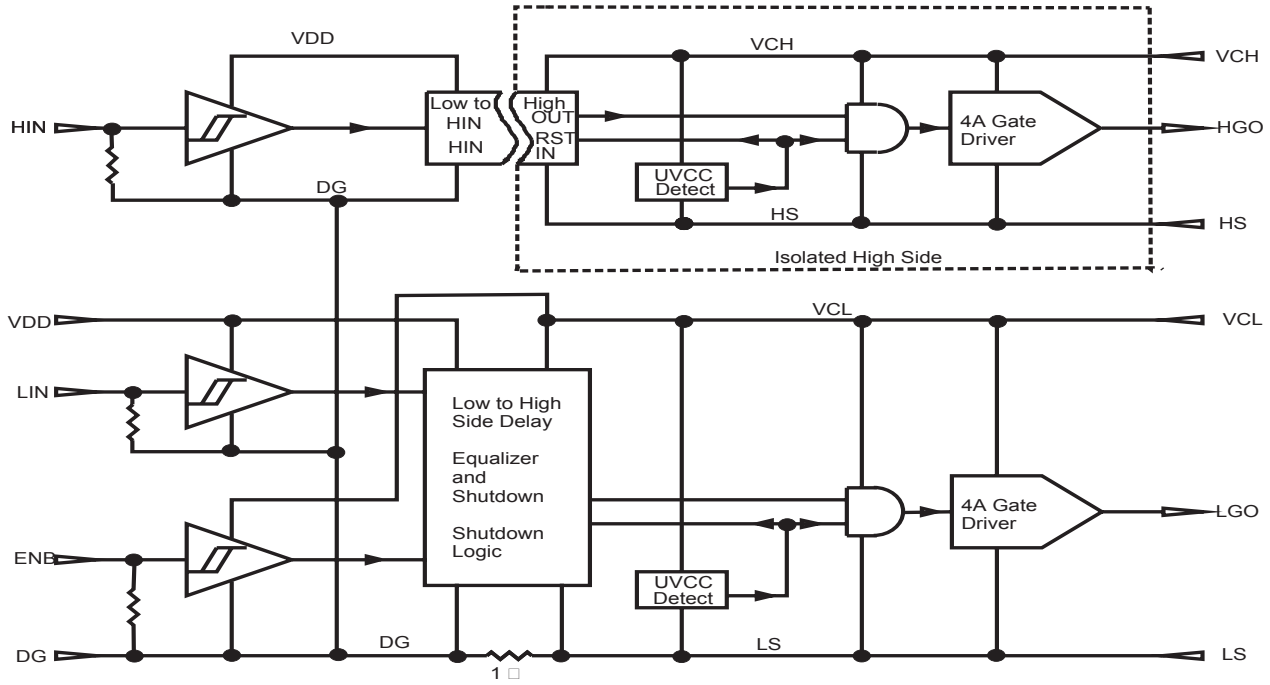


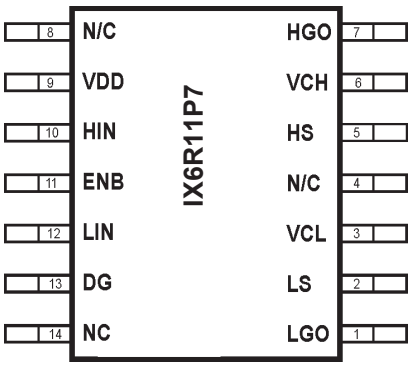
Figure 2 - IX6R11 Functional Block Diagram



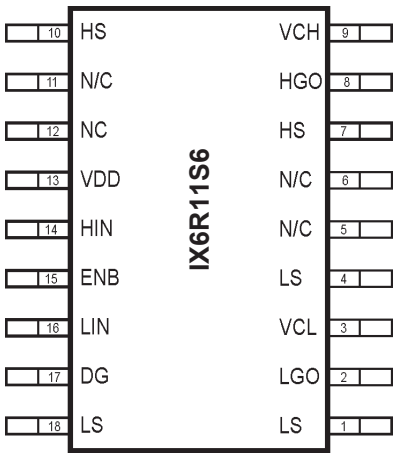
Pin Description And Configuration

SYMBOL	FUNCTION	DESCRIPTION
VDD	Logic Supply	Positive power supply for the chip CMOS functions
HIN	HS Input	High side Input signal, TTL or CMOS compatible; HGO in phase
LIN	LS Input	Low side Input signal, TTL or CMOS compatible; LGO in phase
ENB	Not Enable	Chip enable. When driven high, both outputs go low.
DG	Ground	Logic Reference Ground
VCH	Supply Voltage	High Side Power Supply
HGO	Output	High side driver output
HS	Return	High side voltage return pin
VCL	Supply Voltage	Low side power supply. This power supply provides power for both outputs. Voltage range is from 4.5 to 25V.
LGO	Output	Low side driver output
LS	Ground	Low side return

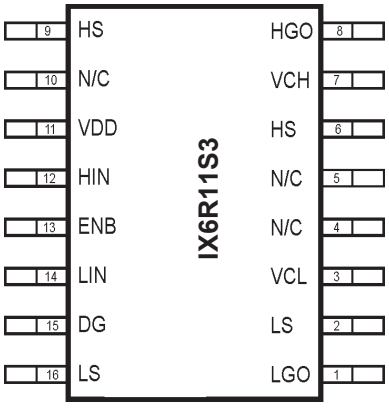
14-PIN DIP



18-PIN SOIC-CT



16-PIN SOIC



Absolute Maximum Ratings

Symbol	Definition		Min	Max	Units
V_{CH}	High side floating supply voltage		-25	650	V
V_{HS}	High side floating supply offset voltage		V_{CH}-200	V_{CH}+.3	V
V_{HGO}	High side floating output voltage		V_{HS}-.3	V_{CH}+.3	V
V_{CL}	Low side fixed supply voltage		-0.3	35	V
V_{LGO}	Low side output voltage		-0.3	V_{CL}+.3	V
V_{DD}	Logic supply voltage		-0.3	V_{DG}+35	V
V_{DG}	Logic supply offset voltage		V_{LS}-3.8	V_{LS}+3.8	V
V_{IN}	Logic input voltage(HIN & LIN)		V_{SS}-.3	V_{DD}+.3	V
dV_S/dt	Allowable offset supply voltage transient			50	V/ns
P_D	Package power dissipation@ $T_A \leq 25C$	(IX6R11S3/P7)		1.25	W
		(IX6R11S6)		1.4	W
P_D	Package power dissipation@ $T_C \leq 25C$	(IX6R11S3/P7)		2.5	W
		(IX6R11S6)		31	W
R_{THJA}	Thermal resistance, junction-to-ambient	(IX6R11S3/P7)		100	K/W
		(IX6R11S6)		90	K/W
R_{THJc}	Thermal resistance, junction-to-case	(IX6R11S3/P7)		50	K/W
		(IX6R11S6)		4	K/W
T_J	Junction Temperature			150	°C
T_S	Storage temperature		-55	150	°C
T_L	Lead temperature (soldering, 10 s)			300	°C

Recommended Operating Conditions

Symbol	Definition	Min	Max	Units
V_{CH}	High side floating supply absolute voltage	V_{HS}+10	V_{HS}+20	V
V_{HS}	High side floating supply offset voltage	-20	650	V
V_{HGO}	High side floating output voltage	V_{HS}	V_{CH}+20	V
V_{CL}	Low side fixed supply voltage	10	20	V
V_{LGO}	Low side output voltage	0	V_{CC}	V
V_{DD}	Logic supply voltage	V_{DG}+3	V_{DG}+20	V
V_{DG}	Logic supply voffset voltage	V_{LS}-1	V_{LS}+1	V
V_{IN}	Logic input voltage(HIN, LIN, ENbar)	V_{DG}	V_{DD}	V
T_A	Ambient Temperature	-40	125	°C

Ordering Information	
Part Number	**Package Type**
IX6R11P7	14-PIN DIP
IX6R11S3	16-PIN SOIC
IX6R11S6	18-PIN SOIC-CT

Dynamic Electrical Characteristics

Symbol	Definition	Test Conditions	Min	Typ	Max	Units
t_{on}	Turn-on propagation delay	V_{HS}= 0V, C_{load}= 2nF		120	170	ns
t_{off}	Turn-off propagation delay	V_{HS}= 600V, C_{load}= 2nF		94	125	ns
t_{enb}	Device not enable delay			110	140	ns
t_r	Turn-on rise time	C_{load}= 2nF		25	35	ns
t_f	Turn-off fall time	C_{load}= 2nF		17	25	ns
t_{dm}	Delay matching, HS & LS turn-on/off	C_{load}= 2nF		10	20	ns

Static Electrical Characteristics

Symbol	Definition	Test Conditions	Min	Typ	Max	Units
V_{INH}	Logic “1” input voltage, HIN	V_{DD}= V_{CL}= 15V	9.5			V
V_{INL}	Logic “0” input voltage, LIN	V_{DD}= V_{CL}= 15V	0		6	V
V_{INH}	NOT ENABLE, ENB	V_{CL}= 15V	9.5			V
V_{INL}	NOTENABLE, ENB	V_{CL}= 15V	0		6	V
V_{HLGO} / V_{HHGO}	High level output voltage, V_{CH}-V_{HGO} or V_{CL}-V_{LGO}	I_O= 0A			0.1	V
V_{LLGO} / V_{LHGO}	High level output voltage, V_{HGO} or V_{LGO}	I_O= 0A			0.1	V
I_{HL}	HS to LS bias current.	V_{HS}= V_{CH}= 600V		170		µA
I_{QHS}	Quiescent V_{CH} supply current	V_{IN}= 0V or V_{DD}		1	3	mA
I_{QLS}	Quiescent V_{CL} supply current	V_{IN}= 0V or V_{DD}		1	3	mA
I_{QDD}	Quiescent V_{DD} supply current	V_{IN}= 0V or V_{DD}		15	30	uA
I_{IN}+	Logic “1” input bias current	V_{IN}= V_{DD}		20	40	uA
I_{IN}-	Logic “0” input voltage	V_{IN}= 0V			1	uA
V_{CHUV}+	V_{CH} supply undervoltage positive going threshold.		7.5	8.6	9.7	V
V_{CHUV}-	V_{CH} supply undervoltage negative going threshold.		7	8.2	9.4	V
V_{CLUV}+	V_{CL} supply undervoltage positive going threshold		7.4	8.5	9.6	V
V_{CLUV}-	V_{CL} supply undervoltage negative going threshold.		7	8.2	9.4	V
I_{GO}+	HS or LS Output low short circuit current; V_{GO}= 15V, V_{IN}= 0V, PW<10us		6	7		A
I_{GO}-	HS or LS Output low short circuit current; V_{GO}= 15V, V_{IN}=0V, PW<10us			-7	-6	A

Timing Waveform Definitions

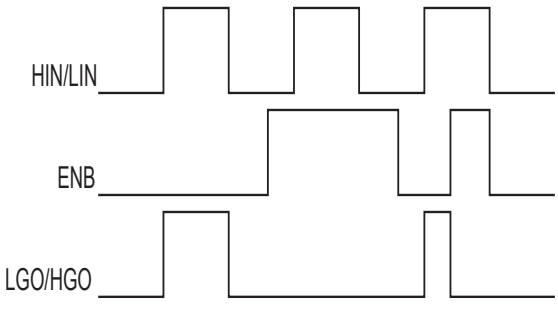


Figure 3. INPUT/OUPUT Timing Diagram

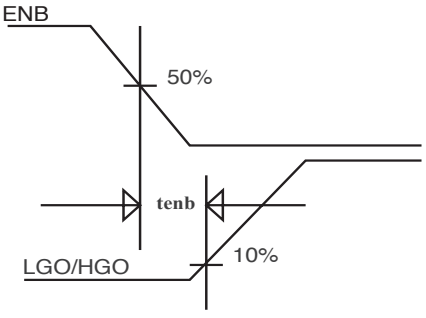


Figure 4. ENABLE Waveform Definitions

Timing Waveform Definitions

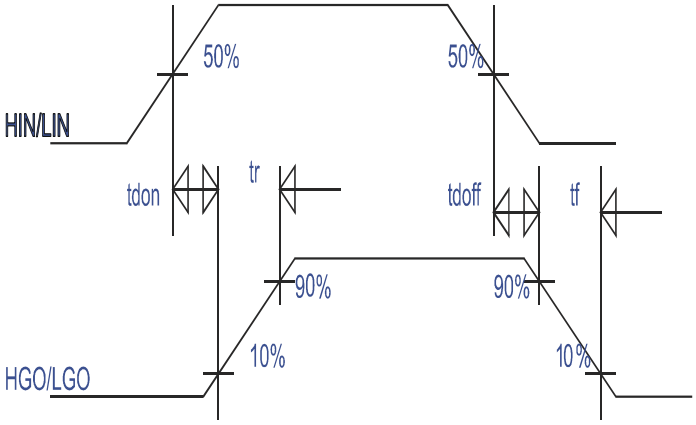


Figure 5. Definitions of Switching Time Waforms

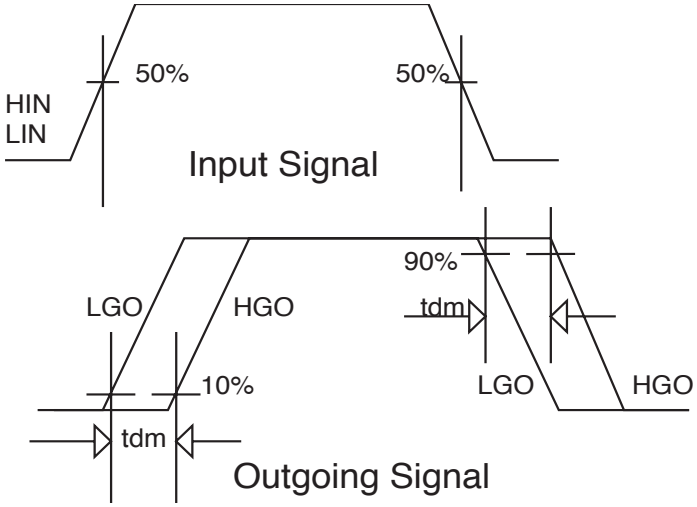


Figure 6. Definitions of Delay Matching Waveforms

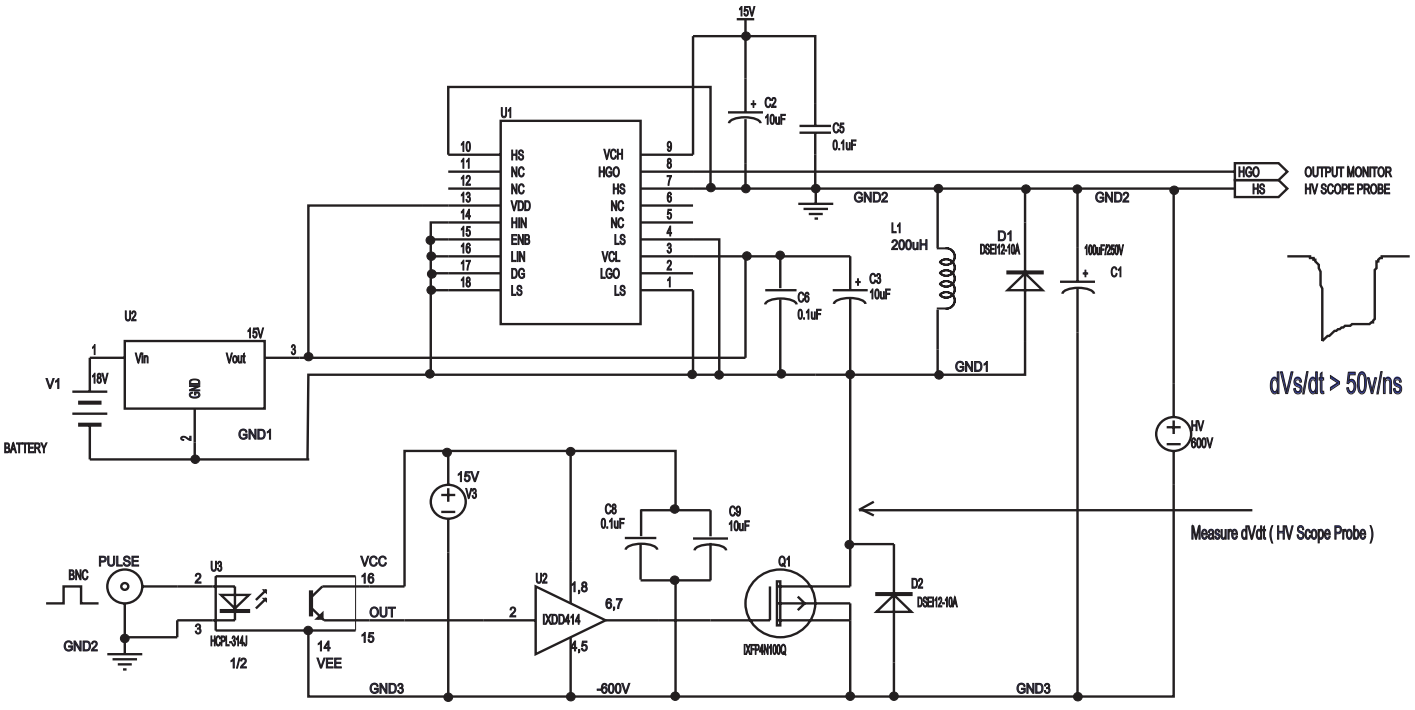


Figure 7. Test circuit for allowable offset supply voltage transient.

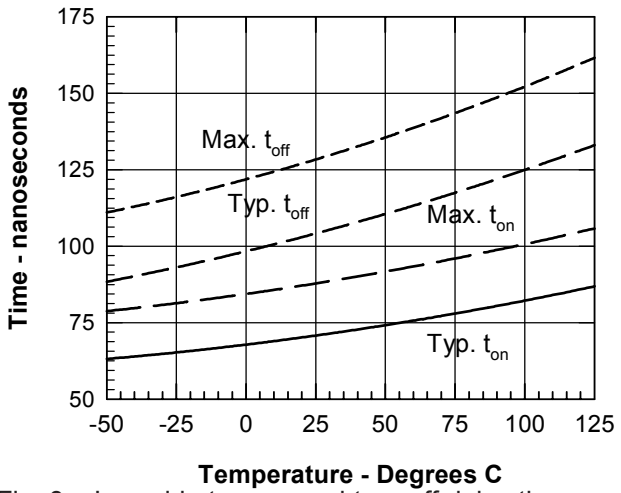


Fig. 8a. Low side turn-on and turn-off delay times vs. temperature.

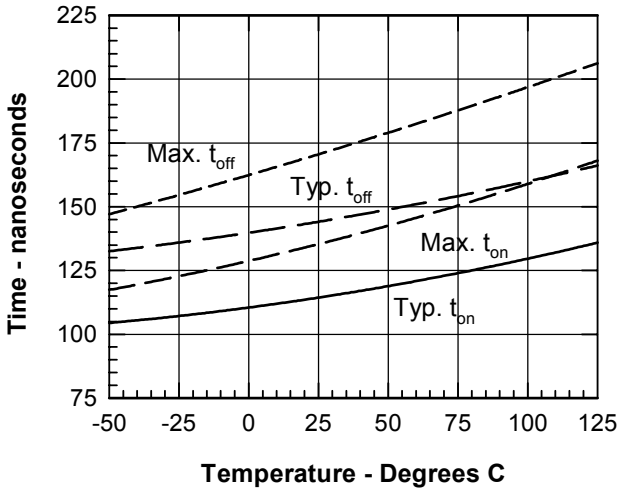


Fig. 8b. High side turn-on and turn-off times vs. temperature.

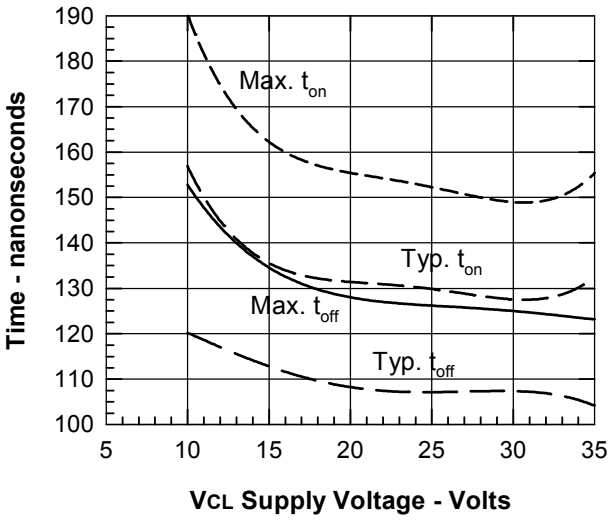


Fig. 9a. Low side turn-on and turn-off delay times vs. V_{CL}.

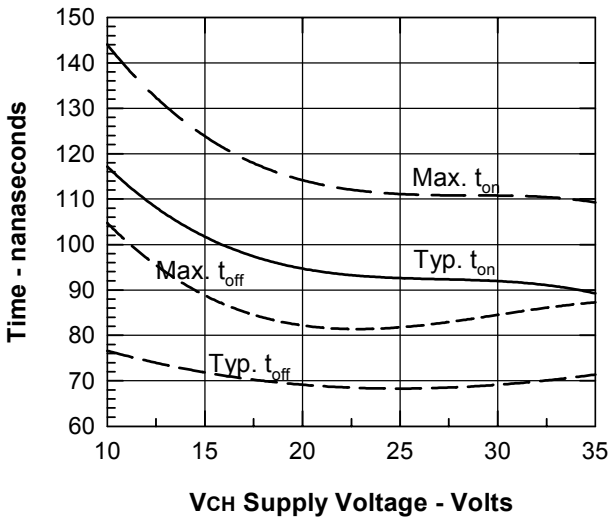


Fig. 9b. High side turn-on and turn-off delay times vs. V_{CH}.

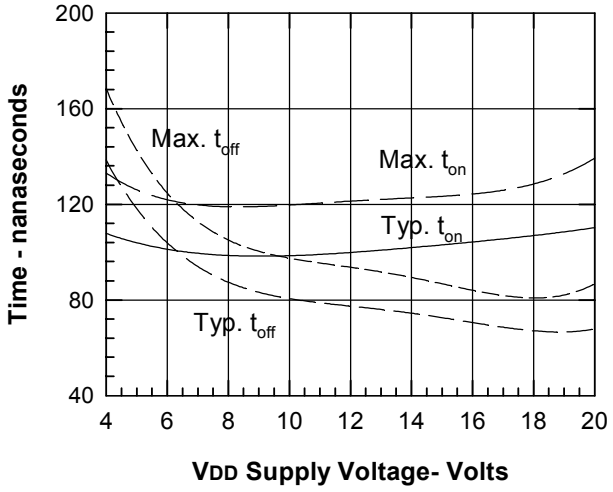


Fig. 10a. Low side turn-on and turn-off delay times vs. V_{DD} supply voltage.

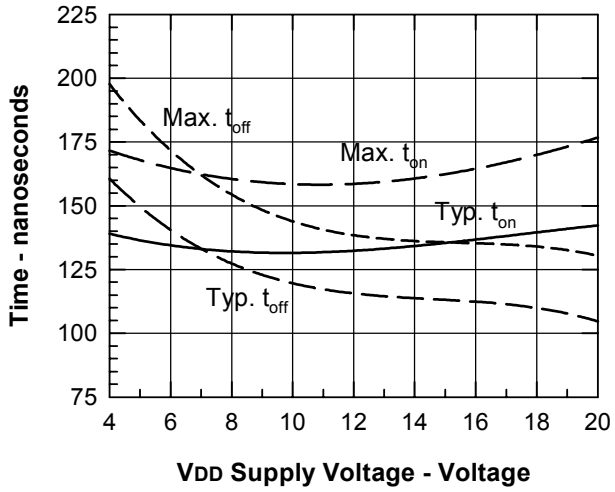


Fig. 10b. High side turn-on and turn-off delay times vs. V_{DD}.

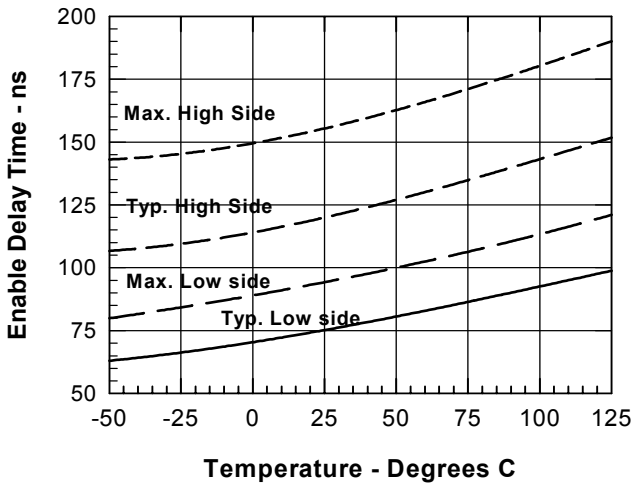


Fig. 11a. High and Low side ENABLE (Shutdown) times vs. temperature.

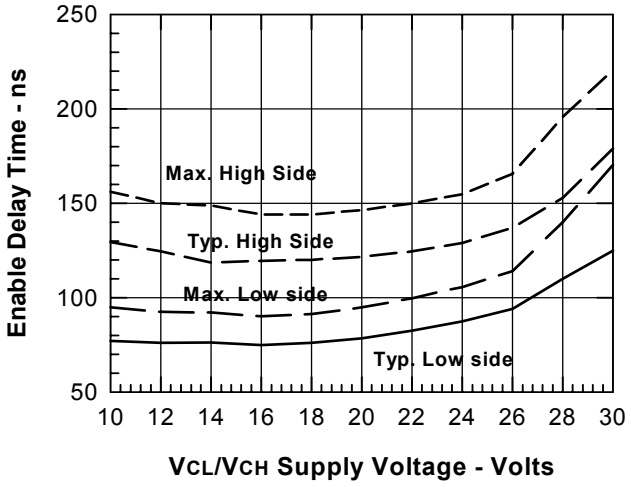


Fig.11b. High and Low side ENABLE (Shutdown) times vs. supply voltage.

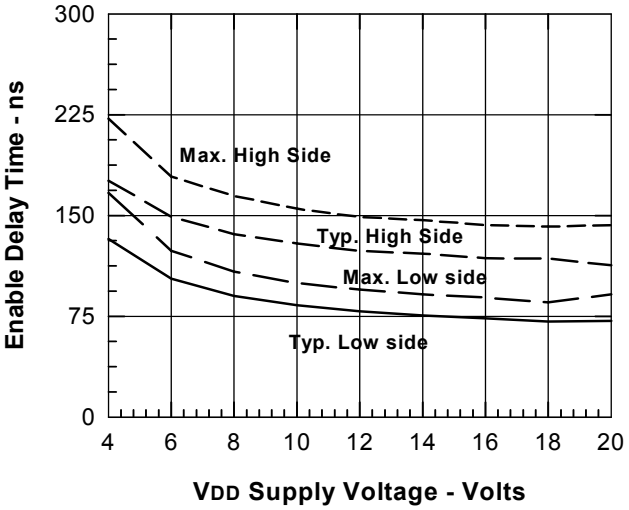


Fig. 11c. High and Low side ENABLE (Shutdown) times vs. supply voltage.

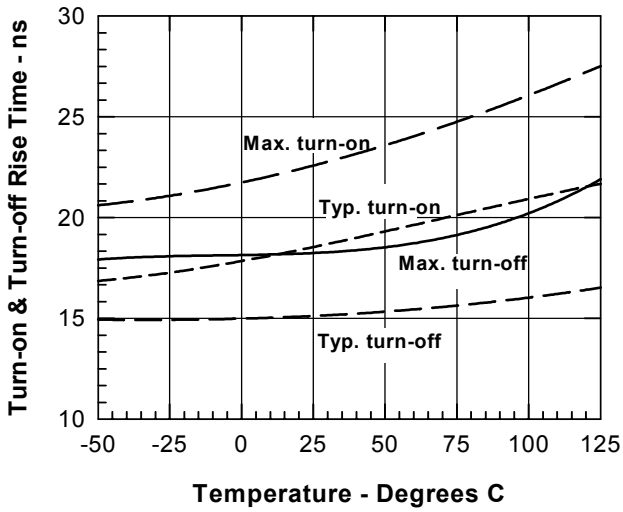


Fig. 12a. Turn-on and turn-off rise times vs. temperature.

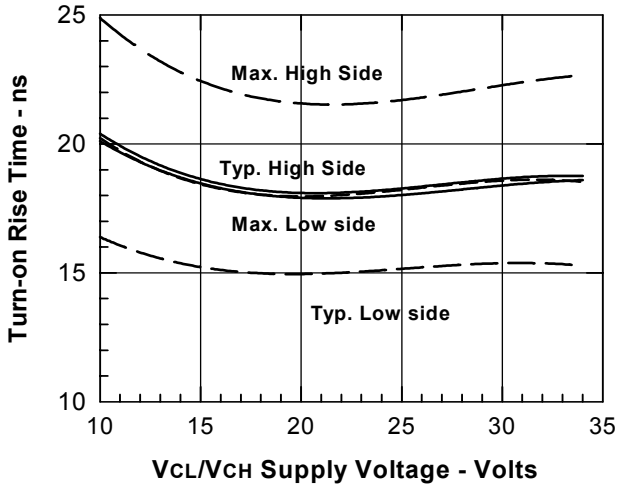


Fig. 12b. Turn-on rise times vs. bias supply voltages.

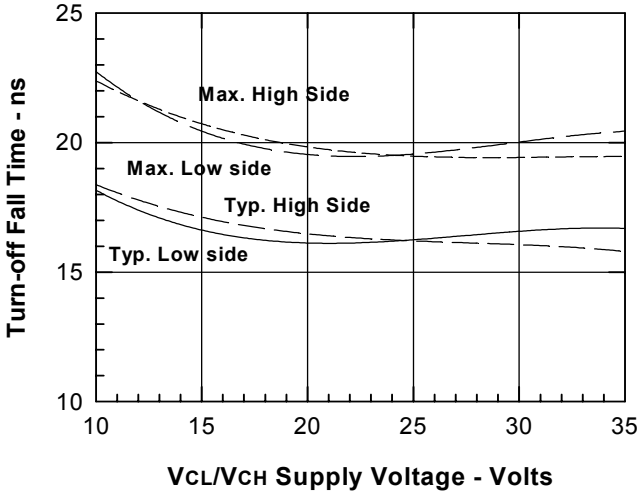


Fig. 12c. Turn-off delay times vs. bias supply voltages.

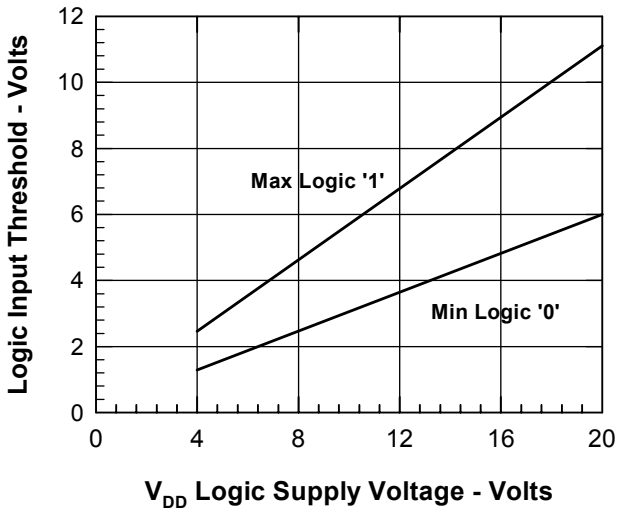


Fig. 13. Logic input threshold voltage vs bias supply voltage.

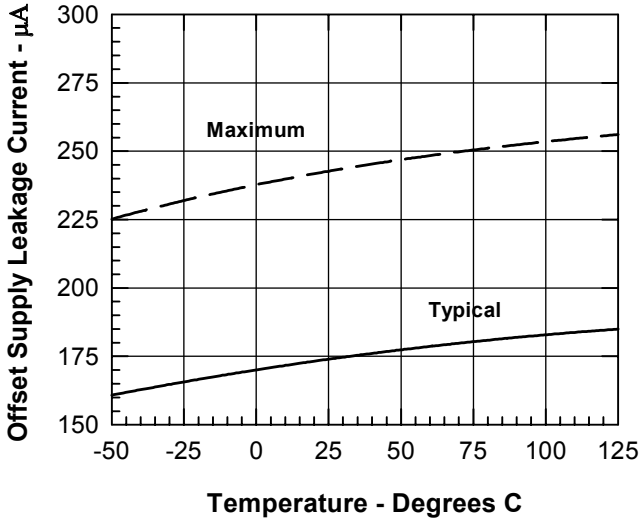


Fig. 14. Offset supply leakage current vs. temperature.

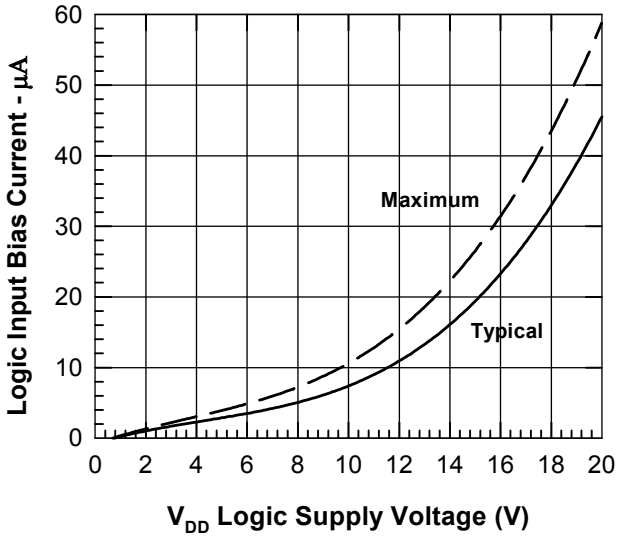


Fig. 15. Logic input current vs. bias voltage.

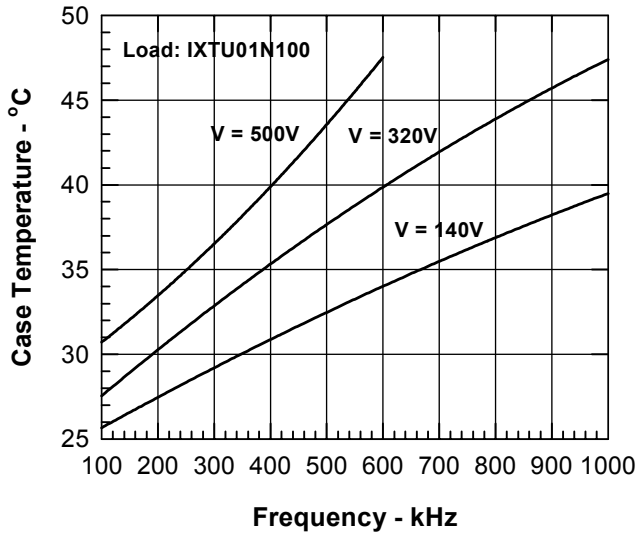


Fig. 16. IX6R11S3 Case temperature rise vs. operating frequency

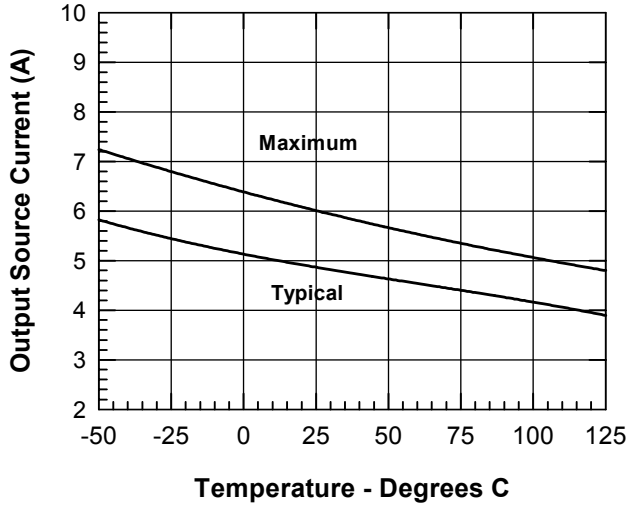


Fig. 17a. Output source current vs. temperature

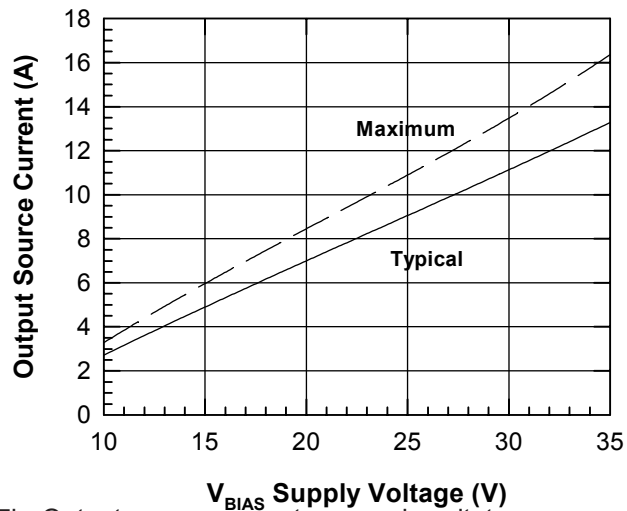


Fig. 17b. Output source current vs supply voltatge

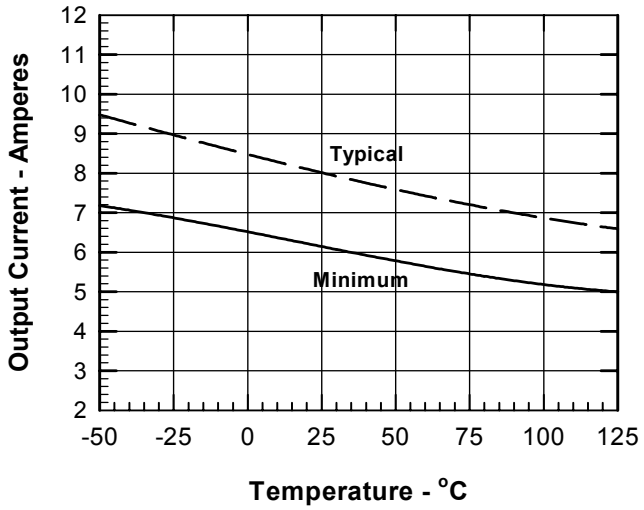


Fig. 18a. Output sink current vs. temperature

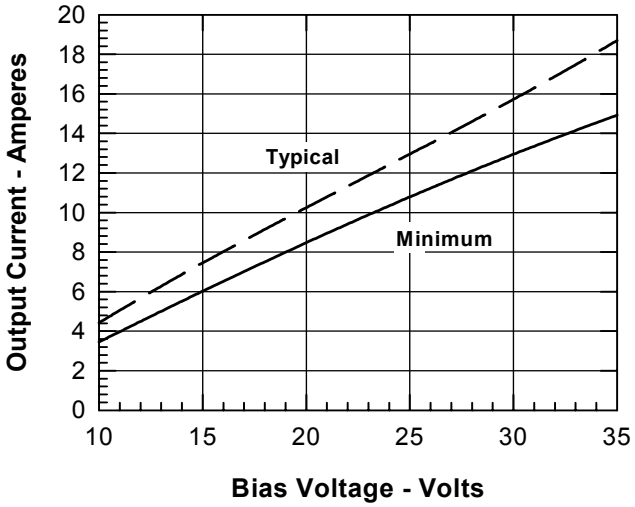


Fig. 18b. Output sink current vs. bias voltage

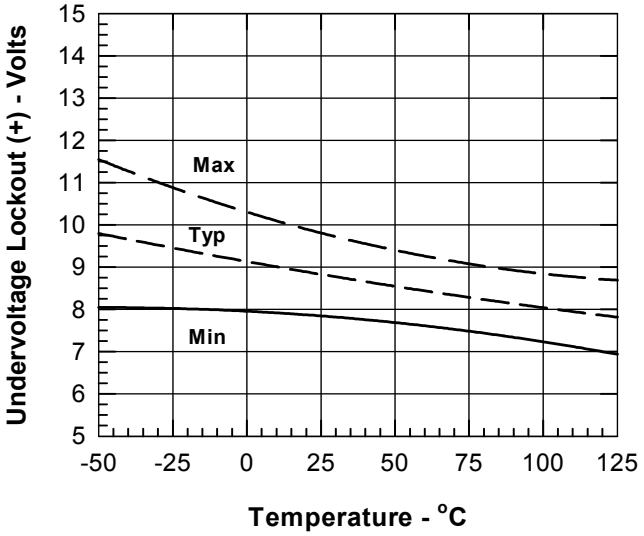


Fig. 19a. V_{CH} Undervoltage positive trip vs. temperature.

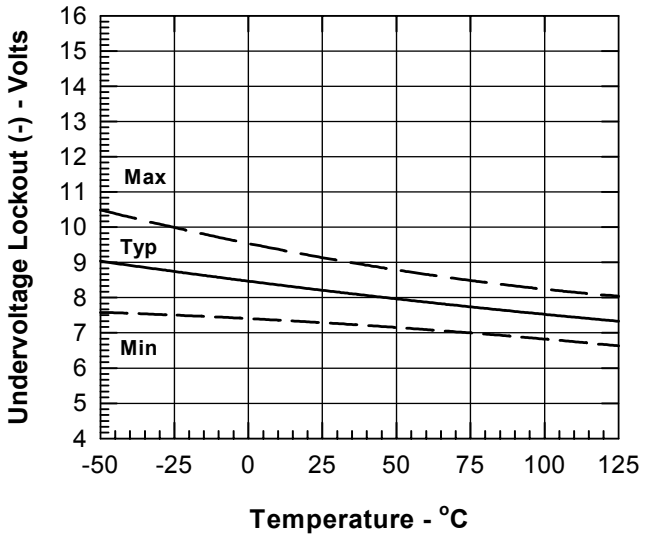


Fig. 19b. V_{CH} Undervoltage negative trip vs. temperature.

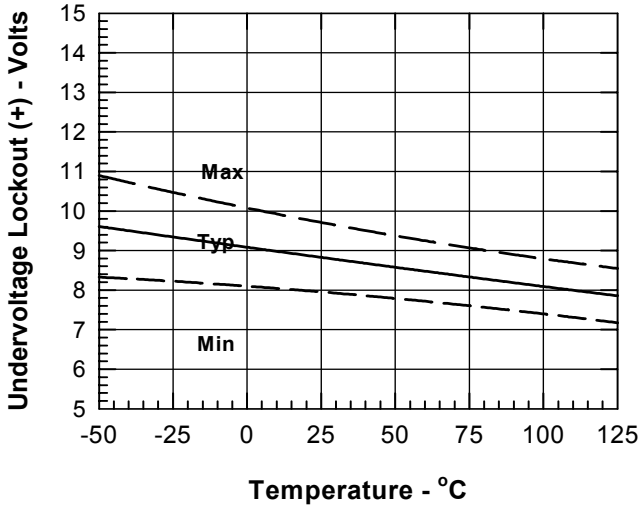


Fig. 20a. V_{CL} Undervoltage positive trip vs. temperature.

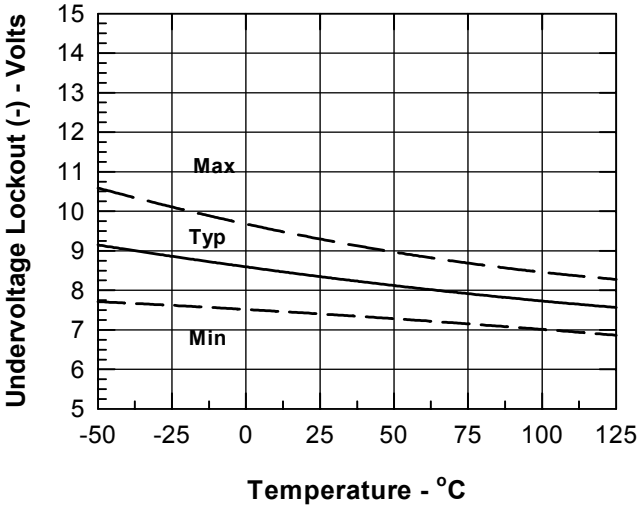


Fig. 20b. V_{CL} Undervoltage negative trip vs. temperature.

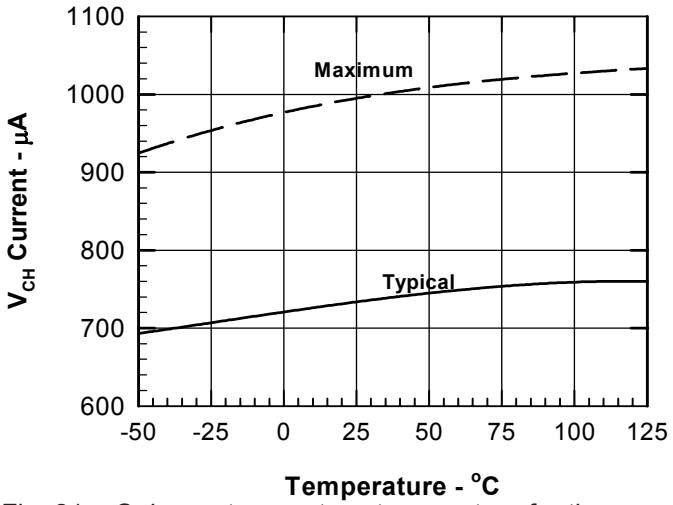


Fig. 21a. Quiescent current vs. temperature for the high side power supply.

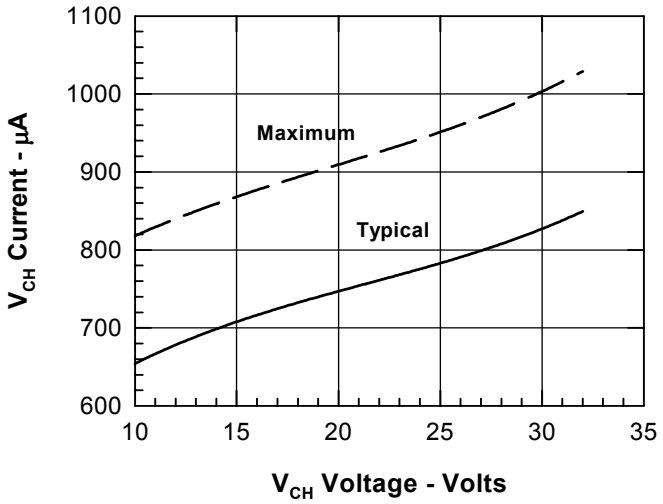


Fig. 21b. Quiescent current vs. voltage for the high side power supply.

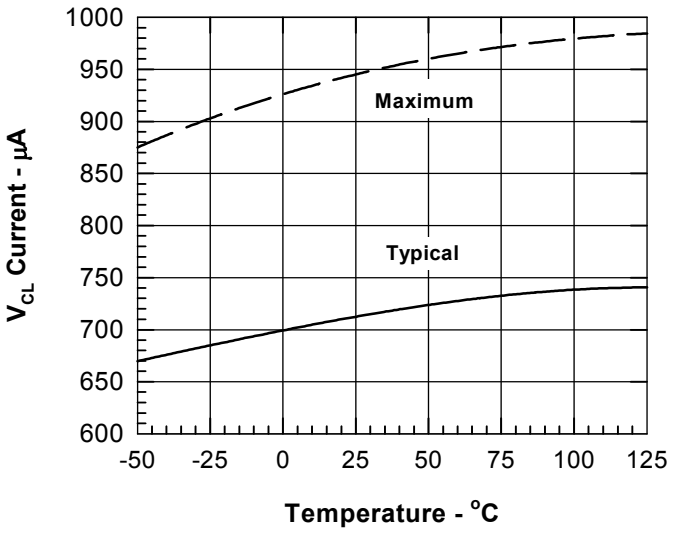


Fig. 22. Quiescent current vs. temperature for the low side power supply

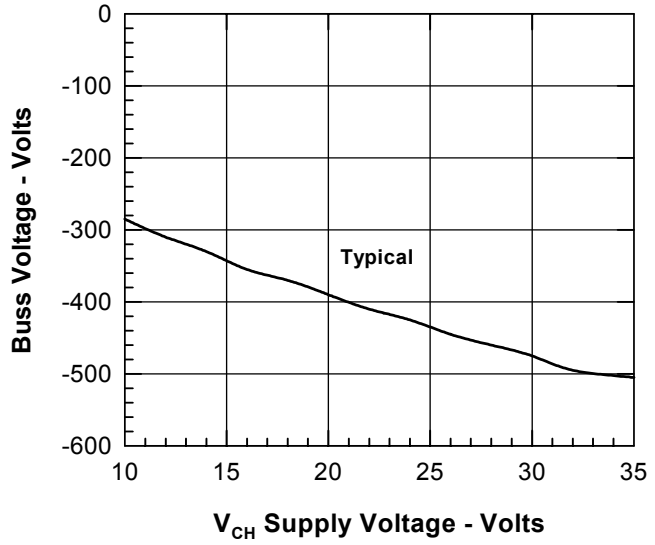


Fig. 23. BUS voltage vs. V_{CH} supply voltage

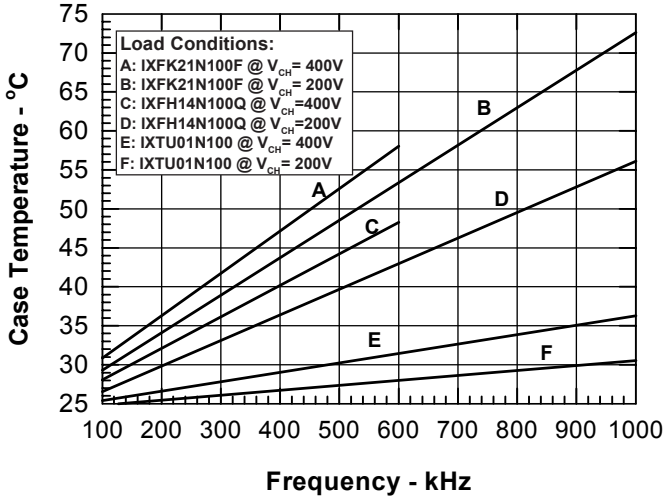


Fig. 24a. Case temperature rise vs. switching frequency for IX6R11S6

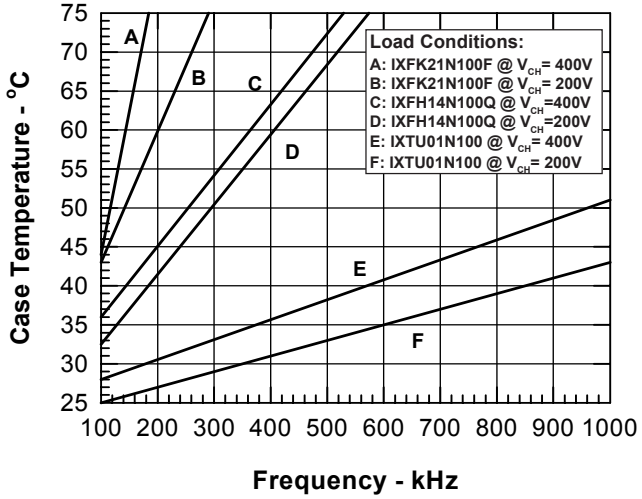
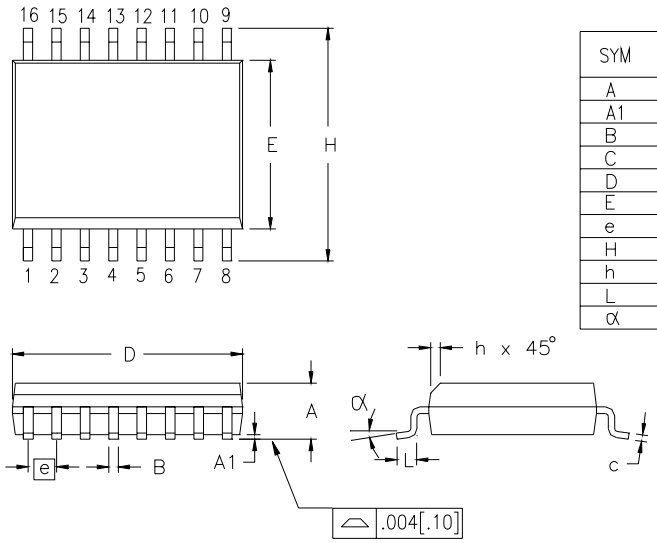


Fig. 24b. Case temperature rise vs. switching frequency for IX6R11S3

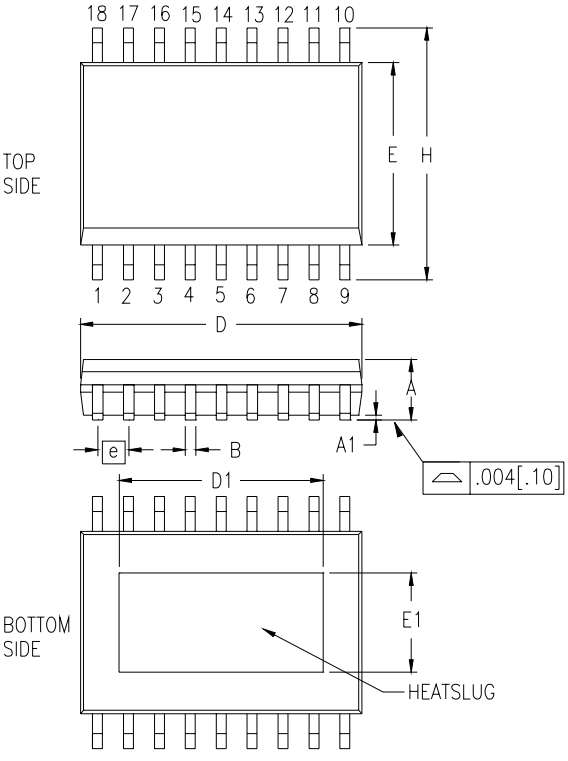
IX6R11S3 Package Outline



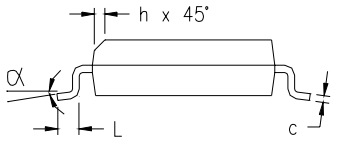
SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.093	.104	2.35	2.65
A1	.004	.012	.10	.30
B	.013	.020	.33	.51
C	.009	.013	.23	.32
D	.398	.413	10.10	10.50
E	.291	.299	7.40	7.60
e	.050BSC		1.27BSC	
H	.394	.419	10.00	10.65
h	.010	.029	.25	.75
L	.016	.050	.40	1.27
α	0°	8°	0°	8°

NOTE: This drawing will meet all dimensions requirement of JEDEC MS-013 AA.

IX6R11S6 Package Outline

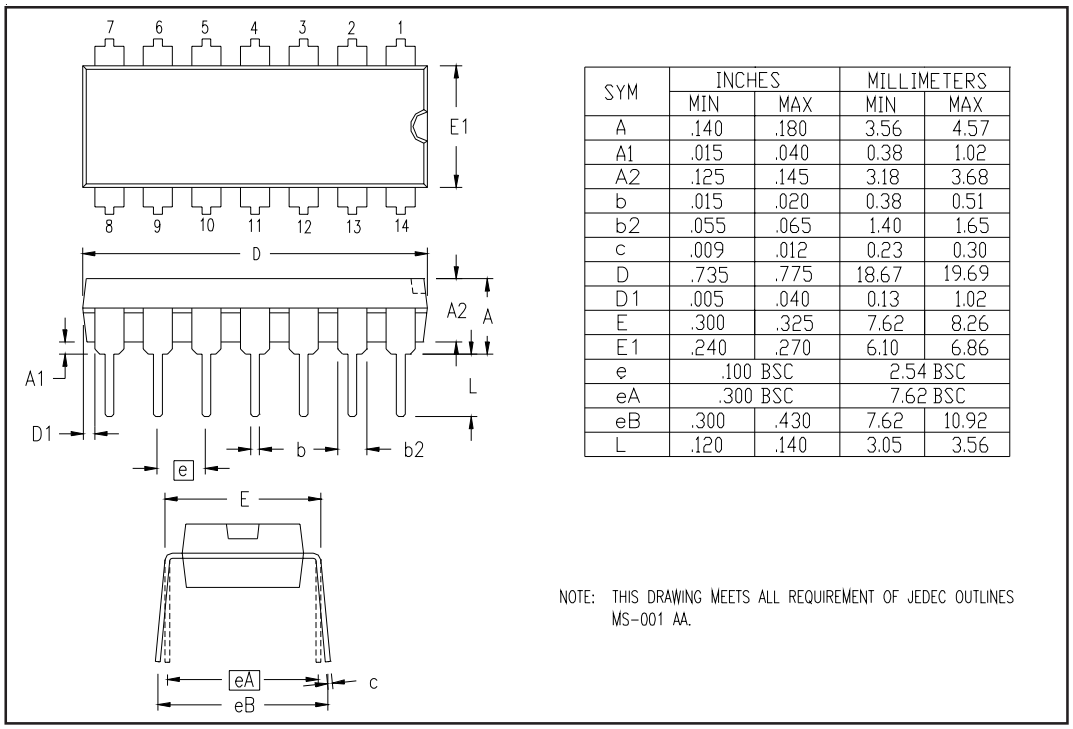


SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.093	.104	2.35	2.65
A1	.004	.012	.10	.30
B	.013	.020	.33	.51
C	.009	.013	.23	.32
D	.447	.462	11.35	11.73
D1	.310	.350	7.87	8.89
E	.291	.299	7.40	7.60
E1	.140	.180	3.56	4.57
e	.050 BSC		1.27 BSC	
H	.394	.419	10.00	10.65
h	.010	.029	.25	.75
L	.016	.050	.40	1.27
α	0°	8°	0°	8°



NOTE: This drawing will meet all dimensions requirement of JEDEC MS-013 AB.

IX6R11P7 Package Outline



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.140	.180	3.56	4.57
A1	.015	.040	0.38	1.02
A2	.125	.145	3.18	3.68
b	.015	.020	0.38	0.51
b2	.055	.065	1.40	1.65
c	.009	.012	0.23	0.30
D	.735	.775	18.67	19.69
D1	.005	.040	0.13	1.02
E	.300	.325	7.62	8.26
E1	.240	.270	6.10	6.86
e	.100 BSC		2.54 BSC	
eA	.300 BSC		7.62 BSC	
eB	.300	.430	7.62	10.92
L	.120	.140	3.05	3.56

NOTE: THIS DRAWING MEETS ALL REQUIREMENT OF JEDEC OUTLINES MS-001 AA.

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