TEMIC
Semiconductors

U6081B

PWM Power Control with Low Duty Cycle Switch Off

Description

U6081B is a PWM IC in bipolar technology for the control of an N-channel power MOSFET used as a high side switch. The IC is ideal for the use in the brightness control (dimming) of lamps e.g., in dashboard applications.

Features

- Pulse width modulation up to 2 kHz clock frequency

- Protection against short circuit, load dump overvoltage and reverse V_S

- Duty cycle 0 to 100%

- Output stage for power MOSFET

- Interference and damage protection according to VDE 0839 and ISO/TR 7637/1.

- Ground wire breakage protection

- Charge pump noise suppressed

Ordering Information

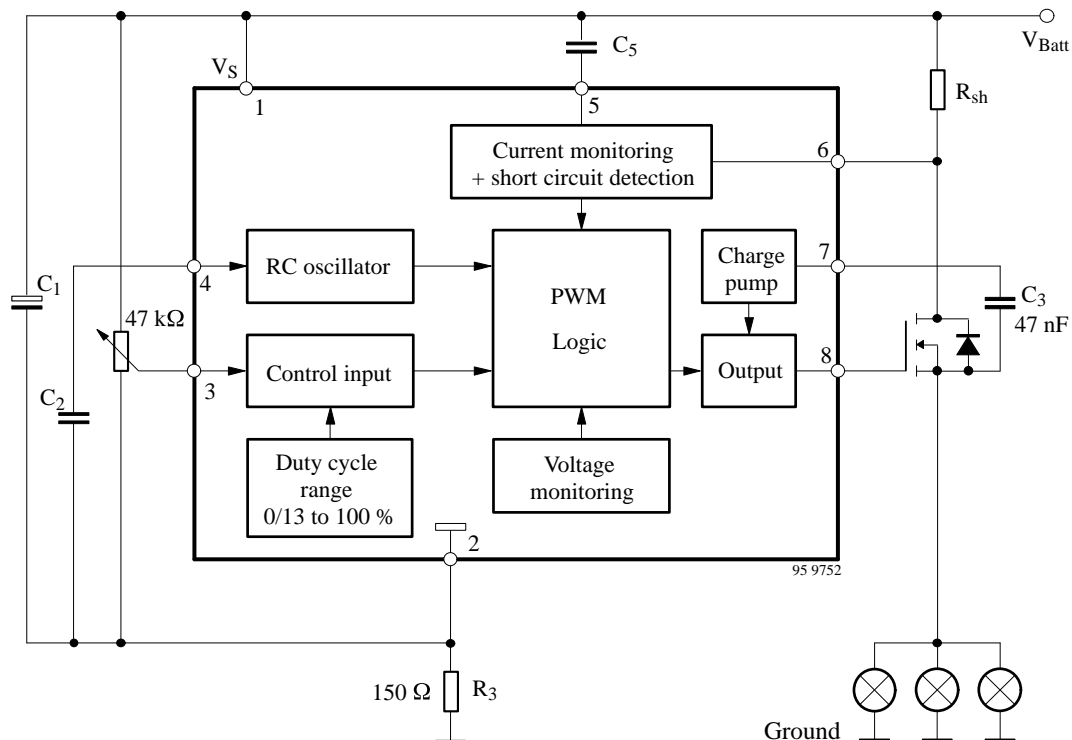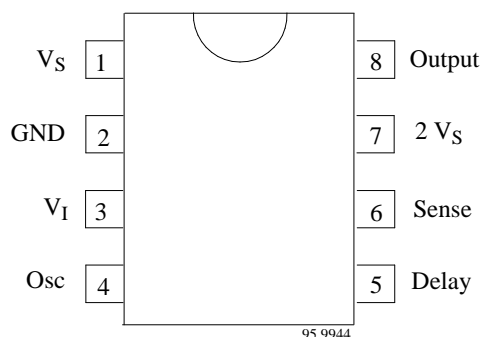| Extended Type Number	Package	Remarks
U6081B	DIP8	

Block Diagram

Figure 1. Block diagram with external circuit

Pin Description

V_S [1] ⌒ [8] Output
GND [2] [7] 2 V_S
V_I [3] [6] Sense
Osc [4] [5] Delay

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Pin	Symbol	Function
1	V_S	Supply voltage V_S
2	GND	IC ground
3	V_I	Control input (duty cycle)
4	Osc	Oscillator
5	Delay	Short circuit protection delay
6	Sense	Current sensing
7	2 V_S	Voltage doubler
8	Output	Output

Functional Description

Pin 1, Supply Voltage, V_s or V_{Batt}

Overvoltage Detection

Stage 1:
If $V_{Batt} > 20$ V occurs the external transistor will be switched off and switched on again at $V_{Batt} < 18.5$ V (hysteresis).

Stage 2:
If $V_{Batt} > 28$ V, the external transistor is switched on again (load-dump protection). At the same time the voltage limitation of the IC is reduced from $V_S \approx 26$ V to $V_S \approx 20$ V. This leads to a hysteresis characteristic so that the load-dump detection is switched off again only at $V_{Batt} < 23$ V. In this case the short–circuit protection is not in operation.

Undervoltage Detection

In the event of voltages of approximately $V_{Batt} < 5.0$ V, the external FET is switched off and the latch for short-circuit detection is reset.

A hysteresis ensures that the FET is switched on again at approximately $V_{Batt} \geqq 5.4$ V.

Pin 2, GND

Ground-Wire Breakage

To protect the FET in the case of ground-wire breakage, a 820-kΩ resistor between gate and source is recommended to provide proper switch-off conditions.

Pin 3, Control Input

The pulse width is controlled by means of an external potentiometer (47 kΩ). The characteristic (angle of rotation/duty cycle) is linear. The duty cycle can be varied from 0 to 100%. To avoid inadmissibly high filament cold currents, the dimmer is switched off at duty cycles of approximately < 10% or is switched on only at duty cycles of approximately > 13% (hysteresis). It is possible to further restrict the duty cycle with the resistors R_1 and

R_2 (see figure 2). Pin 3 is protected against short-circuit to V_{Batt} and ground GND ($V_{Batt} \leqq 16.5$ V).

Output Slope Control

The rise and fall time (t_r, t_f) of the lamp voltage can be limited to reduce radio interference. This is done with an integrator which controls a power MOSFET as source follower. The slope time is controlled by an external capacitor C4 and the oscillator current (see figure 2).

Calculation:

$$t_f = t_r = V_{Batt} \times \frac{C_4}{I_{osc}}$$

With $V_{Batt} = 12$ V, $C_4 = 470$ pF and $I_{osc} = 40$ μA, we thus obtain a controlled slope of

$$t_f = t_r = 12 \text{ V} \times \frac{470 \text{ pF}}{40 \text{ μA}} = 141 \text{ μs}$$

A 100-Ω resistor in series to C4 is recomended to damp device oscillations (see figure 2).

Pin 4, Oscillator

The oscillator determines the frequency of the output voltage. This is defined by an external capacitor, C_2. It is charged with a constant current, I, until the upper switching threshold is reached. A second current source is then activated which taps a double current, $2 \times I$, from the charging current. The capacitor, C_2, is thus discharged by the current, I, until the lower switching threshold is reached. The second source is then switched off again and the procedure starts again.

Example for oscillator frequency calculation:

$$V_{T100} = V_S \times \alpha_1 = (V_{Batt} - I_S \times R_3) \times \alpha_1$$

$$V_{T<100} = V_S \times \alpha_2 = (V_{Batt} - I_S \times R_3) \times \alpha_2$$

$$V_{TL} = V_S \times \alpha_3 = (V_{Batt} - I_S \times R_3) \times \alpha_3$$

where

V_{T100} = High switching threshold (100% duty cycle)

$V_{T<100}$ = High switching threshold($<$ 100% duty cycle)

V_{TL} = Low switching threshold

α_1, α_2 and α_3 are fixed constant.

The above mentioned threshold voltages are calculated for the following values given in the data sheet.

V_{Batt} = 12 V, I_S = 4 mA, R_3 = 150 Ω ,
$\alpha_1 = 0.7$, $\alpha_2 = 0.67$ and $\alpha_3 = 0.28$.

$V_{T100} = (12\ V - 4\ mA \times 150\ \Omega) \times 0.7 \approx 8\ V$

$V_{T<100} = 11.4\ V \times 0.67 = 7.6\ V$

$V_{TL} = 11.4\ V \times 0.28 = 3.2\ V$

For a duty cycle of 100%, an oscillator frequency, f, is as follows:

$$f = \frac{I_{osc}}{2 \times (V_{T100} - V_{TL}) \times C_2} , \quad \text{whereas } C_2 = 22\ nF$$
$$\text{and } I_{osc} = 40\ \mu A$$

Therefore:

$$f = \frac{40\ \mu A}{2 \times (8\ V - 3.2\ V) \times 22\ nF} = 189\ Hz$$

For a duty cycle of less than 100%, the oscillator frequency, f, is as follows:

$$f = \frac{I_{osc}}{2 \times (V_{T<100} - V_{TL}) \times C_2 + 4 \times V_{Batt} \times C_4}$$

whereas $\quad C_4 = 470\ pF$

$$f = \frac{40\ \mu A}{2 \times (7.6\ V - 3.2\ V) \times 22\ nF + 4 \times 12\ V \times 470\ pF}$$

$= 185\ Hz$

A selection of different values of C_2 and C_4, provides a range of oscillator frequency, f, from 10 to 2000 Hz.

Pins 5 and 6, Short-Circuit Protection and Current Sensing

1. Short-Circuit Detection and Time Delay, t_d

The lamp current is monitored by means of an external shunt resistor. If the lamp current exceeds the threshold for the short-circuit detection circuit ($V_{T2} \approx 90$ mV), the duty cycle is switched over to 100% and the capacitor C_5 is charged by a current source of 20 μA ($I_{ch} - I_{dis}$). The external FET is switched off after the cut-off threshold (V_{T5}) is reached. Renewed switching on the FET is possible only after a power-on reset. The current source, I_{dis}, ensures that the capacitor C_5 is not charged by parasitic currents. The capacitor C_5 is discharged by I_{dis} to typ. 0.7 V.

Time delay, t_d, is as follows:

$t_d = C_5 \cdot (V_{T5} - 0.7\ V)/(I_{ch} - I_{dis})$

With C_5 = 330 nF and V_{T5} = 9.8 V, ($I_{ch} - I_{dis}$) = 20 μA, we have

$t_d = 330\ nF \cdot (9.8\ V - 0.7\ V)/20\ \mu A$

$= 150\ ms.$

2. Current Limitation

The lamp current is limited by a control amplifier to protect the external power transistor. The voltage drop across an external shunt resistor acts as the measured variable. Current limitation takes place for a voltage drop of $V_{T1} \approx 100$ mV. Owing to the difference $V_{T1} - V_{T2} \approx 10$ mV it is ensured that current limitation occurs only when the short circuit detection circuit has responded.

After a power-on reset, the output is inactive for an half oscillator cycle. During this time, the supply voltage capacitor can be charged so that the current limitation is guaranteed in the event of a short circuit when the IC is switched on for the first time.

Pins 7 and 8, Charge Pump and Output

Output, Pin 8, is suitable for controlling a power MOSFET. During the active integration phase, the supply current of the operational amplifier is mainly supplied by the capacitor C_3 (bootstrapping). Additionally, a trickle charge is generated by an integrated oscillator ($f_7 \approx 400$ kHz) and a voltage doubler circuit. This permits a gate voltage supply at a duty cycle of 100%.

Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Junction temperature	T_j	150	°C
Ambient temperature range	T_{amb}	–40 to +110	°C
Storage temperature range	T_{stg}	–55 to +125	°C

Thermal Resistance

Parameters	Symbol	Maximum	Unit
Junction ambient	R_{thJA}	120	K/W

Electrical Characteristics

T_{amb} = –40 to +110°C, V_{Batt} = 9 to 16.5 V, (basic function is guaranteed between 6.0 V to 9.0 V) reference point is ground, unless otherwise specified (see figure 1). All other values refer to Pin GND (Pin 2).

Parameters	Test Conditions / Pins	Symbol	Min	Typ	Max	Unit
Current consumption	Pin 1	I_S			6.8	mA
Supply voltage	Overvoltage detection, stage 1	V_{Batt}			25	V
Stabilized voltage	I_S = 10 mA Pin 1	V_Z	24.5		27.0	V
Battery undervoltage detection	ON OFF	V_{Batt}	4.4 4.8	5.0 5.4	5.6 6.0	V
Battery overvoltage detection Pin 2						
Stage 1:	– on – off	V_{Batt}	18.3 16.7	20.0 18.5	21.7 20.3	V
Stage 2:	– on – off	V_{Batt}	25.5 19.5	28.5 23.0	32.5 26.5	V
Stabilized voltage	I_S = 30 mA Pin 1	V_Z	18.5	20.0	21.5	V
Short-circuit protection Pin 6						
Short-circuit current limitation	$V_{T1} = V_S - V_6$	V_{T1}	85	100	120	mV
Short-circuit detection	$V_{T2} = V_S - V_6$	V_{T2}	75	90	105	mV
		$V_{T1} - V_{T2}$	3	10	30	mV
Delay timer short-circuit detection, V_{Batt} = 12 V Pin 5						
Switched off threshold	$V_{T5} = V_S - V_5$	V_{T5}	9.5	9.8	10.1	V
Charge current		I_{ch}		23		µA
Discharge current		I_{dis}		3		µA
Capacitance current	$I_5 = I_{ch} - I_{dis}$	I_5	13	20	27	mA
Voltage doubler Pin 7						
Voltage	Duty cycle 100%	V_7	$2\,V_S$			
Oscillator frequency		f_7	280	400	520	kHz
Internal voltage limitation	I_7 = 5 mA	V_7	26	27.5	30.0	V
	(whichever is lower)	V_7	V_{S+14}	V_{S+15}	V_{S+16}	V

Parameters	Test Conditions / Pins	Symbol	Min	Typ	Max	Unit
Switch-off at small duty cycles $V_{Batt} = 12$ V Pin 3						
Output disabled		V_3/V_S	0.3	0.32	0.34	
Output active		V_3/V_S	0.32	0.34	0.36	
Hysteresis switch-on		$\Delta V_3/V_S$	0.004		0.032	
Gate output Pin 8						
Voltage	Low level	V_8	0.35	0.70	0.95	V
	$V_{Batt} = 16.5$ V, $T_{amb} = 110°C, R_3 = 150\ \Omega$				1.5 *)	
	High level, duty cycle 100%	V_8		V_7		
Current	$V_8 =$ Low level	I_8	1.0			mA
	$V_8 =$ High level, $I_7 > \mid I_8 \mid$		−1.0			
Oscillator						
Frequency	Pin4	f	10		2000	Hz
Threshold cycle Upper	$V_8 =$ High, $\alpha_1 = \dfrac{V_{T100}}{V_S}$	α_1	0.68	0.7	0.72	
	$V_8 =$ Low, $\alpha_2 = \dfrac{V_{T<100}}{V_S}$	α_2	0.65	0.67	0.69	
Lower	$\alpha_3 = \dfrac{V_{TL}}{V_S}$	α_3	0.26	0.28	0.3	
Oscillator current	$V_{Batt} = 12$ V	$\pm I_{osc}$	34	45	54	µA
Frequency tolerance	C_4 open, $C_2 = 470$ nF, duty cycle = 50%	f	6.0	9.9	13.5	Hz

*) Reference point is battery ground

Package Information

Package DIP8

Dimensions in mm

technical drawings
according to DIN
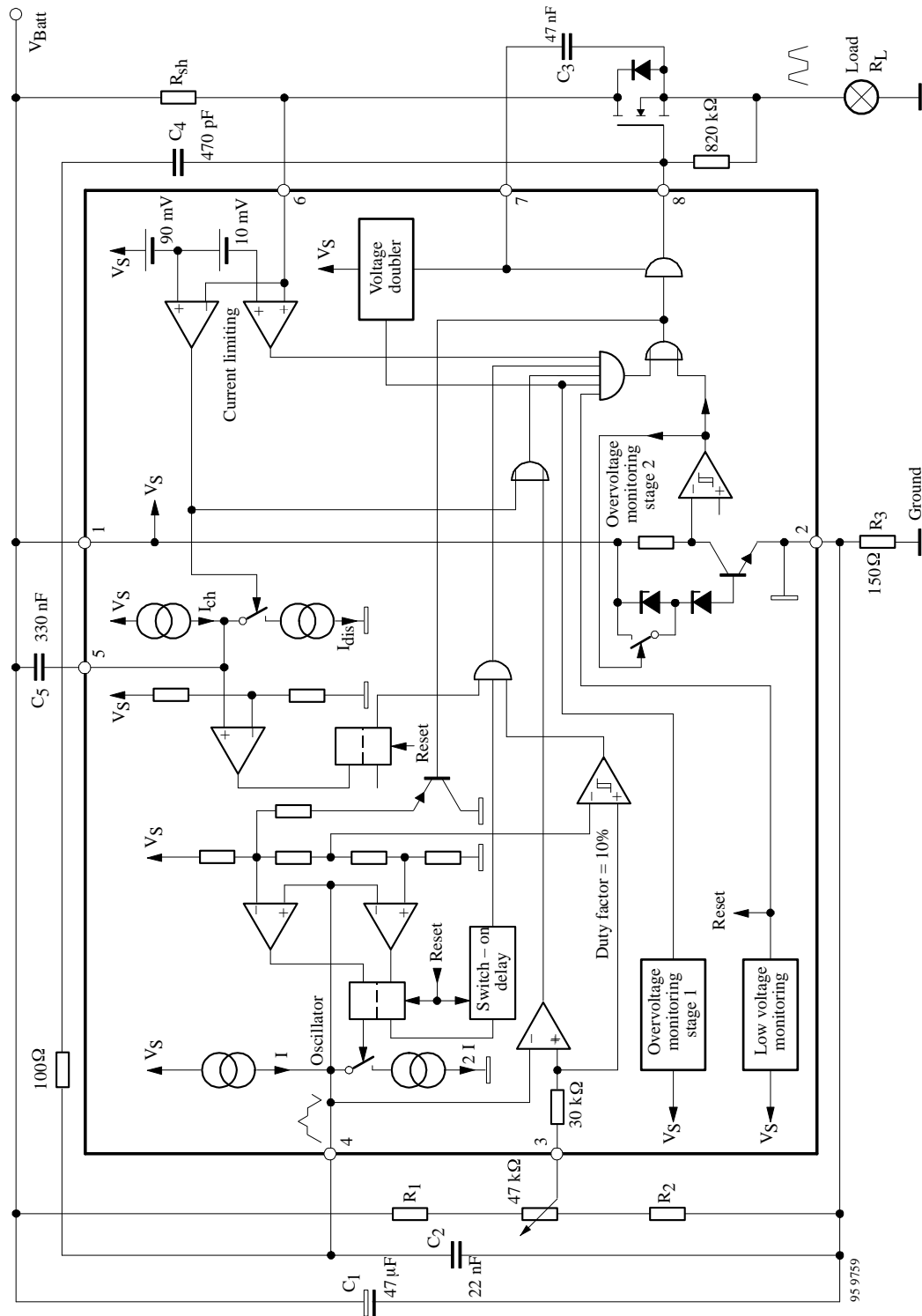specifications

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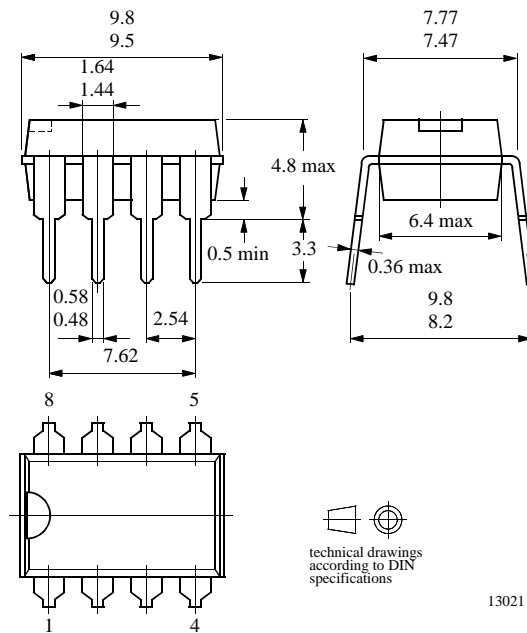
Application

Figure 2.

Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC TELEFUNKEN microelectronic GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC TELEFUNKEN microelectronic GmbH semiconductor division has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

We reserve the right to make changes to improve technical design and may do so without further notice. Parameters can vary in different applications. All operating parameters must be validated for each customer application by the customer. Should the buyer use TEMIC products for any unintended or unauthorized application, the buyer shall indemnify TEMIC against all claims, costs, damages, and expenses, arising out of, directly or indirectly, any claim of personal damage, injury or death associated with such unintended or unauthorized use.

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