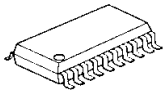
Unipolar Stepper Motor Driver

GENERAL DESCRIPTION

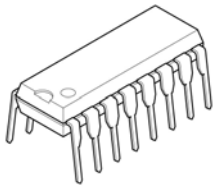
The NJW4351 is a high efficiency DMOS unipolar stepper motor driver IC. Compared to previous devices, it is more suitable for low voltage operation, capable of handling 5.0V, 3.3V and the like logic circuits. Drive Stage consists of DMOS which produces high efficiency and low heat generation motor drive circuit.

The motor can be controlled by the STEP and DIR system. Further more, to improve controllability of system, MO, ENABLE, RESET and PD function are included, various applications are possible.

PACKAGE OUTLINE



NJW4351VC3

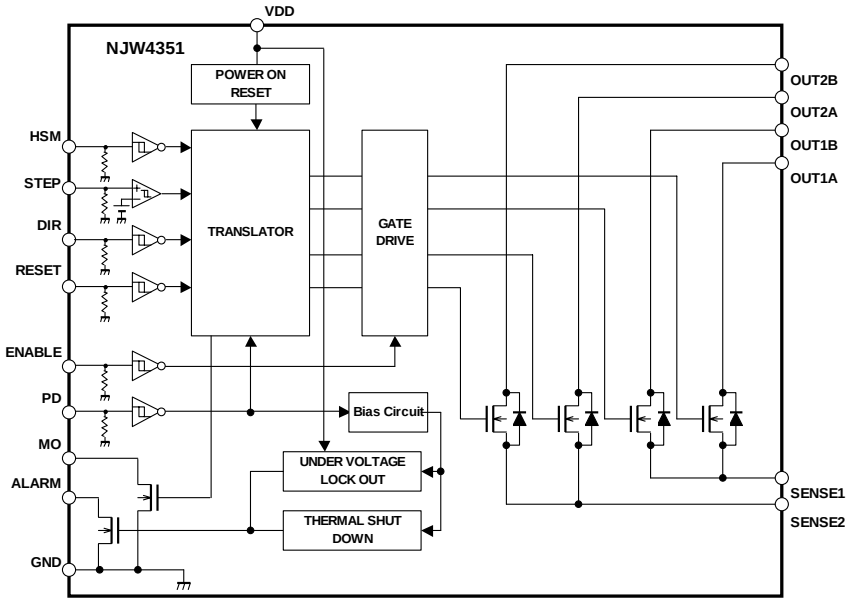


NJW4351D

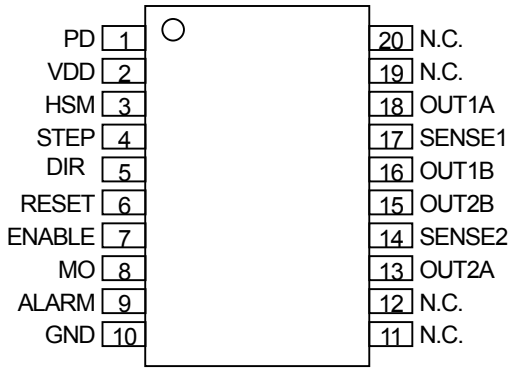
FEATURES

- Supply Voltage V_{DD}=2.7 to 5.5V
  V_{MM}= to 55V
- Output Current Io=1.5A peak at V_{DD}=5V
- Low Quiescent Current I_{DD}=500μA typ.
- STEP&DIR Input Operation (Internal Translator)
- HALF/FULL Mode Generation
- TTL compatible Input With Schmitt-Comparator
- ENABLE Function
- RESET Function
- MO (Motor Origin Monitor) -Position-indication Output
- PD (Standby) Function
- Under Voltage Lock Out
- Thermal Shutdown Circuit
- Alarm Output Function (As the protection circuit operates)
- BCD Technology
- Package Outline SSOP20-C3, DIP16

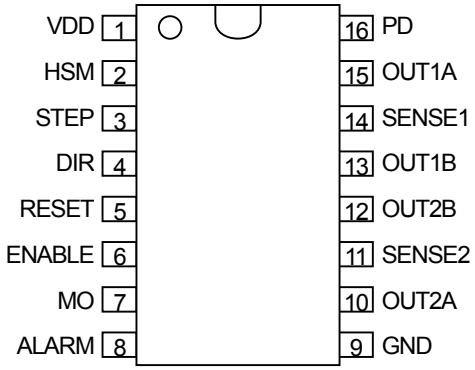
BLOCK DIAGRAM



□ PIN CONNECTION



SSOP20-C3



DIP16

□ PIN FUNCTION LIST

Pin#		Terminal Name	Function	Remark
SSOP20-C3	DIP16			
1	16	PD	Power Saving State Setting Input Terminal	L=Standby, H=Normal Operation
2	1	VDD	Logic Voltage Supply Terminal	Logic Voltage Supply
3	2	HSM	HALF/FULL Step Mode Setting Input Terminal	L=FULL, H=HALF
4	3	STEP	Stepping Pulse Input Terminal	The Translator is triggered by positive edge of STEP Pulse.
5	4	DIR	Direction Setting Input Terminal	L=FORWARD, H=REVERSE
6	5	RESET	Reset Input Terminal	L=The Translator is initialized, H=Normal Operation
7	6	ENABLE	Phase Output Off Input Terminal	L=ACTIVE, H=Normal Operation
8	7	MO	MO Output Terminal	When the Translator is in initial status, L level is to output.
9	8	ALARM	Internal Protection Operation Detection Output Terminal	When the internal protection operation is detected, L level is to output.
10	9	GND	Logic Ground Terminal	Logic Ground
11,12,19,20	-	N.C.	No Connection	No Connection
13	10	OUT2A	2ch Output Terminal A	—
14	11	SENSE2	Current Detection Resistance Connection Terminal 2	It connects resistance for the detection of the side of 2ch. At the unused time, it connects with GND.
15	12	OUT2B	2ch Output Terminal B	—
16	13	OUT1B	1ch Output Terminal B	—
17	14	SENSE1	Current Detection Resistance Connection Terminal 1	It connects resistance for the detection of the side of 1ch. At the unused time, it connects with GND.
18	15	OUT1A	1ch Output Terminal A	—

□ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT	
Logic Supply Voltage	V_{DD}	7	V	VDD PIN
Motor Output Voltage	V_O	55	V	OUT1A/1B/2A/2B PIN
Logic Input Voltage	V_{IN}	7	V	STEP, DIR, HSM, RESET, ENABLE, PD PIN
ALARM Output Voltage	V_{ALARM}	7	V	ALARM PIN
MO Output Voltage	V_{MO}	7	V	MO PIN
Output Current	Io	1.5	A	OUT1A/1B/2A/2B PIN
ALARM Output Current	I_{ALARM}	20	mA	ALARM PIN
MO Output Current	I_{MO}	20	mA	MO PIN
Operating Temperature	Topr	-40 to +85	°C	-
Junction Temperature	Tj	-40 to +150	°C	-
Storage Temperature	Tstg	-50 to +150	°C	-
Power Dissipation (SSOP20-C3)	P_D	1.0	W	(*1) Mounted on 2Layers PCB
		1.5	W	(*1) Mounted on 4Layers PCB
Power Dissipation (DIP16)	P_D	1.2	W	Device itself
		1.4	W	(*1) Mounted on 2Layers PCB
		2.0	W	(*1) Mounted on 4Layers PCB

(*1): Mounted on glass epoxy board based on EIA/JEDEC. (114.3x76.2x1.6mm: 2Layers/4Layers)

□ RECOMMENDED OPERATING CONDITIONS

(Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Logic Supply Voltage	V_{DD}		2.7	3.3	5.5	V
Output Current	Io	V_{DD}=5V	-	500	-	mA
		V_{DD}=3.3V	-	-	500	mA

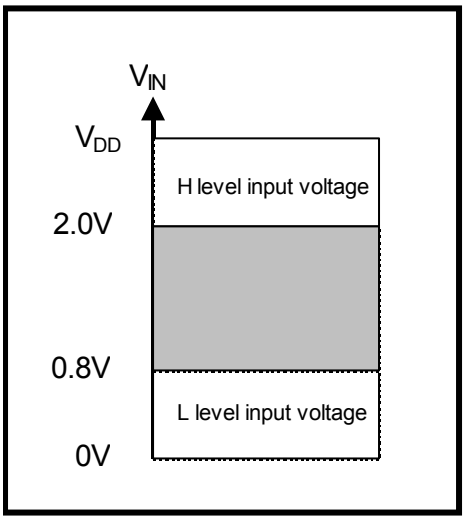
■ ELECTRICAL CHARACTERISTICS

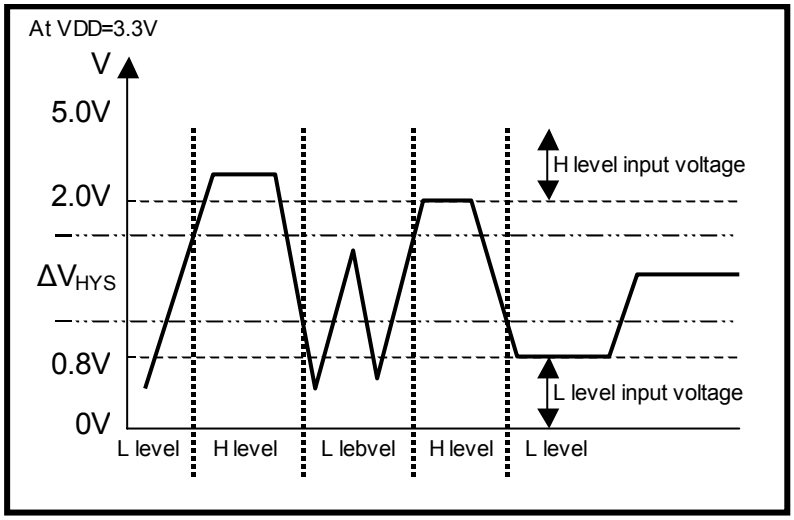
(V_{MM}=24V, V_{DD}=PD=3.3V, R_L=1kΩ, R_{MO}=3.3kΩ, R_{ALARM}=3.3kΩ, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
■ GENERAL						
Quiescent current	I_{DD}	STEP,DIR,HSM,RESET,ENABLE=3.3V, Except I_{IH}	-	0.5	0.8	mA
Quiescent current (Standby)	I_{PD}	PD=0V, except I_{IH}	-	-	1.0	uA
■ INPUT BLOCK1 (STEP)						
H level input voltage1	V_{IH1}		2.0	-	-	V
L level input voltage1	V_{IL1}		0	-	0.8	V
Input hysteresis voltage1	V_{IHYS1}		0.4	0.55	-	V
H level input voltage2	V_{IH2}	V_{DD}=5V	2.4	-	-	V
L level input voltage2	V_{IL2}	V_{DD}=5V	0	-	0.8	V
Input hysteresis voltage2	V_{IHYS2}	V_{DD}=5V	0.4	0.55	-	V
H level input current	I_{IH}	STEP=3.3V	15	33	45	uA
L level input current	I_{IL}	STEP=0V	-	10	20	uA
Input pull down resistance	R_{DOWN}		-	100	-	kΩ
Input pulse widths	tp		2	-	-	us
■ INPUT BLOCK2 (PD/DIR/HSM/RESET/ENABLE)						
H level input voltage1	V_{IH1}		2.0	-	-	V
L level input voltage1	V_{IL1}		0	-	0.8	V
Input hysteresis voltage1	V_{IHYS1}		-	0.13	-	V
H level input voltage2	V_{IH2}	V_{DD}=5V	2.4	-	-	V
L level input voltage2	V_{IL2}	V_{DD}=5V	0	-	0.8	V
Input hysteresis voltage2	V_{IHYS2}	V_{DD}=5V	-	0.14	-	V
H level input current	I_{IH}	PD, DIR, HSM, RESET, ENABLE=3.3V, per input	15	33	45	uA
L level input current	I_{IL}	PD, DIR, HSM, RESET, ENABLE=0V, per input	-200	0	+200	nA
Input pull down resistance	R_{DOWN}		-	100	-	kΩ
Input pulse widths	tp		2	-	-	us
Data setup time	t_{DS}		1	-	-	us
Data hold time	t_{DH}		1	-	-	us
■ MOTOR OUTPUT BLOCK (OUT1A/OUT1B/OUT2A/OUT2B)						
Output ON resistance1	R_{O1}	Io=500mA	-	1.2	1.45	Ω
Output ON resistance2	R_{O2}	V_{DD}=5.0V, Io=500mA	-	0.9	1.25	Ω
Output leak current	I_{OLEAK}	ENABLE=0V,Vo=50V	-	1	5	uA
Delay time	t_{DELAY}	At turn on	-	0.3	-	us
Sense terminal leak current	$I_{SENSELEAK}$	ENABLE=0V, V_{SENSE}=1V(SENSE→GND)	-	-	1	uA
■ MO OUTPUT (MO)						
L level output voltage	V_{MO}	I_{MO}=10mA	-	0.3	0.5	V
MO terminal leak current	I_{MOLEAK}	V_{MO}=5.5V	-	-	1	uA
■ MO OUTPUT (ALARM)						
L level output voltage	V_{ALARM}	I_{ALARM}=10mA	-	0.3	0.5	V
ALARM terminal leak current	$I_{ALARMLEAK}$	V_{ALARM}=5.5V	-	-	1	uA
■ THERMAL SHUTDOWN BLOCK						
Thermal shutdown operating temperature	T_{TSD1}		-	170	-	°C
Thermal shutdown recovery temperature	T_{TSD2}		-	140	-	°C
Thermal shutdown hysteresis	ΔT_{TSD}		-	30	-	°C
■ UNDER VOLTAGE LOCK OUT BLOCK						
UVLO operating voltage	V_{UVLO1}		1.6	1.9	2.2	V
UVLO recovery voltage	V_{UVLO2}		1.9	2.2	2.5	V
UVLO hysteresis voltage	ΔV_{UVLO}		0.2	0.3	0.4	V

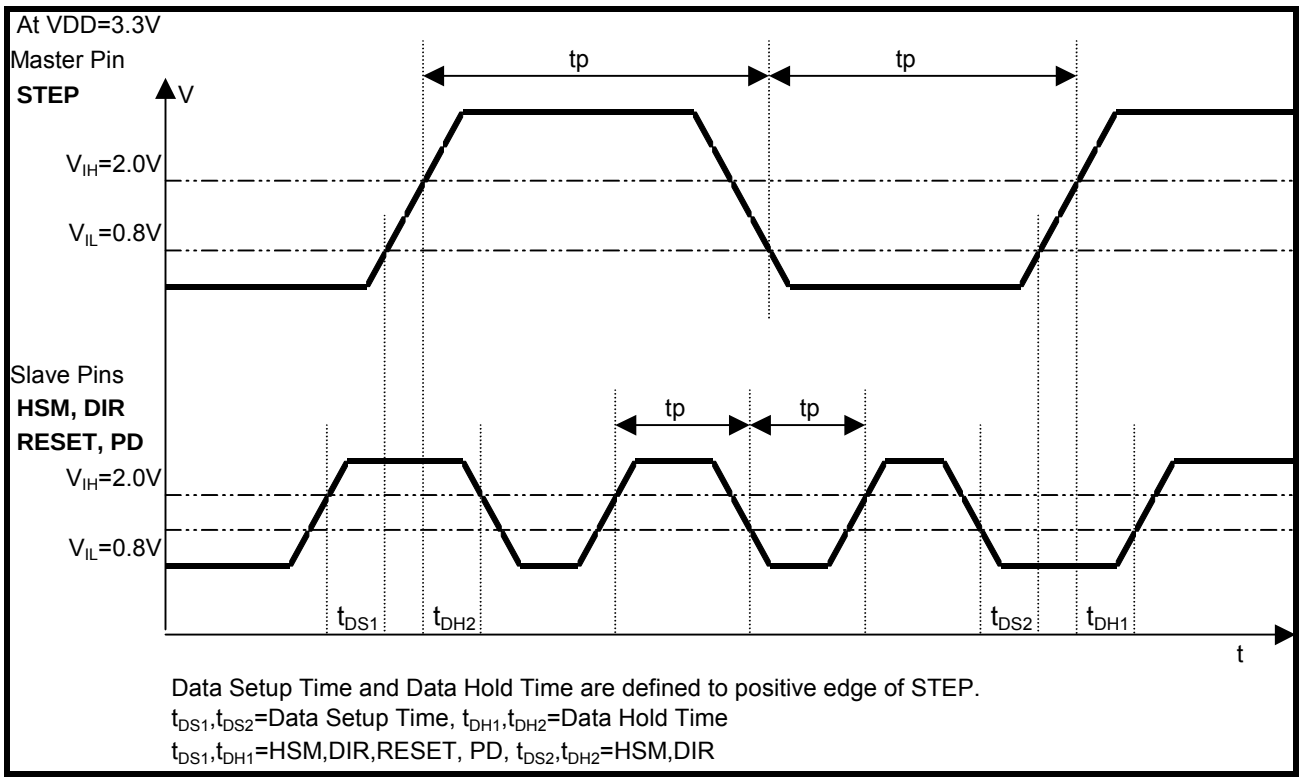
□ PIN/ CIRCUIT OPERATIONAL DEFINITION

♦ Logic Input Pins Operational Voltage Definition



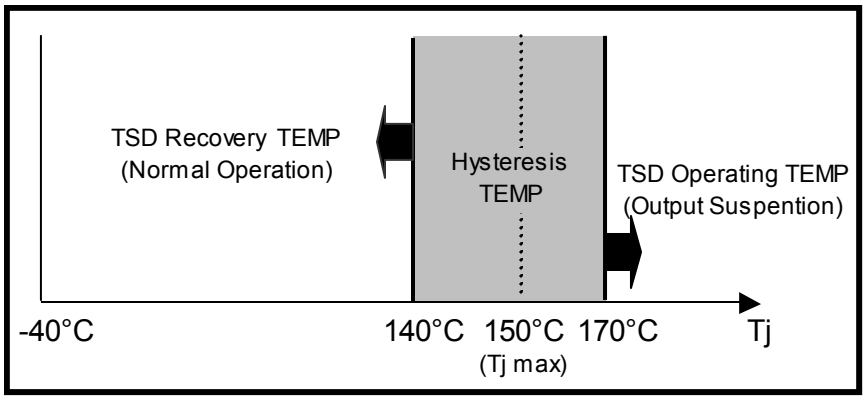


♦ Logic Input Pins Timing Definition

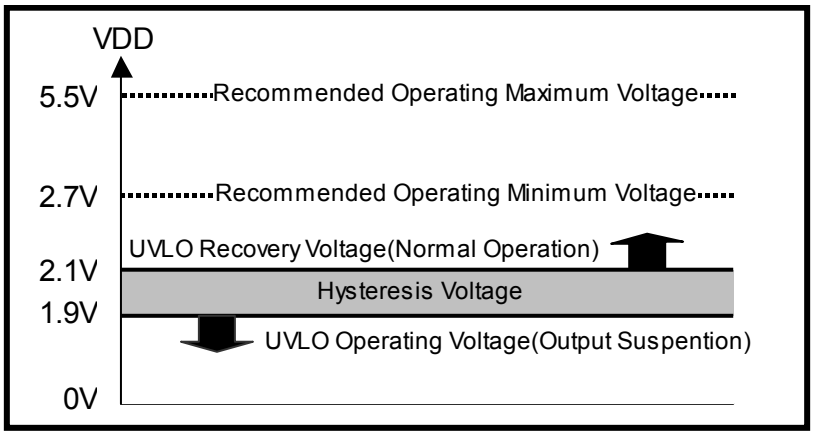


Data Setup Time and Data Hold Time are defined to positive edge of STEP.
t_{DS1},t_{DS2}=Data Setup Time, t_{DH1},t_{DH2}=Data Hold Time
t_{DS1},t_{DH1}=HSM,DIR,RESET, PD, t_{DS2},t_{DH2}=HSM,DIR

♦ Thermal Shutdown Operational Definition



♦ Under Voltage Protection Operational Definition



□ TERMINAL STATUS

STEP-Motor Stepping Pulse Input

STEP	Function
Negative Edge	-
Positive Edge	Internal translator gose on every this edge
OPEN	-

MO-Motor Origin Position Output

MO	Function
H	The translator is in noninitial status
L	The translator is in initial status

HSM-HALF/FULL Step Mode Input

HSM	Function
H	HALF Step
L	FULL Step
OPEN	FULL Step (Inside PULL DOWN)

ALARM-Alarm Output

ALARM	Function
H	Normal Operation
L	OUT terminals are OFF, as the protection circuit operates.

DIR-Direction Command Input

DIR	Function
H	REVERSE
L	FORWARD
OPEN	FORWARD (Inside PULL DOWN)

ENABLE-Enable Input

ENABLE	Function
H	ACTIVE
L	OUT terminals are OFF , but internal logic circuit is ON.
OPEN	OUT terminals are OFF , but internal logic circuit is ON. (Inside PULL DOWN)

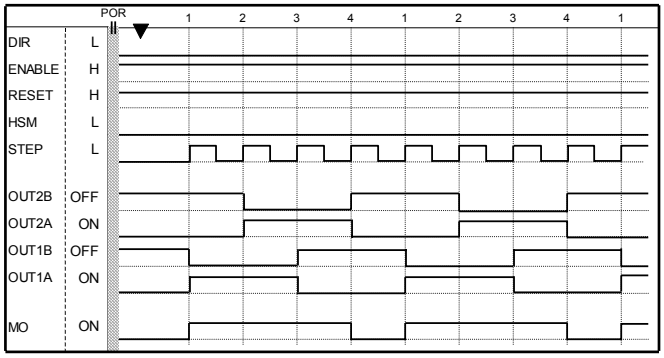
RESET-Reset Input

RESET	Function
H	ACTIVE
L	RESET
OPEN	RESET (Inside PULL DOWN)

PD-Power Down State Input

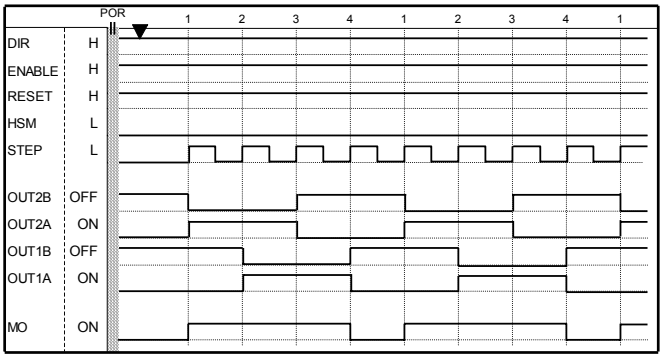
PD	Function
H	ACTIVE
L	RESET+POWER SAVING
OPEN	RESET+POWER SAVING (Inside PULL DOWN)

□ TIMING CHART



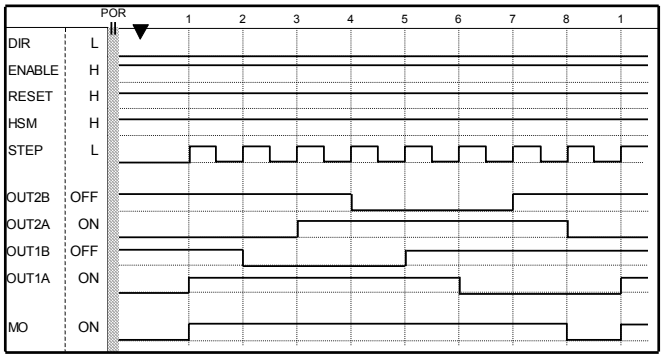
STEP	After POR	1	2	3	4
OUT2B	OFF	OFF	ON	ON	OFF
OUT2A	ON	ON	OFF	OFF	ON
OUT1B	OFF	ON	ON	OFF	OFF
OUT1A	ON	OFF	OFF	ON	ON
MO	ON	OFF	OFF	OFF	ON

Fig.1 Full Step Mode / Forward Direction Sequence



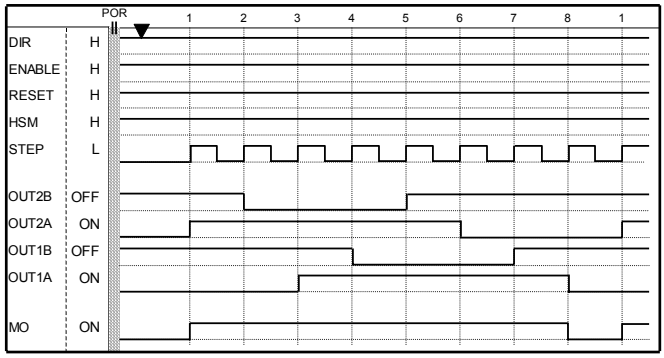
STEP	After POR	1	2	3	4
OUT2B	OFF	ON	ON	OFF	OFF
OUT2A	ON	OFF	OFF	ON	ON
OUT1B	OFF	OFF	ON	ON	OFF
OUT1A	ON	ON	OFF	OFF	ON
MO	ON	OFF	OFF	OFF	ON

Fig.2 Full Step Mode / Reverse Direction Sequence



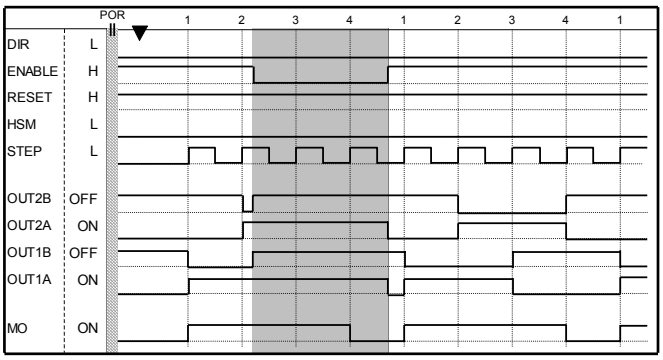
STEP	After POR	1	2	3	4	5	6	7	8
OUT2B	OFF	OFF	OFF	OFF	ON	ON	ON	OFF	OFF
OUT2A	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	ON
OUT1B	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	OFF
OUT1A	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	ON
MO	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON

Fig.3 Half Step Mode / Forward Direction Sequence



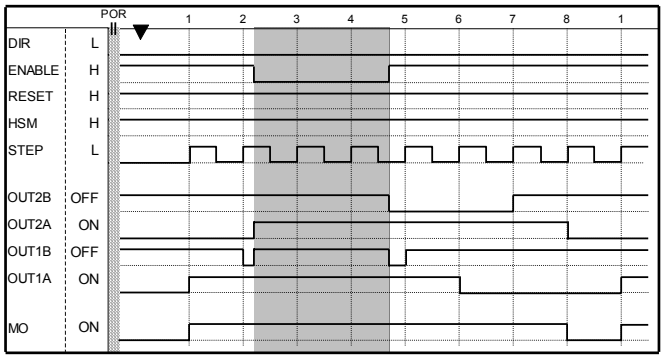
STEP	After POR	1	2	3	4	5	6	7	8
OUT2B	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	OFF
OUT2A	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	ON
OUT1B	OFF	OFF	OFF	OFF	ON	ON	ON	OFF	OFF
OUT1A	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	ON
MO	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON

Fig.4 Half Step Mode / Reverse Direction Sequence



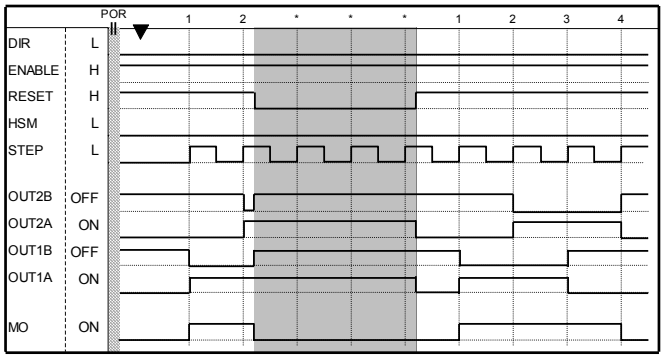
* When ENABLE is active OUT terminals are OFF, but internal logic circuit is ON.

Fig.5 Full Step Mode / Enable Sequence



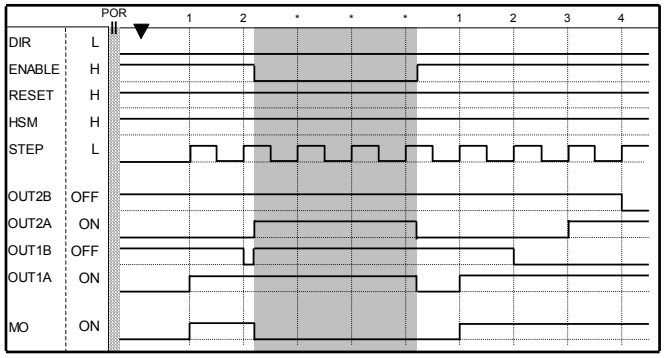
* When ENABLE is active OUT terminals are OFF, but internal logic circuit is ON.

Fig.6 Half Step Mode / Enable Sequence



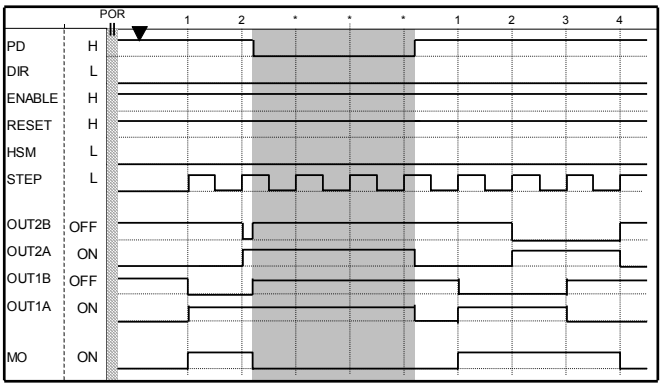
* When RESET is active OUT terminals are OFF, and internal logic circuit is to reset.

Fig.7 Full Step Mode / Reset Sequence



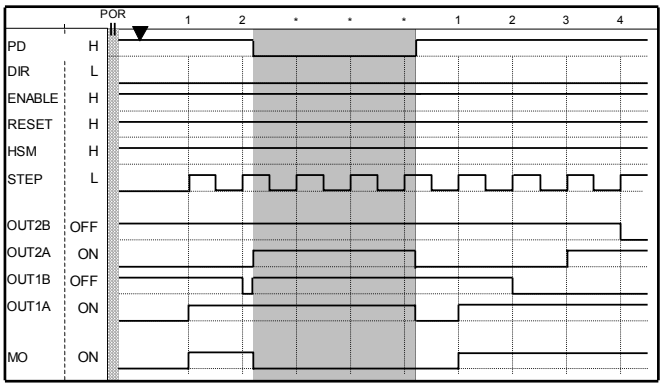
* When RESET is active OUT terminals are OFF, and internal logic circuit is to reset.

Fig.8 Half Step Mode / Rest Sequence



* When PD is active it forces all settings to initialize and be in stand-by mode, and MO is to be low.

Fig.9 Full Step Mode / PD Sequence



* When PD is active it forces all settings to initialize and be in stand-by mode, and MO is to be low.

Fig.10 Full Step Mode / PD Sequence

□ FUNCTION DESCRIPTION

The NJW4351 is designed for a high-performance constant-voltage unipolar stepper motor.

Using a general-purpose STEP&DIR motion controller, the device can easily control a stepper motor when combined with a pulse generator.

The maximum value of the phase output is 55 V that keeps the voltage margin of the motor from exceeding the limit, which is a common problem with unipolar winding systems. It simplifies the design of power control circuits during phase turn-off.

□ LOGIC INPUT BLOCK

All inputs are LS-TTL compatible. Input Block1 (STEP) has Schmitt Comparator to keep the thresh voltage unchanged even if logic supply voltage applied to it varies. It produces hesteresis voltage for noise immunity. Input Block2 (PD, DIR, HSM, RESET, ENABLE) has Schmitt Inverter for the main purpose of noise immunity.

Inputs are internally connected to GND by pull-down resistances, being open, the device recognizes to be low.

- STEP – Stepping Pulse

The Translator starts counting on every positive edge of the STEP. In full step mode, the pulse turns the stepper motor at the basic step angle. In half step mode, two pulses are required to turn the motor at the basic step angle.

The DIR (direction) signal and HSM (half/full mode) are latched to the STEP positive edge and must therefore be established before the start of the positive edge.

- DIR – Direction

The DIR signal determines the step direction. The direction of the stepper motor depends on how the NJW4351 is connected to the motor. DIR can be modified anytime, it miss-steps when it is simultaneous with the positive edge.

- HSM – Half/full Step Mode Switching

This signal determines whether the stepper motor runs at half step or full step mode. The Translator is set to half step mode when HSM is low. Like DIR, HSM can be modified anytime but not when its simultaneous with the positive edge.

- ENABLE – Phase Output Off

All phase outputs are turned off when ENABLE goes high reducing power consumption.

- RESET

A two-phase stepper motor repeats the same winding energizing sequence every angle that is a multiple of four of the basic step. The Translator is repeated every four pulses in full step mode and every eight pulses in half step mode.

When RESET is low, the Translator is initialized and the phase outputs turn-off.

When returning to high, the phase outputs are set to the initial energizing pattern output status.

- PD-Power Down

When PD goes low, it forces all settings to initialize and be in stand-by mode.

AND MO is to be low.

□ POR – Power On And Reset Function

The POR connected to VDD is to prevent miss-step under unstable condition of the inputting of logic supply voltage VDD.

After inputting VDD, the phase outputs are set to the initial energizing pattern output status.

□ PHASE OUTPUT BLOCK

The phase output block consists of four open-drain DMOS FET capable of sinking max 1.5A.

□ MO – Motor Origin Monitor

In initialized position of the Translator, MO output low to indicate to external devices that it is the initial energizing pattern output status.

□ PRECAUTIONS

1. Never disconnect the device or PC-board when power is supplied.
2. Remember that excessive voltages might be generated by motor, even though clamping diodes are used.
3. Choose a motor that is proportional to the current you need to establish desired torque. A high supply voltage will gain better stepping performance. If the motor is not specified for the VMM voltage, a current limiting resistor will be necessary to connect in series with center tap. This changes the L/R time constant.
4. Avoid VMM and VDD power supplies with serial diodes (without filter capacitor) and common ground with VDD.
5. To change actual motor rotation direction, exchange motor connections at OUT1A and OUT1B (OUT2A and OUT2B).
6. Half-stepping

   In the half-step mode, the power input to the motor alternates between one or two phase windings. In half-step mode, motor resonances are reduced. In a two-phase motor, the electrical phase shift between the windings is 90 degrees. The torque developed is the vector sum of two windings energized. Therefore, when only one winding is energized, which is the case in half-step mode for every second step, the torque of the motor is reduced by approximately 30%. This causes a torque ripple.
7. Drive Circuits

   High-performance stepper motor operation requires windings to be energized immediately at phase turn-on and quickly turned off when not in use.
8. Phase Turn-off Considerations

   When the winding current is turned off, induced high voltage spike will damage the drive circuits if not properly suppressed. Refer to the turn-off circuits described in Figures 11 to 14.

   The voltage potential at the phase output terminal may sometimes become negative (GND or below) due to the configuration of the turn-off circuit or the kickback voltage generated in it. In this condition there is a danger of a malfunction occurring in the logic circuit inside the device.

8.1. Precautions against high voltage using the Zener-diode turn-off circuit

Refer the Zener-diode turn-off circuit (see Fig.15). Zener-diode voltage value is Vz and the forward voltage of the diodes connected in series with the Zener-diode is Vd, the voltage VP of the phase output (OUT1A, OUT1B, OUT2A, OUT2B) terminal when the turn-off operation have occurred is expressed by the following equation. VP = VMM – (Vz + Vd)

The higher voltage, Vz, used, the shorter is the turn-off time of the winding current, thus producing high speed operation of the stepper motor. Note, however, that depending on the Zener voltage, VZ, the voltage potential at the phase output terminal may become negative, so design the turn-off circuit as indicated below.

8.1.1. When VP is a positive voltage: VMM > VZ + Vd

The circuit configuration is that of Fig.15.

Set the Zener voltage. For example, if VMM is 12 V, VZ + Vd is no higher than12V.

8.1.2 When VP is a negative voltage: VMM < VZ + Vd

The circuit configuration is that of Fig.16. In order to prevent a malfunction due to a negative voltage, be sure to insert diodes in series with the phase output terminals.

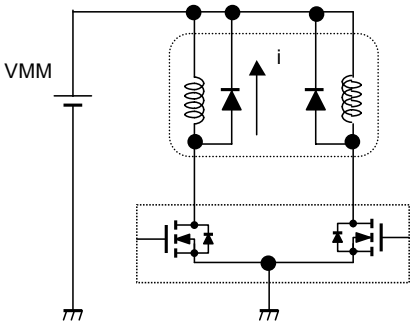


Fig.11 Diode and turn off circuit.

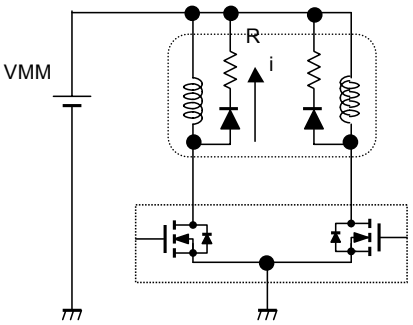


Fig12 Resistor and turn off circuit.

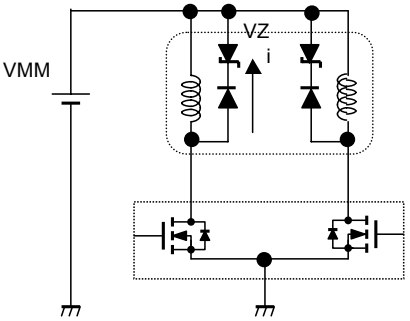


Fig.13 Zener diode and turn off circuit.

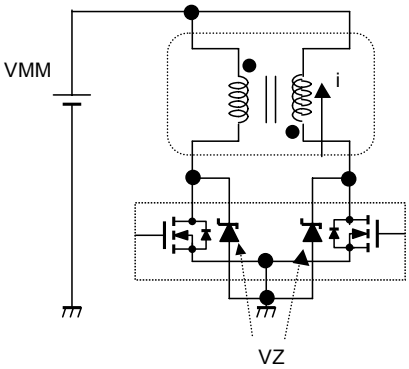


Fig.14 Power regeneration and turn off circuit.

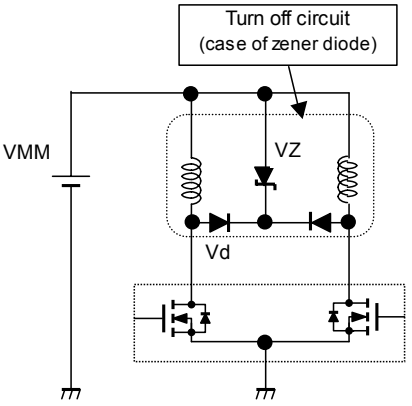


Fig.15 Zener diode and turn off circuit 2.

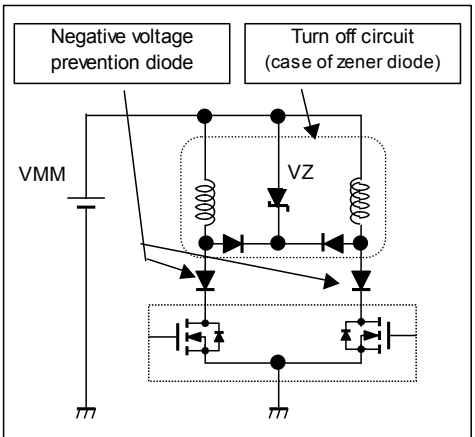
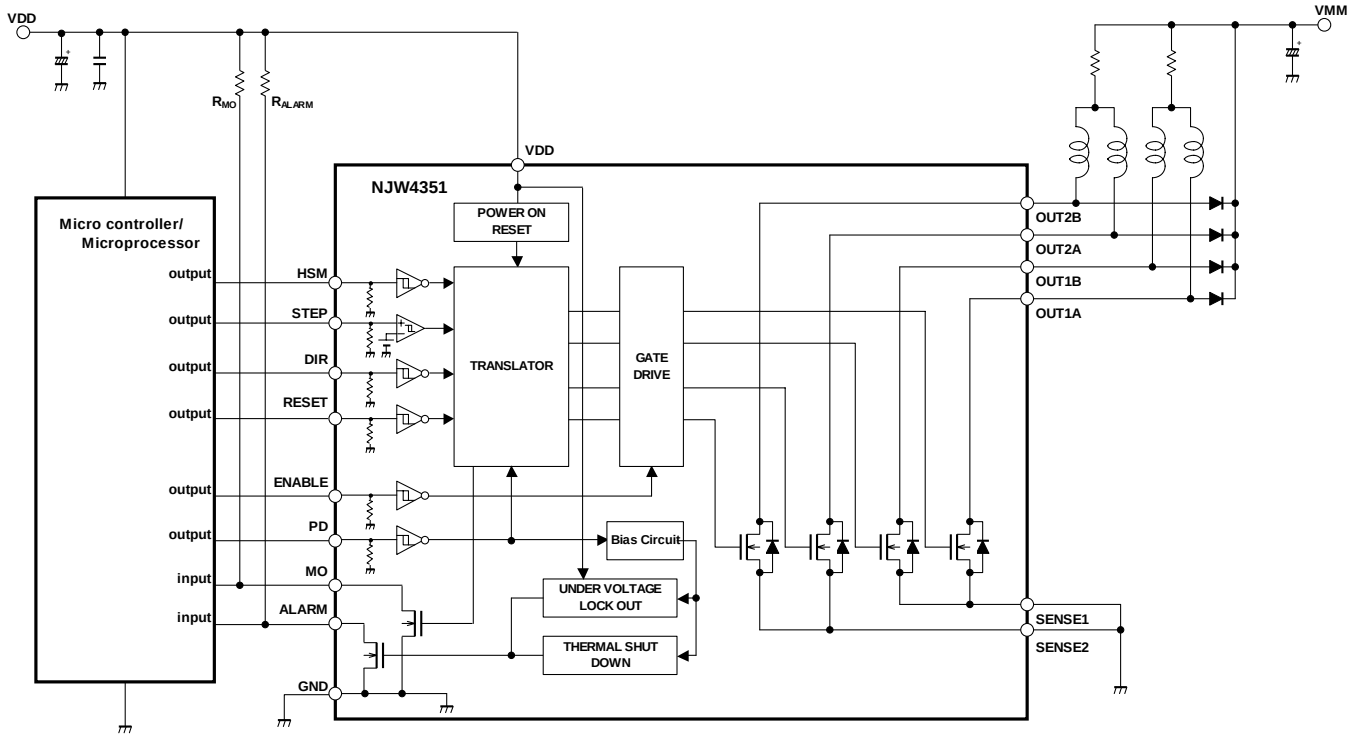


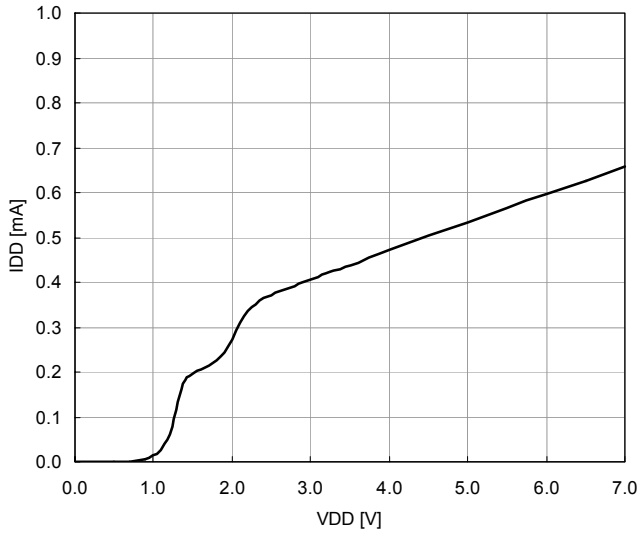
Fig.16 Turn off negative voltage prevention circuit
by zener diode

□ APPLICATION CIRCUIT

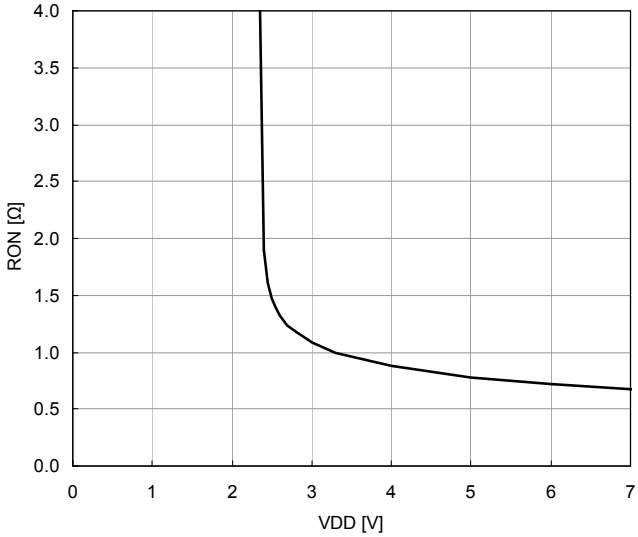


□ TYPICAL CHARACTERISTICS

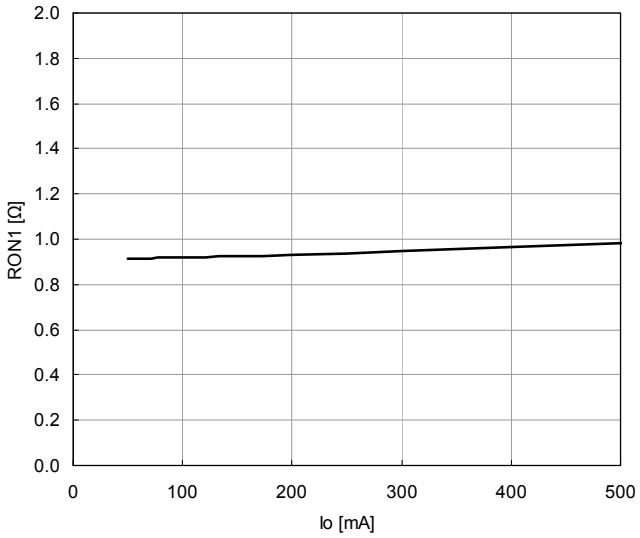
IDD - VDD
STEP=HSM=DIR=RESET=ENABLE=PD=VDD, Ta=25°C



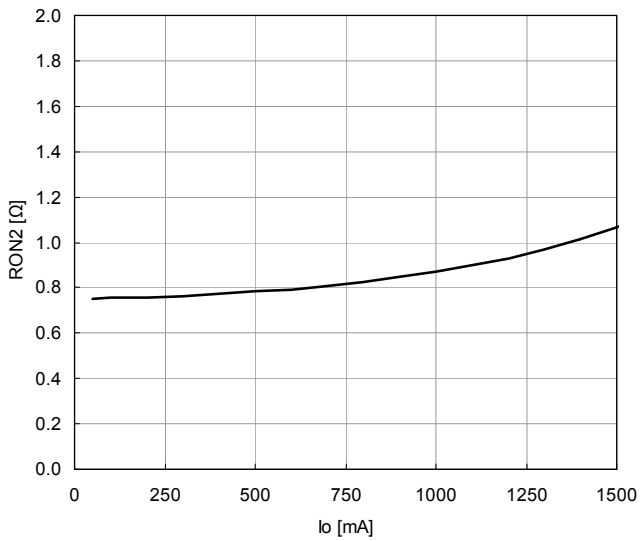
RON - VDD
Io=500mA, Ta=25°C



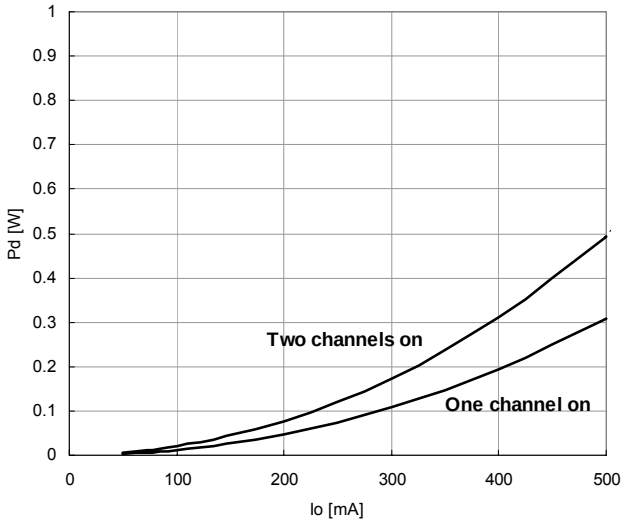
RON1 - Io
VDD=3.3V, Ta=25°C



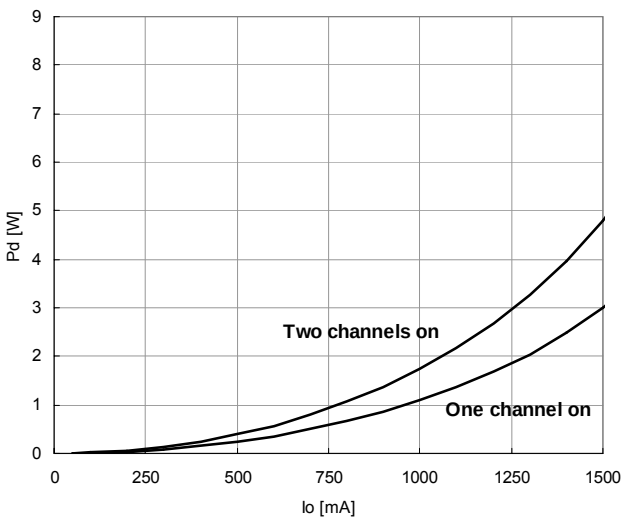
RON2 - Io
VDD=5.0V, Ta=25°C



Pd - Io
VDD=3.3V,Ta=25°C

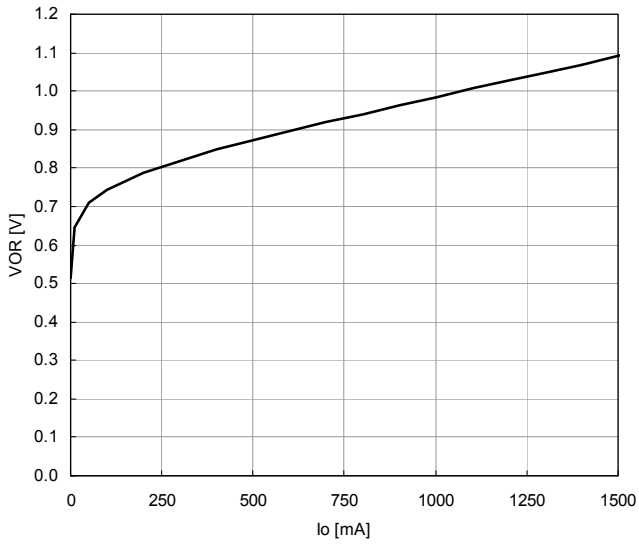


Pd - Io
VDD=5.0V,Ta=25°C

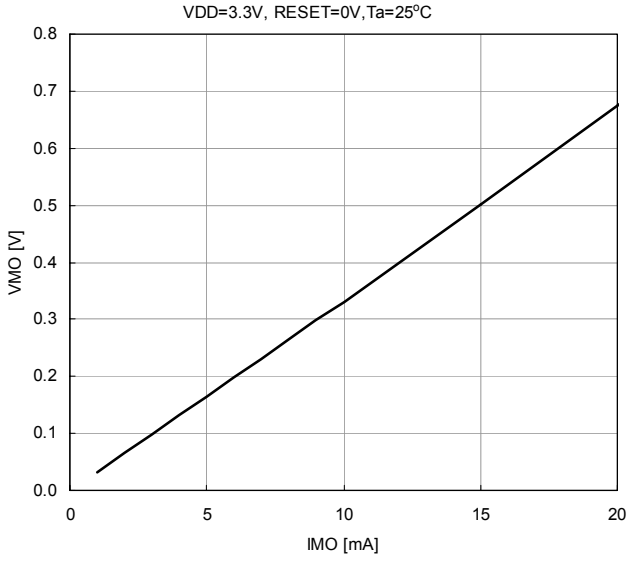


□ TYPICAL CHARACTERISTICS

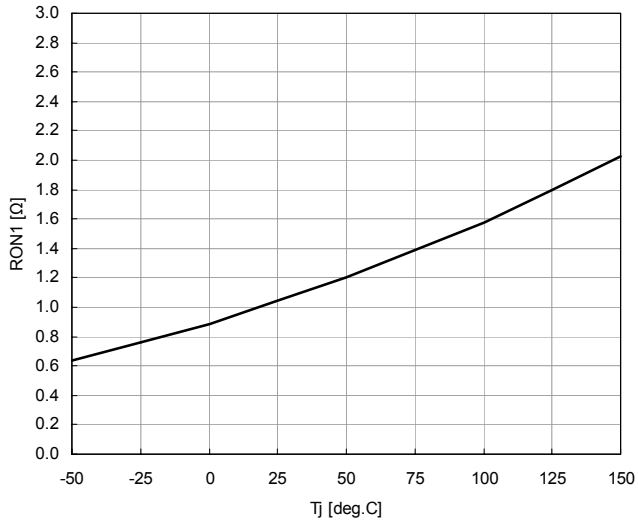
VOR - Io
VDD=3.3V, ENABLE=0V,Ta=25°C



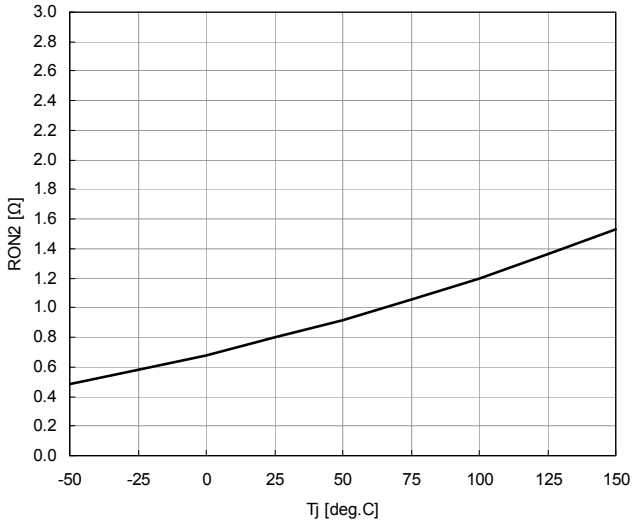
VMO - IMO
VDD=3.3V, RESET=0V,Ta=25°C



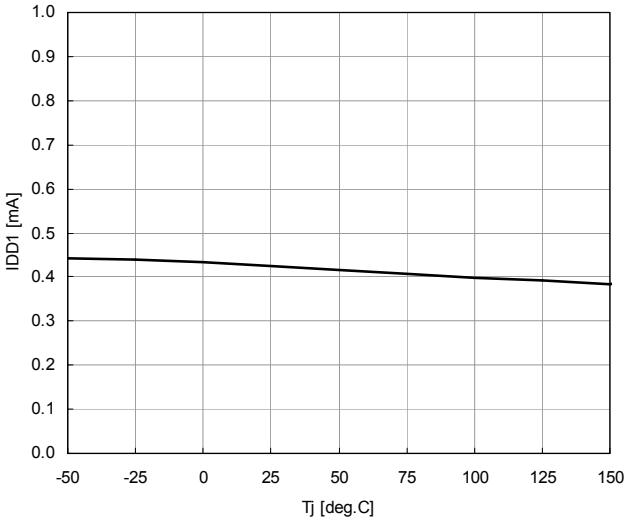
RON1 - Tj
VDD=3.3V, Io=500mA



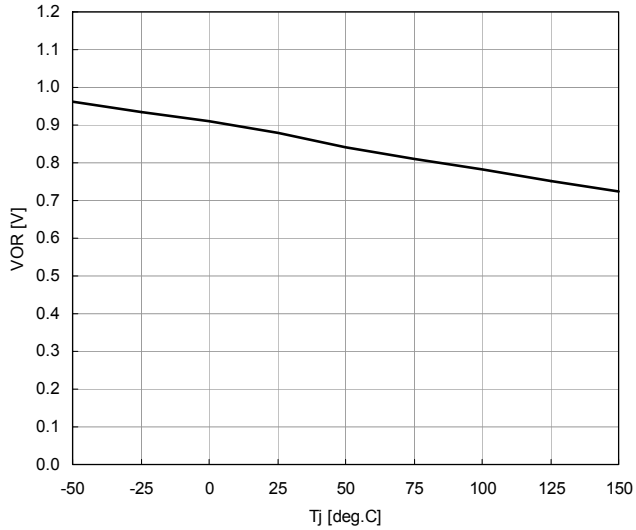
RON2 - Tj
VDD=5.0V, Io=500mA



IDD1 - Tj
VDD=3.3V



VOR - Tj
VDD=3.3V,Io=500mA



□ TYPICAL CHARACTERISTICS