HT-2000

PRODUCT Brief

HT-2000 HyperTransport™ SystemI/O™ Controller

FEATURES

- **The HT-2000 (BCM5780) integrates:**
  - Dual Broadcom® BCM5714 Gigabit Ethernet (GbE) controller
  - 17 PCI Express® (PCIe™) links with support for up to four controllers
  - Full PCI-X® 1.0 compliance with up to five bus masters
  - Two HyperTransport ports with integrated tunnel

- **HyperTransport features include:**
  - 2-GHz (1-GHz, 2X) HyperTransport bus interface
  - CRC generation and error checking
  - Programmable error checking and handling
  - Scalable clock speeds as well as support for reduced bit widths of 8 bits, 4 bits, and 2 bits
  - 16x HyperTransport transfer rates of 2000 Mbps, 1600 Mbps, 1200 Mbps, 1000 Mbps, 800 Mbps, and 400 Mbps, per wire
  - 8x HyperTransport transfer rates of 1600 Mbps, 1200 Mbps, 1000 Mbps, 800 Mbps, and 400 Mbps, per wire
  - Link disconnect protocol support
  - HyperTransport interrupt control and system management support
  - HyperTransport I/O link specification, Revision 1.05 compliant

- **Gigabit Ethernet features include:**
  - Dual integrated 10/100/1000/BASE-T transceivers
  - Dual 10/100/1000 tri-speed, full-duplex/half-duplex MACs
  - VLAN tag support (IEEE 802.1q)
  - Layer 2 priority encoding (IEEE 802.1p)
  - Link aggregation (IEEE 802.3ad)
  - Jumbo frame support
  - SMBus 2.0 interface
  - Broadcom BCM5714 driver compatible
  - Universal Management Port (UMP) for server management traffic
  - Programmable rules checker for advanced packet filtering and classification

- **PCI Express features include:**
  - Configurable I/O with 17 serial links and four masters operating at 2.5 GHz with differential, low-voltage signaling
  - Recoverable CRC errors with retransmission
  - 64-bit addressing support
  - Advanced error-detection, error-transmission on destination bus
  - Integrated bit-error generator and monitor function
  - PCIe V1.0 and 1.0a compliant

- **PCI-X features include:**
  - Concurrency between HyperTransport and PCI-X bus
  - Eight-deep outbound request queue (HyperTransport to PCI-X)
  - Eight-deep HyperTransport to PCI-X memory write posting
  - Eight-deep PCI-X to HyperTransport request queue (PCI-X to main memory transactions)
  - Parity protection on the PCI-X bus
  - Integrated PCI-X bus arbitration for up to five PCI-X bus masters
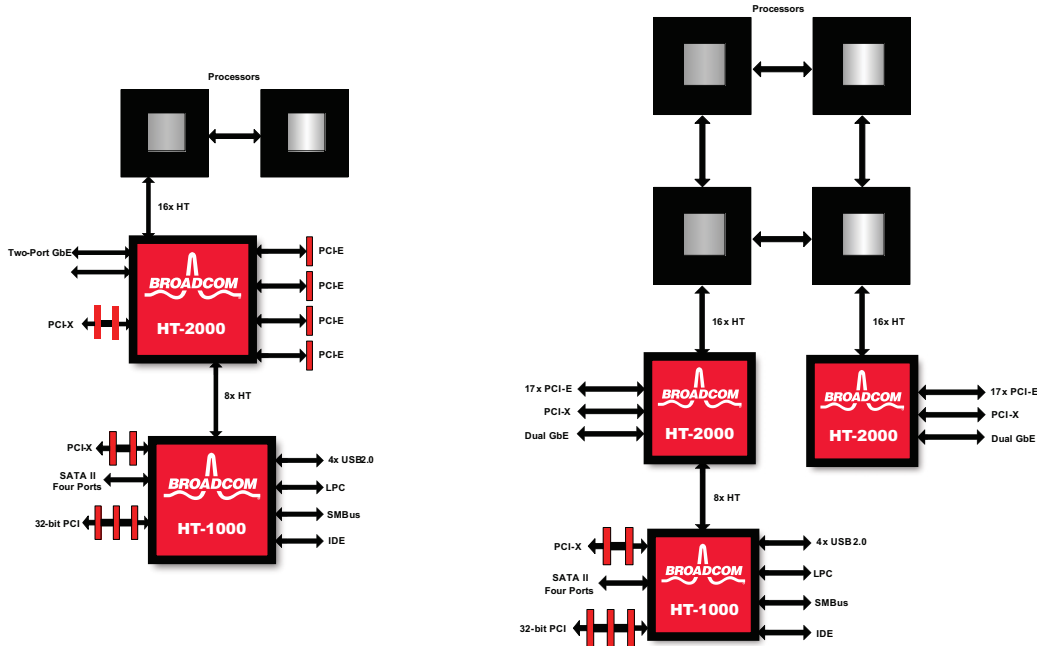 - Up to 133 MHz support

SUMMARY OF BENEFITS

- **Multiprocessing SystemI/O controller for the HyperTransport-enabled processors offering integration, performance, reliability, availability, scalability, and modularity**

- **Integrates all main server I/O interconnects: PCIe, PCI-X, and GbE**

- **Best-in-class 64-bit performance**
  - HyperTransport-based architecture reduces I/O bottlenecks and improves overall system performance
  - Best-in-class 64-bit and 32-bit performance

- **Industry proven reliability and availability**
  - Reusable design methodology used with field-proven functional blocks
  - Designed for 24/7 enterprise computing uptime
  - Advanced error detection and correction
  - Comprehensive driver suite from BCM57XX product family

- **Extensive scalability**
  - HyperTransport multiprocessor architecture allows superior per processor scalability compared to similar x86 architectures
  - Individual HyperTransport link widths and clock speeds easily suit cost/performance targets
  - Multiple HT-2000 SystemI/O controllers deliver plenty of bandwidth and I/O slots

- **Modular architecture**
  - Modular building blocks allow platform designs that scale from the low-end all the way to high-end
  - SystemI/O modularity keeps costs low without sacrificing functionality
  - Modular design allows more freedom to differentiate from competition

- **The HT-2000 utilizes the HyperTransport interconnect to the CPU/host bridge to a variety of South Bridge and I/O bridge solutions. This building block approach enables OEMs to tailor systems to their applications.**

TARGET APPLICATIONS

- Uni, dual, and quad processor servers
- Workstations
- Server clusters
- Storage systems (NAS)

ORDERING INFORMATION

- SWC-HT2000-S07: PBGA 867LD Leaded
- SWC-HT2000-S07LF: PBGA 867LD Lead-Free

Processors

16x HT

Two-Port GbE | PCI-E
PCI-E
BROADCOM
HT-2000
PCI-X | PCI-E
PCI-E

8x HT

PCI-X | 4x USB2.0
SATA II Four Ports | BROADCOM | LPC
HT-1000 | SMBus
32-bit PCI | IDE

Processors

16x HT | 16x HT

17 x PCI-E | BROADCOM | BROADCOM | 17 x PCI-E
PCI-X | HT-2000 | HT-2000 | PCI-X
Dual GbE | Dual GbE

8x HT

PCI-X | 4x USB2.0
SATA II Four Ports | BROADCOM | LPC
HT-1000 | SMBus
32-bit PCI | IDE

Multiprocessing SystemI/O Configurations

The HT-2000 is targeted at the volume server market with the capability to efficiently span from one-to-eight CPUs without incurring large latencies.

The HT-2000 is a highly-scalable SystemI/O solution for 64-bit/32-bit processors that can be configured to meet OEM needs for a variety of product segments. The dual processor configuration shown above can be used for mainstream tower and rack servers. Additional HT-2000 devices can be added to a system to scale to larger multi CPU servers.

The HT-2000 is a high-performance HyperTransport to the PCI/PCI-X bridge and PCIe bridge, capable of tunneling the data between the two HyperTransport ports. The HyperTransport tunneling enables an efficient four-way system as shown above (on the right), where a base configuration can be created with fewer devices.

The HT-2000 takes I/O bandwidth, configurability, and scalability to unprecedented levels. The 16x HyperTransport port can operate at a frequency of 1-GHz double-data rate in both the transmit and receive directions to aggregate up to a total bandwidth of 8 GBps. This bandwidth is available to communicate with devices such as the processor or a host bridge.

The 8x HyperTransport port can operate at a frequency of 800-MHz double data rate in both the transmit and receive directions to aggregate up to a total bandwidth of 3.2 GBps. This bandwidth is available to communicate with HyperTransport I/O hubs such as the HT-1000.

The HT-2000 offers the best I/O configurability available. The PCI-X bus supports up to five bus masters and deep transaction queues, and enables designers to implement the right balance between performance and slot count as required by their systems. The PCI-X bus is capable of supporting all modes up to 133 MHz.

For the next-generation low-latency, high-bandwidth I/O interconnect PCIe, the HT-2000 offers an array of choices to match the bandwidth needs of the device as well as the number of devices that need to be supported on the platform. The 17 serial links operating at 2.5 GHz can be configurable to four PCIe masters. Some sample configurations that are possible are x8 + x8 + x1, x8 + x4 + x4 + x1, or x4 + x4 + x4 +x4, or x8 + x4 + x1. Combinations of link widths that are lower than the ones mentioned are possible. No other device in the marketplace matches this level of flexibility for PCIe.

The HT-2000 takes integration a level further by offering two server class GbE NIC ports. The high-performance MAC + PHY **+** SerDes combination within the device provides the two Ethernet ports that every server needs in the most cost-effective way. No feature compromises have been made with respect to the embedded Ethernet controllers, and they offer such server class features as link aggregation, VLAN tag support, jumbo frame support, packet filtering, and classification. The UMP interfaces to a Baseboard Management Controller (BMC) and allows the BMC to send and receive system management information through the GbE port. This dedicated management interface allows for a much higher bandwidth as compared to the traditional SMBus, making video redirection possible, and eliminates the need for an Ethernet port on the BMC, which saves cost.

Multiple HT-2000 devices can be used to scale out the system in terms of processors and I/O connectivity for building higher-end multiprocessor systems.

The high levels of integration, enterprise server features, I/O flexibility, and device scalability make the HT-2000 the best-in-class SystemI/O solution in the market for building the servers.

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