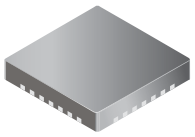
WLED/RGB Backlight Driver for Medium Size LCDs

Features and Benefits

- Active current sharing between 6 LED strings for ±1.3% typical current matching
- ±1.2% typical current accuracy
- Drive up to 11 series × 8 parallel = 88 LEDs (V_f = 3.5 V, I_f = 40 mA)
- External PWM control for LED dimming
- An external resistor for LED current setting
- Boost converter with integrated 50 V, 2 A DMOS
- LED sinks rated for 45 mA
- 200 kHz to 2 MHz switching frequency
- Open LED disconnect
- Boost current limit, thermal shutdown, and soft start
- No audible ceramic capacitor noise during PWM dimming
- Adjustable overvoltage protection (OVP)
- No pull-up resistors required for LED modules that use ESD capacitors

Package: 26 pin QFN/MLP (suffix EC)

Approximate Scale 1:1



Description

The A8504 is a multi-output WLED driver for medium display backlighting. The A8504 integrates a boost converter and eight current-sinks to provide a WLED/RGB backlight driver. The boost converter can provide output voltage up to 47 V. The flexible channel selection control and high voltage capability allow a wide range of LED backlight applications. The boost converter is a constant frequency current-mode converter. Each LED channel can sink 45 mA, and channels can be paralleled for higher currents. LED current can be controlled with external PWM duty cycle.

The A8504 is available in a 26 pin, 4 mm × 4 mm QFN/MLP package that is only 0.75 mm nominal in height. Applications include:

- Thin notebook displays
- LCD TV
- RGB backlight
- GPS systems
- Portable DVD players

Typical Application

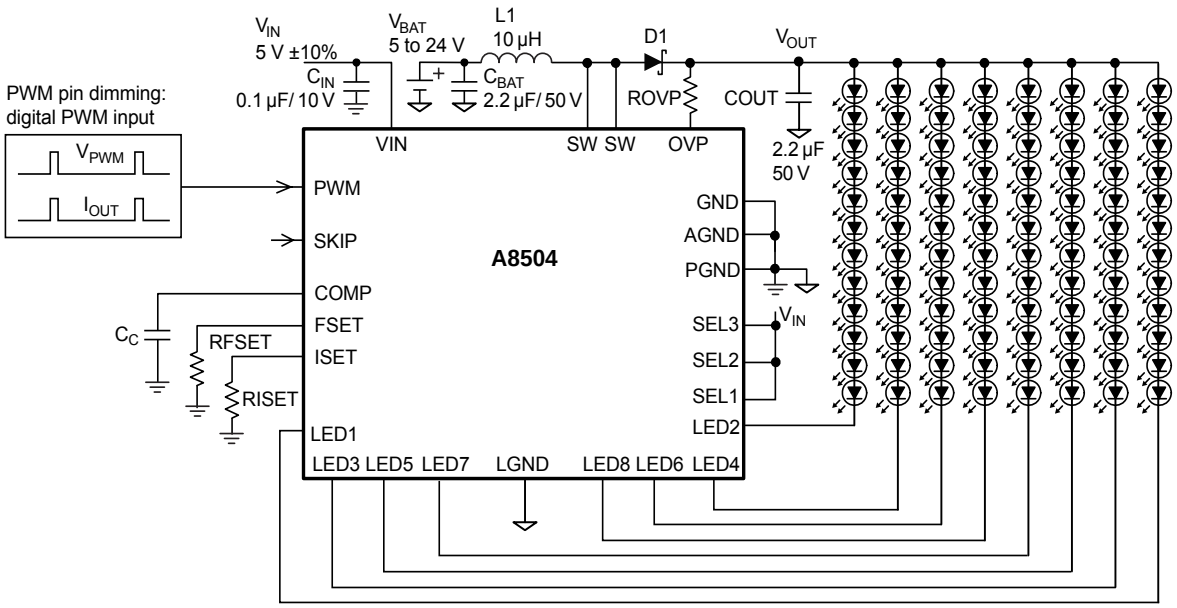


Figure 1. LCD monitor backlight, driving 11 green, blue, or white LEDs with V_f= 3.5 V, or 18 red LEDs with V_f = 2.2 V, per LED string. Overvoltage protection set to 45 V nominal (40.5 V minimum). See also: Recommended Components table, page 16.

Selection Guide

Part Number	Package	Packing*
A8504EECTR-T	4 mm × 4 mm QFN/MLP	1500 pieces / 7-in. reel

*Contact Allegro for additional packing options

Device package is lead (Pb) free, with 100% matte tin leadframe plating.

Absolute Maximum Ratings

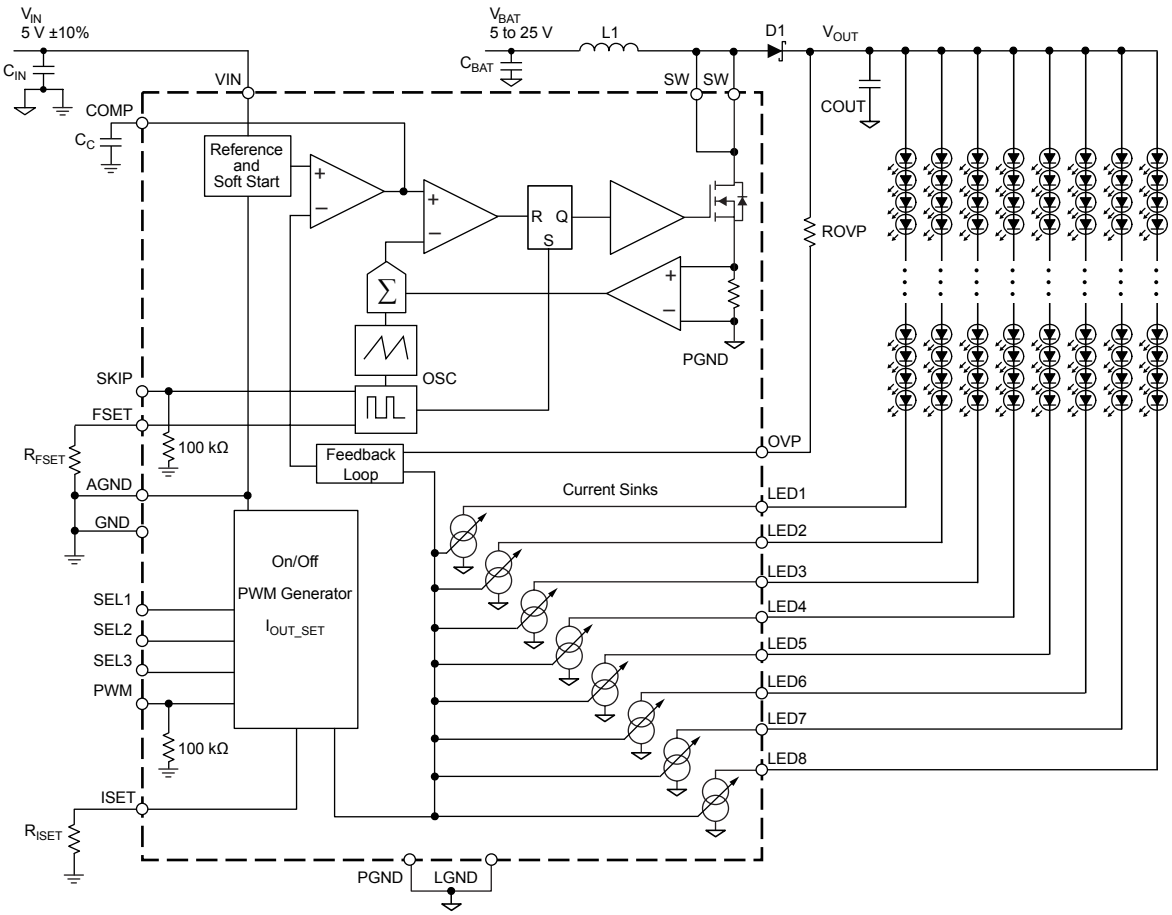
Characteristic	Symbol	Notes	Rating	Units
SW and OVP Pins			–0.3 to 50	V
LED1 through LED8 Pins			–0.3 to 23	V
VIN Pin	V_{IN}		–0.3 to 6	V
Remaining Pins			–0.3 to V_{IN} + 0.3	V
Operating Ambient Temperature	T_A	Range E	–40 to 85	ºC
Maximum Junction Temperature	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

Package Thermal Characteristics*

Characteristic	Symbol	Note	Rating	Units
Package Thermal Resistance	$R_{\theta JA}$	Measured on 3 in. × 3 in., 2-layer PCB	48.5	°C/W

*Additional information is available on the Allegro website

Functional Block Diagram



ELECTRICAL CHARACTERISTICS, valid at T_A = –40°C to 85°C, typical values at T_A = 25°C, V_{IN} = 5 V, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Input Voltage Range	V_{IN}		4.2	–	5.5	V
Undervoltage Lockout Threshold	V_{UVLO}	V_{IN} falling	–	–	4	V
UVLO Hysteresis Window	$V_{UVLOhys}$		–	0.2	–	V
Supply Current	I_{SUP}	Switching at no load, T_A = 25°C	–	5	–	mA
		Shutdown PWM = V_{IL}	–	0.1	1	µA
Error Amplifier						
Error Amplifier Open Loop Gain	A_{VEA}		–	60	–	dB
Error Amplifier Unity Gain Bandwidth	UGB_{EA}		–	3	–	MHz
Error Amplifier Transconductance	Gm_{EA}	ΔI_{COMP} = ±10 µA	–	850	–	µA/V
Error Amplifier Output Sink Current	I_{EAsink}	V_{LED1-8} = 1 V	–	280	–	µA
Error Amplifier Output Source Current	$I_{EAsource}$	V_{LED1-8} = 0 V	–	–280	–	µA
Boost Controller						
Switching Frequency	f_{SW}	R_{FSET} = 13 kΩ, SKIP = V_{IL}	1.8	2	2.2	MHz
		R_{FSET} = 26.1 kΩ, SKIP = V_{IL}	–	1	–	MHz
		R_{FSET} = 32.4 kΩ, SKIP = V_{IH}	–	200	–	kHz
Minimum Switch Off-Time	t_{OFFmin}		–	70	–	ns
Logic Input Levels (PWM, SEL*x*, and SKIP pins unless otherwise specified)						
Input Voltage Level Low	V_{IL}		–	–	0.4	V
Input Voltage Level High	V_{IH}		1.5	–	–	V
Input Leakage Current (PWM, and SKIP pins)	I_{Ileak}	$V_{I(pin)}$ = 5 V, T_A = 25°C	–	–	100	µA
Input Leakage Current (SEL*x* pins)	$I_{SELleak}$		–	–	1	µA
Over Voltage Protection (OVP)						
Output Overvoltage Rising Limit	V_{OVP}		28	–	32	V
OVP Sense Current	I_{OVPH}		–	49	–	µA
OVP Release Current	I_{OVPL}		–	44	–	µA
OVP Leakage Current	$I_{OVPleak}$	V_{VOP} = 21 V	–	0.1	–	µA
Boost Switch						
Switch On Resistance	$R_{ds(on)}$	I_{SW} = 1.5 A	–	225	–	mΩ
Switch Leakage Current	I_{SWleak}	V_{SW} = 5 V, T_A = 25°C	–	–	1	µA
		V_{SW} = 21 V	–	1	–	µA
Switch Current Limit	I_{SWlim}		1.6	2	–	A

Continued on the next page…

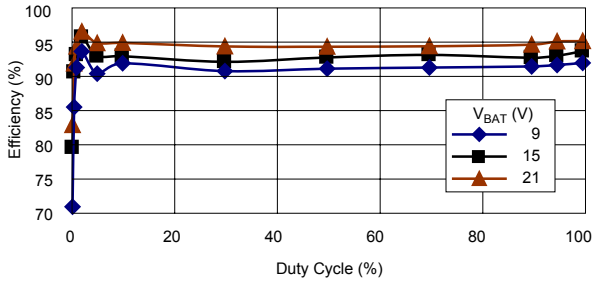
ELECTRICAL CHARACTERISTICS (continued), valid at T_A = –40°C to 85°C, typical values at T_A = 25°C, V_{IN} = 5 V, unless otherwise noted

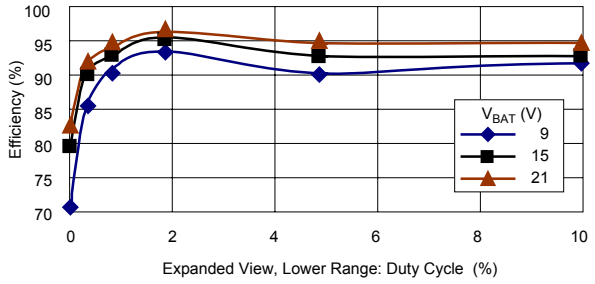
Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
LED Current Sinks						
LED*x* Regulation Voltage	V_{LEDx}		–	800	–	mV
I_{SET} to I_{LEDx} Current Gain	A_{ISET}	I_{SET} = 83 µA	–	460	–	–
Voltage on ISET Pin	V_{ISET}		–	1.23	–	V
I_{SET} Allowable Current Range	I_{SET}		40	–	100	µA
LED*x* Accuracy	Err_{LEDx}	R_{ISET} = 14.7 kΩ; 100% current ratio, measured as average of LED1 to LED8; LED1 to LED8 = 0.8 V	–	±1.2	–	%
LED*x* Matching	Δ_{LEDx1}	LED1 to LED6; I_{SET} = 83 µA , 100% current ratio; LED1 to LED6 = 0.8 V; SEL1=SEL3=V_{IH}; SEL2=V_{IL}	–	±1.3	–	%
	Δ_{LEDx2}	LED1 to LED8; I_{SET} = 83 µA , 100% current ratio; LED1 to LED8 = 0.8 V; SEL1=SEL2=SEL3=V_{IH}	–	–1.7 to 2.5	–	%
LED*x* Switch Leakage Current	$I_{LSleak5}$	V_{LEDx}= 5 V, PWM = 0, T_A = 25°C	–	–	1	µA
LEDx Switch Leakage Current	$I_{LSleak21}$	V_{LEDx}= 21 V, PWM =0	–	1	–	µA
Soft Start						
Soft Start Boost Current Limit	I_{SWSS}	Initial soft start current for boost switch	-	1.2	-	A
Soft Start LED*x* Current Limit	I_{LEDSS}	Current through enabled LED*x* pins during soft start, R_{ISET}= 14.7 kΩ	-	3	-	mA
Thermal Shutdown Threshold	T_{SHDN}	40°C hysteresis	–	165	–	°C

Performance Characteristics

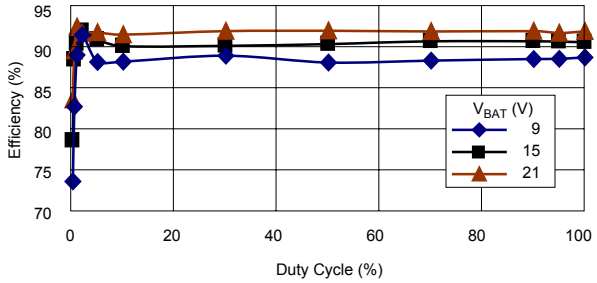
Efficiency with PWM dimming: PLED/PBAT, V_{IN} = 5 V

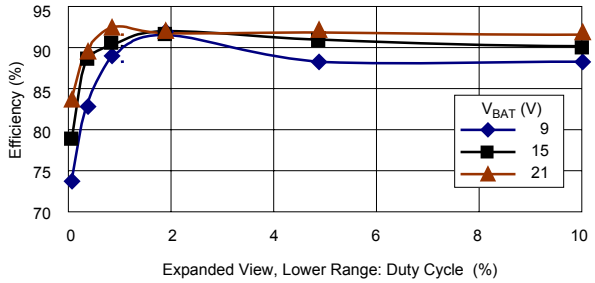
V_{IN} = 5 V, 6 ch. with 7 LEDs per ch., 40 mA per ch., f_{SW} = 1 MHz



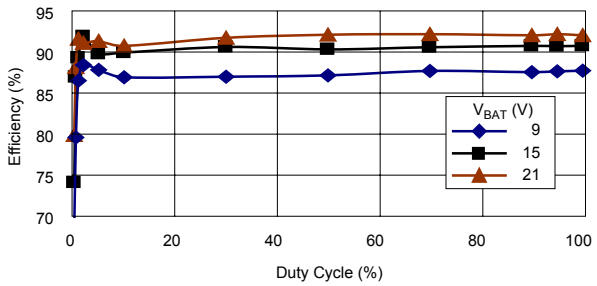


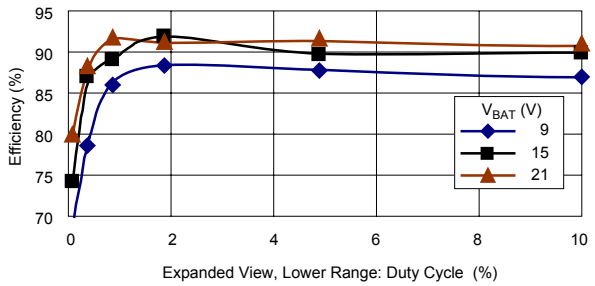
V_{IN} = 5 V, 6 ch. with 7 LEDs per ch., 40 mA per ch., f_{SW} = 2 MHz



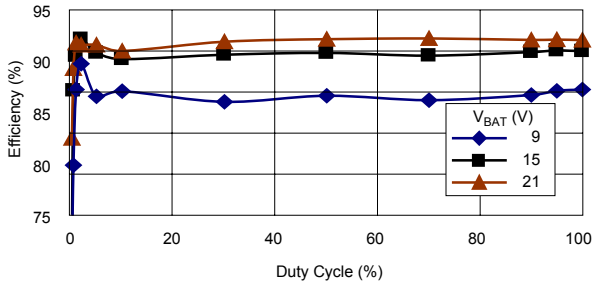


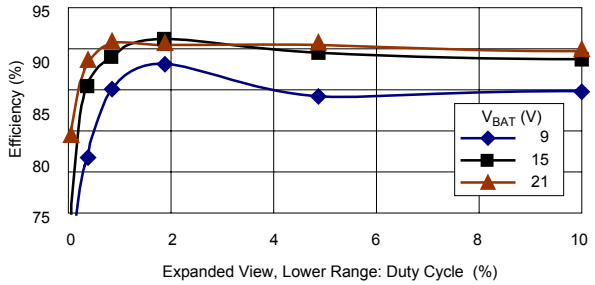
V_{IN} = 5 V, 8 ch. with 8 LEDs per ch., 40 mA per ch., f_{SW} = 1 MHz





V_{IN} = 5 V, 8 ch. with 8 LEDs per ch., 40 mA per ch., f_{SW} = 2 MHz



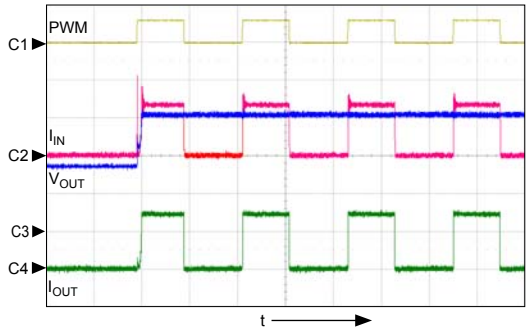


Performance Characteristics

Turn-On with PWM Signal

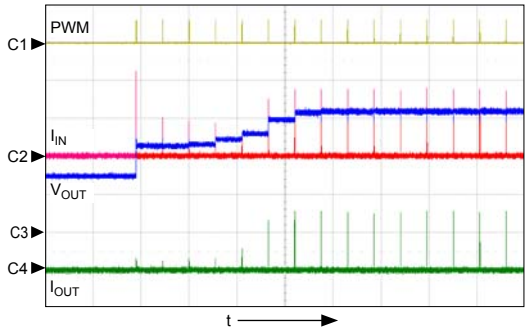
V_{IN} = 5 V, V_{BAT} = 15 V; f_{PWM} = 100 Hz; f_{SW} = 1 MHz
8S8P configuration, 40 mA per channel

50% Duty Cycle



Symbol	Parameter	Units/Division
C1	V_{PWM}	5 V
C2	I_{IN}	500 mA
C3	V_{OUT}	10 V
C4	I_{OUT}	200 mA
t	time	5 ms

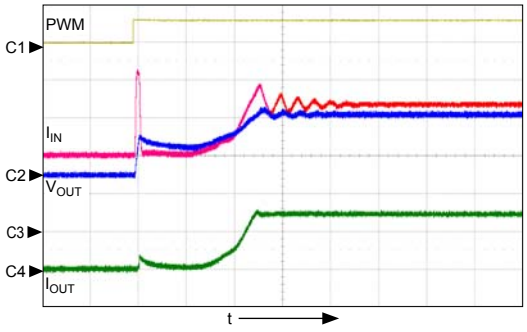
1% Duty Cycle



Symbol	Parameter	Units/Division
C1	V_{PWM}	5 V
C2	I_{IN}	500 mA
C3	V_{OUT}	10 V
C4	I_{OUT}	200 mA
t	time	20 ms

Soft Start Operation

V_{IN} = 5 V, V_{BAT} = 15 V; f_{SW} = 1 MHz
8S8P configuration, 40 mA per channel



Symbol	Parameter	Units/Division
C1	V_{PWM}	5 V
C2	I_{IN}	500 mA
C3	V_{OUT}	10 V
C4	I_{OUT}	200 mA
t	time	200 µs

Functional Description

The A8504 is a multioutput WLED driver for medium display backlighting. The A8504 works with 4.2 to 5.5 V input supply, and it has an integrated boost converter to boost battery voltage up to 47 V, 40 mA per LED string. An inductor can be connected to a separate power supply, V_{BAT}, from 5 to 25 V, with the A8504 IC powered from a 5 V source. The LED sinks can sink up to a 45 mA current.

The boost converter is a constant frequency current-mode converter. The integrated boost DMOS switch is rated for 50 V at 2 A. This switch has pulse-by-pulse current limiting, with the current limit independent of duty cycle. The switch also has output overvoltage protection (OVP), with the OVP level adjustable, typically from 30 to 47 V, as described in the Device Internal Protection section.

The A8504 has individual open LED detection. If any LED opens, the corresponding LED pin is removed from regulation logic. This allows the remaining LED strings to function normally, without excessive power dissipation.

The switching frequency, f_{SW}, can be set from 600 kHz to 2 MHz by a single resistor, RFSET, connected across the FSET and AGND pins, and with the SKIP pin set to logic low (see figure 2).

The switching frequency is set as:

$$F_{SW} = 26.03 / R_{FSET},$$

where F_{SW} is in MHz and R_{FSET} is in kΩ When the SKIP pin is connected to logic low, switching frequency is as set by RFSET.

When the SKIP pin is connected to logic high, the switching frequency is divided by 4. The SKIP pin can be used to reduce switching frequency in order to reduce switching losses and improve efficiency at light loads.

The IC offers a wide-bandwidth transconductance amplifier with external COMP pin. External compensation offers optimum performance for the desired application.

The A8504 has eight well-matched current sinks to provide regulated current through LEDs for uniform display brightness. The quantity of LED*x* pins used is determined by the SEL*x* pins. Refer to table 1 for further description.

The boost converter is controlled such that the minimum voltage on any LED*x* pin is 800 mV. In a typical application, the LED*x* pin connected to the LED string with the maximum voltage drop controls the boost loop, so the remaining pins will also have the higher voltage drop. All LED sinks are rated for 21 V, to allow PWM dimming control.

LED Current Setting

The maximum LED current can be set at up to 45 mA per channel, by using the ISET pin. To set the reference current, I_{SET}, connect a resistor, RISET, between this pin and ground, valued according to the following formula:

$$I_{SET} = 1.23 / R_{ISET},$$

where I_{SET} is in mA and R_{ISET} is in kΩ.

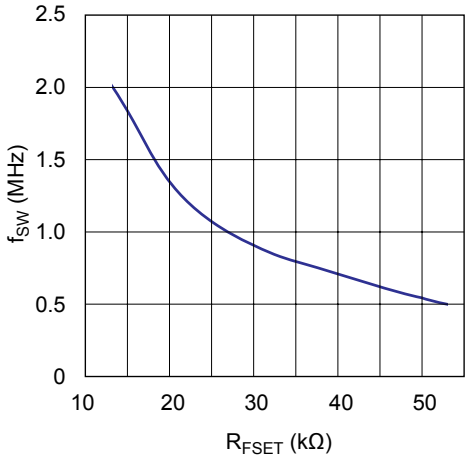


Figure 2. Switching frequency setting by value of RFSET.

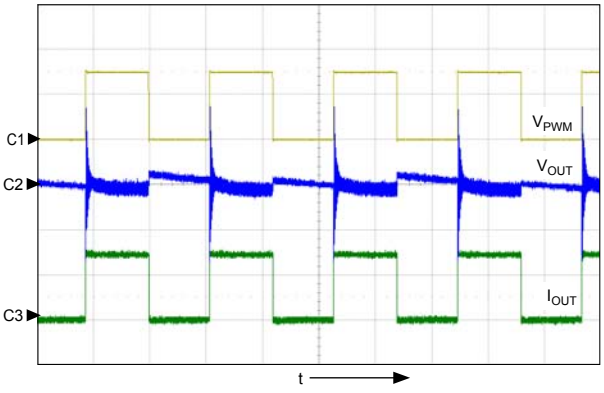
Table 1. LEDx Channel Enable Table

SEL1	SEL2	SEL3	LED*x* Outputs
0	0	0	Only LED1 on
1	0	0	LED1 through LED2 on
0	1	0	LED1 through LED3 on
1	1	0	LED1 through LED4 on
0	0	1	LED1 through LED5 on
1	0	1	LED1 through LED6 on
0	1	1	LED1 through LED7 on
1	1	1	LED1 through LED8 on

This current is multiplied internally with a gain of 480, and then mirrored on all enabled LED*x* pins. This sets the maximum current through the LEDs, referred to as "100% current." The LED current can be reduced from 100% by on/off control (PWM) with an external PWM signal on the PWM pin

On/off Control (PWM) with an External PWM Signal on the PWM Pin. When the PWM pin is pulled high, the A8504 turns on and all enabled LED*x* pins sink 100% current. When the PWM pin is pulled low, the IC shuts down with the LED*x* pins disabled. External PWM applied to the PWM pin should be in the range of 100 to 400 Hz for optimal accuracy.

At startup, the output capacitor is discharged and the IC enters soft start. The boost current is limited to 1 A, and all active LED*x* pins sink $^1/_{16}$ of the set 100% current until all of the enabled LED*x* pins reach 0.8 V. After the IC comes out of soft start, the boost current and the LED*x* pin currents are set to 100% current. The output capacitor charges to the voltage level required to supply full LED*x* current within a few cycles. The startup sequence is shown in the Soft Start chart in the Performance Characteristics section. The IC is shut down immediately when PWM goes low.



Symbol	Parameter	Units/Division
C1	V_{PWM}	2.00 V
C2	$V_{OUT(ac)}$	500 mV
C3	I_{OUT}	200 mA
t	time	5 ms

Figure 3. Output Voltage Ripple During PWM Dimming. V_{IN}= 5 V, V_{BAT}= 15 V, f_{SW}= 1 MHz, f_{PWM}= 100 Hz, PWM duty cycle = 50%, 8S8P configuration, 40 mA per channel.

Device Internal Protection

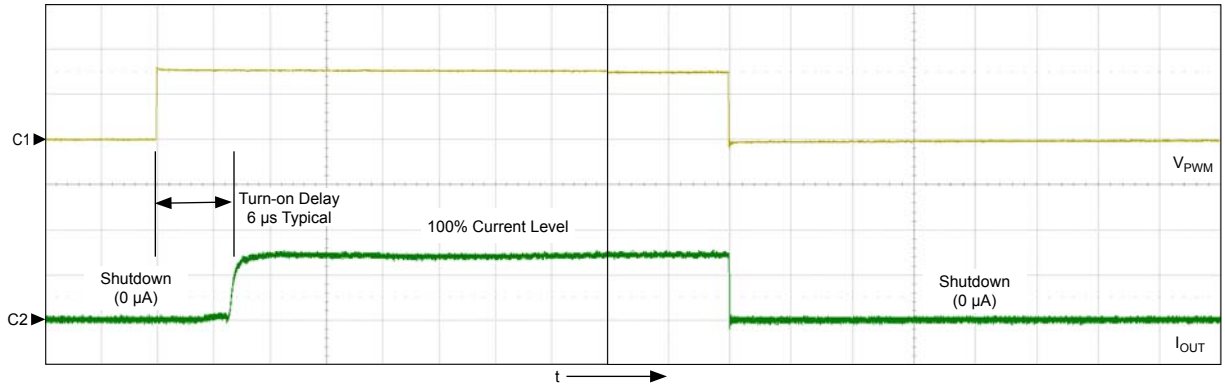
Overcurrent Protection (OCP). The A8504 has a pulse-by-pulse current limit of 2 A on the boost switch. This current limit is independent of duty cycle.

Thermal Shutdown Protection (TSD). The IC shuts down when junction temperature exceeds 165°C and restarts when the junction temperature falls by 40°C.

Overvoltage Protection (OVP). The A8504 has overvoltage protection to protect the IC against output overvoltage. The overvoltage level can be set, from 30 to 45 V typical, with an external resistor, ROVP, as shown in figure 5. When the current though the OVP pin exceeds 49 µA, the OVP comparator goes high. When the OVP pin current falls below 44 µA, OVP is reset. Calculate the value for R_{OVP} as follows:

$$R_{OVP} = (V_{OVP} - 30) / 49\ \mu A\ ,$$

where V_{OVP} is the desired typical OVP level in V, and R_{OVP} is in Ω. For tighter OVP limits, a low–leakage-current Zener diode, DZ, can be used, instead of ROVP, to set OVP at up to 47 V. For redundancy, DZ can be connected across ROVP to provide additional protection, if ROVP should open. Select a 17 V low-leakage Zener diode for DZ.



Symbol	Parameter	Units/Division
C1	V_{PWM}	2.00 V
C2	I_{OUT}	200 mA
t	time	5 µs

Figure 4. Timing of turn-on delay and turn-off delay when using the PWM pin. V_{IN}= 5 V, V_{BAT}= 15 V, f_{SW}= 1 MHz, f_{PWM}= 100 Hz, 8S8P configuration, 40 mA per channel.

Open LED Protection. The A8504 has protection against open LEDs. If any enabled LED string opens, voltage on the corresponding LED*x* pin goes to zero. The boost loop operates in open loop till the OVP level is reached. The A8504 identifies the open LED string when overvoltage on the OVP pin is detected. This string is then removed from the boost controlling loop. The boost circuit is then controlled in the normal manner, and the output voltage is regulated, to provide the output required to drive the remaining strings. If the open LED string is reconnected, it will sink current up to the programmed current level.

Note: Open strings are removed from boost regulation, but not disabled. This keeps the string in operation if LEDs open for only a short length of time, or reach OVP level on a transient event. The disconnected string can be restored to normal mode by re-enabling the IC. It can also be restored to normal operation if the fault signal is removed from the corresponding LED*x* pin, but an OVP event occurs on any other LED*x* pin.

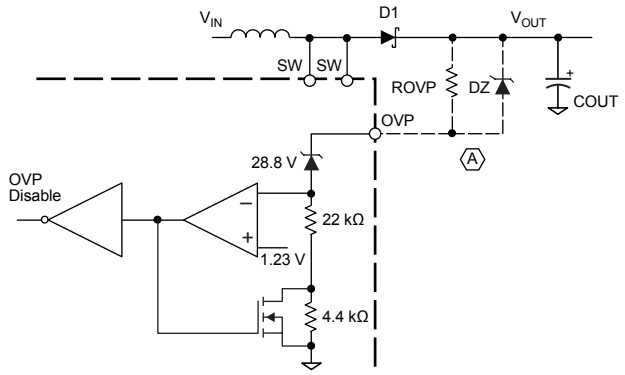
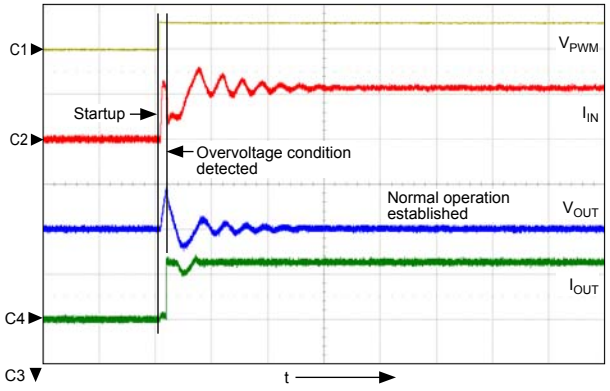
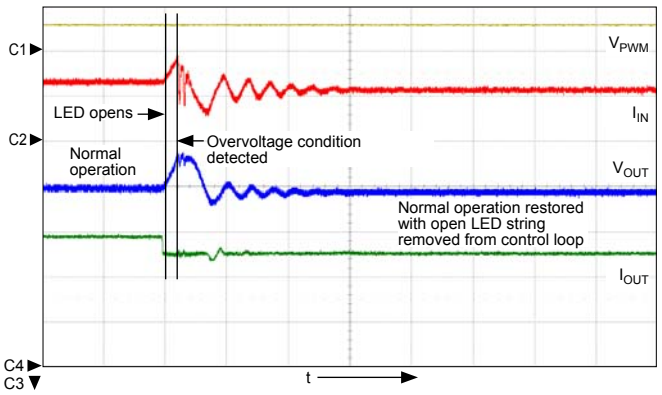


Figure 5. Overvoltage protection circuit. Three alternative configurations at (A) are available, as follows:

External Component	OVP Rating
ROVP only	up to 45 V
DZ only	up to 47 V
both ROVP and DZ	redundancy



Symbol	Parameter	Units/Division
C1	V_{PWM}	5.00 V
C2	I_{IN}	500 mA
C3	v_{out}	5.00 V
C4	I_{out}	200 mA
t	time	200 µs



Symbol	Parameter	Units/Division
C1	V_{PWM}	5.00 V
C2	I_{IN}	500 mA
C3	v_{out}	5.00 V
C4	I_{out}	100 mA
t	time	200 µs

Figure 4. Timing of overvoltage protection (OVP) function when open LEDs are detected at startup (left) and during normal operation (right).

Application Information

Design Example

This section provides a method for selecting component values when designing an application using the A8504.

Assumptions For the purposes of this example, the following are given as the application requirements:

- V_{BAT}: 8 to 21 V
- V_{IN}: 5 V
- Quantity of LED channels: 6
- Quantity of LEDs per channel: 8
- LED current per channel, I_{LED}: 40 mA
- V_f at 40 mA: 3 to 3.4 V
- f_{SW}: 2 MHz
- T_A(max): 65°C

Dimming Use a 100 Hz PWM signal on the PWM pin. The A8504 can work with wide range of PWM frequencies, taking about 6 µs typical (10 µs maximum) to turn on. This delay may have a noticeable effect at high PWM frequencies combined with low duty cycles. For example, at 100 Hz and 10% duty cycle, the PWM on-period is 1 ms. In that period, a delay of 6 µs causes only a 0.6% error. If the PWM frequency is 1 kHz, this error is 6%. However, error due to turn-on delay can be nullified by increasing the applied PWM duty cycle.

Procedure The procedure consists of selecting the appropriate configuration and then the individual component values, in an ordered sequence.

1. Identify the SEL*x* pins to use. For 6 channels:
   - connect pins SEL1 and SEL3 to V_{IN}
   - connect pin SEL2 to AGND
2. Connect LEDs to pins LED1 through LED6 (leave pins LED7 and LED8 open).
3. Select resistor RISET (connected between pin ISET and AGND). Given I_{LED} = 40 mA and V_{ISET} = 1.23 V typical, then:

$$R_{ISET} = 1.23 / (40/460) = 14.2\ k\Omega\ . \quad (1)$$

   Select a common value: 14.3 kΩ, 1%.
4. Select resistor RFSET (connected between pin FSET and AGND). Given:

$$R_{FSET} = 26.03 / f_{SW}\ , \quad (2)$$

   for a 2 MHz switching frequency, select:

$$R_{FSET} = 26.03 / 2 = 13\ k\Omega\ .$$

5. Select resistor ROVP (connect to the OVP pin to set the OVP level, V_{OUT}(max)). Given V_f(max) = 3.4 V, then:

$$V_{OUT}(max) = 3.4 \times 8 + 0.5 = 27.7\ V\ . \quad (3)$$

   With a 15% margin, to set the output OVP level, given an I_{OVPH} of 49 µA typical, and V_{OVP} = 30 V:

$$R_{OVP} = (32 - 30) / 49 = 40.8\ k\Omega\ . \quad (4)$$

   Select a common value: 41.2 kΩ.
6. Select inductor L1. This should assume a maximum duty cycle, D(max), at V_{BAT}(min) and 90% efficiency.

$$D = 1 - (V_{BAT} \times \eta) / V_{OUT} \quad (5)$$

$$D(max) = 1 - (8 \times 0.9) / 27.7 = 74\%\ .$$

   Then calculate maximum switch on-time:

$$t_{on}(max) = D(max) / f_{SW} \quad (6)$$

$$= 0.74 / 2\ MHz = 370\ ns\ .$$

   Maximum input current can be calculated as:

$$I_{BAT} = (V_{OUT} \times I_{OUT}) / (V_{BAT}(min) \times \eta) \quad (7)$$

$$I_{BAT}(max) = [27.7\ (40 \times 6)] / (8 \times 0.9) = 923\ mA\ .$$

   Set inductor ripple at 60% of I_{BAT}(max):

$$\Delta I_L = 0.6 \times 923 = 554\ mA$$

   Given, during switch on-time:

$$V_{BAT} = L \times \Delta I_L \times f_{SW} / D \quad (8)$$

$$8 = L \times 0.554 \times 2 / 0.74, \text{ and}$$

$$L = 5.3\ \mu H\ .$$

   Select a common value, 6.8 µH.

   It is recommended to select an inductor that can handle a DC current level that is greater than 923 mA, at the peak current level (saturation) of 923 mA + 554 / 2 = 1200 mA. This is to ensure that the inductor does not saturate at any steady state or transient condition, within specified temperature and tolerance ranges. Inductor saturation level decreases with increasing temperature. It is advisable to use a inductor with a saturation level of 1.6 A, because the switch current limit is 1.8 A typical. The inductor should have a minimum DC resistance and core loss for better efficiency.

7. Select output capacitor COUT (connect between the A8504 and the LEDs), given:

$$C_{OUT} = I_{OUT} \times t_{on} / \Delta V_{OUT} \ , \qquad (9)$$

where I_{OUT} is the total output current, and ΔV_{OUT} is the output voltage ripple, 0.5% of V_{OUT} (0.05 × 27.7 = 0.14 V). Then:

$$C_{OUT} = (40 \text{ mA} \times 6) \times 370 \text{ ns} / 0.14 = 0.63 \ \mu\text{F} \ .$$

Select a ceramic capacitor with a 35 or 50 V rating, X5R or X7R grade. Usually capacitance at 35 V drops significantly compared to the 0 V specification. Typically, this requires the selection of a 2.2 µF capacitor to compensate for DC voltage bias derating.

The rms current through capacitor should be selected such that internally-generated temperature rise is limited to 10°C to 20°C. The rms current through COUT is given by:

$$I_{COUTrms} = I_{OUT} \times [(D+r^2/12) / (1 - D)]^{1/2} , \qquad (10)$$

where $r = \Delta I_L / I_{BAT} = 0.554 \text{ mA} / 0.923 \text{ mA} = 0.6$.

COUT should have an rms current rating greater than:

$$(40 \text{ mA} \times 6) \times \{[0.74 + (0.36 / 12)]/(1–0.74)\}^{1/2} = 0.48 \text{ A}.$$

8. Select input capacitor CBAT (connect to battery input), given:

$$C_{BAT} = \Delta I_L / (V_{BAT}(\text{min}) \times f_{SW} \times \Delta V_{INripple} \ , \qquad (11)$$

where $\Delta V_{INripple}$ is the input ripple voltage, which can be assumed to be 1% of V_{BAT}. Then:

$$C_{IN} = 0.554 \text{ mA} / (8 \times 2 \text{ MHz} \times 0.08) = 0.4 \ \mu\text{F} \ .$$

Select a 1 µF or higher, 25 or 35 V, ceramic capacitor, X5R or X7R grade.

The rms current through capacitor should be selected such that internally-generated temperature rise is limited to 10°C. The rms current through CBAT is given by:

$$I_{BATrms} = (I_{OUT} \times r) / [(1 - D) \times 3.46], \qquad (12)$$

$$= [(40 \text{ mA} \times 6) \times 0.6] / [(1 – 0.74) \times 3.46] = 160 \text{ mA} .$$

9. Select the boost diode D1 (connect between the SW pins and the output). D1 should be a Schottky diode with low forward drop and junction capacitance.

   The diode reverse voltage rating should be greater than V_{OUT}. A 50 V diode rating is recommended.

   The diode DC current rating should be greater than I_{OUT} and the peak repetitive current rating should be greater than $I_{BAT} + \Delta I_L / 2$.

10. Select the compensation capacitor CC (connect between the COMP pin and ground. Typically, use a 0.1 to 0.47 µF capacitor for stability.

High Output Current Operation

LED strings can be paralleled for higher current. The A8504 can sink up to 40 mA through each sink. These outputs can be connected together with various possibilities for higher current as shown in figure 7. As an example, for an application with up to 50 mA using 3 parallel strings: LED1 connected with LED2, LED3 with LED4, and LED5 with LED6; LED7 and LED8 open; SEL1 and SEL3 set logic high, and SEL2 set low.

I_{LED}(max)	Quantity of Strings	SEL1	SEL2	SEL3	LED1	LED2	LED3	LED4	LED5	LED6	LED7	LED8
25	8	H	H	H								
25	7	L	H	H								NC
25	6	H	L	H							NC	NC
25	5	L	L	H						NC	NC	NC
25	4	H	H	L					NC	NC	NC	NC
25	3	L	H	L				NC	NC	NC	NC	NC
25	2	H	L	L			NC	NC	NC	NC	NC	NC
25	1	L	L	L		NC	NC	NC	NC	NC	NC	NC
50	4	H	H	H	Connect		Connect		Connect		Connect	
50	3	H	L	H	Connect		Connect		Connect		NC	NC
50	2	H	H	L	Connect		Connect		NC	NC	NC	NC
50	1	H	L	L	Connect		NC	NC	NC	NC	NC	NC
100	2	H	H	H	Connect				Connect			
100	1	H	H	L	Connect				NC	NC	NC	NC
200	1	H	H	H	Connect							

Figure 7. LED strings can be combined to allow various maximum current levels to be applied. The “Connect” notes indicate LED strings connected together.

Typical Application Circuits

A typical application circuit for dimming an LCD monitor backlight with multiple LED strings is shown in figure 1. Figure 8 shows two dimming methods: digital PWM control (PWM signal on the PWM pin) and analog PWM control, with the analog signal, V_A, applied to the ISET pin through a resistor, RA.

The current flowing through RA can be calculated as:

$$I_A = V_A / R_A .$$

This current changes the reference current, I_{SET}, as follows:

$$I_{SET} = V_{SET} / R_{SET} - (V_A - V_{SET}) / R_A .$$

LED current can be changed by changing V_A. I_{SET} can be changed in the range from 40 µA to 100 µA.

Application Circuit for 1000:1 Dimming Level

A wider dimming range can be achieved by changing the reference current, I_{SET}, while using PWM dimming. For higher output, current levels turn on Q1. R_{ISET} and R_{ISETP} set the 100% current level. This current level can be set to 45 mA, and then it can be dimmed by applying 100% to 0.25% duty cycle on the PWM pin. The reference current can be reduced by turning off Q1. LED current can be dimmed to 18 mA by reducing reference current through ISET pin. This provides 1000:1 combined dimming level range. Figure 10 shows the accuracy, Err_{LEDX}, results using this circuit.

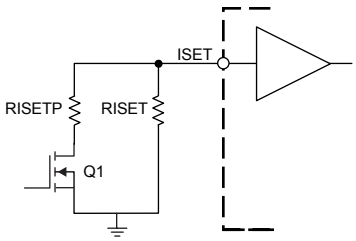


Figure 9. Configuration for 1000:1 dimming.

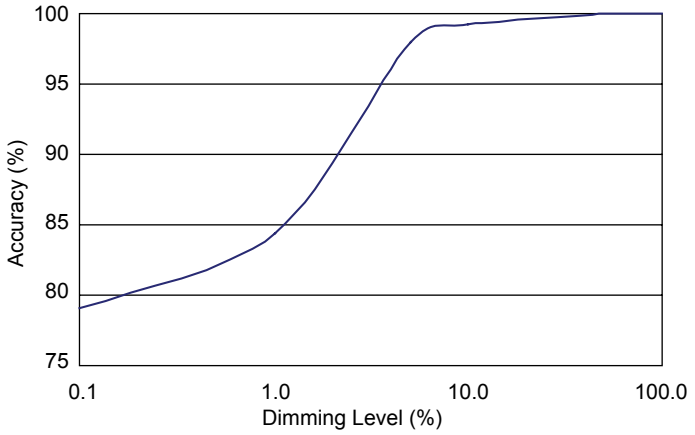


Figure 10. Typical accuracy, normalized to the 100% current level, versus dimming level, with F_{PWM} = 100 Hz.

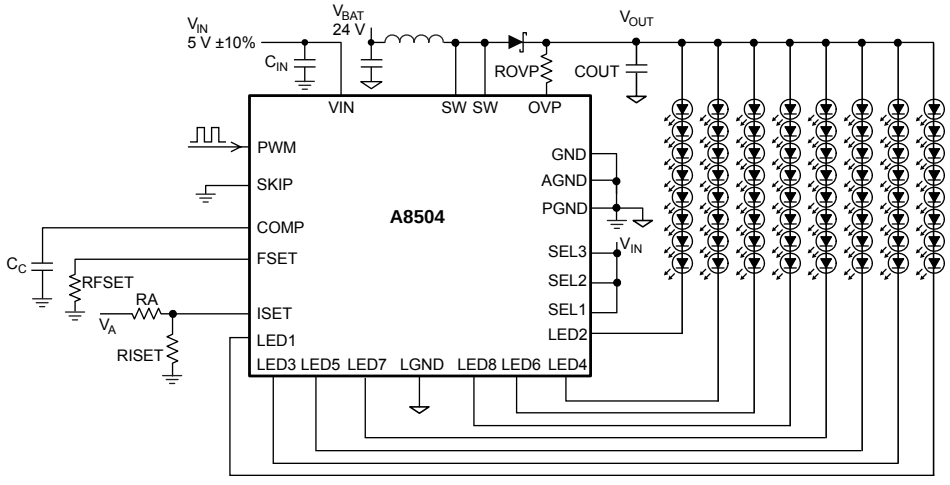


Figure 8. Typical application circuit for PWM dimming, using digital PWM (on the PWM pin).

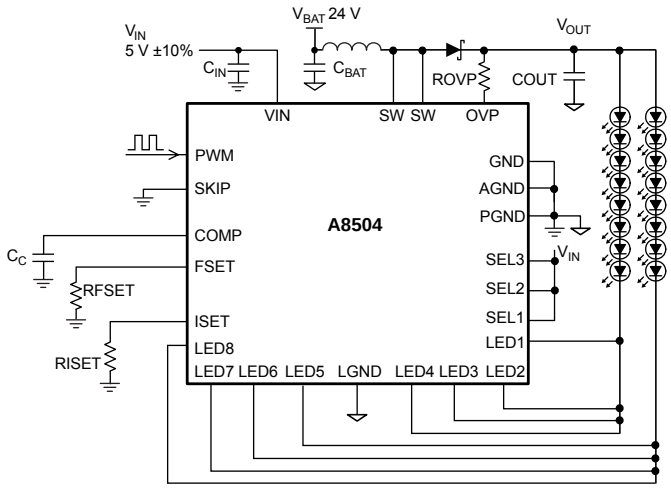


Figure 11. Typical application circuit for PWM dimming, using digital PWM (on the PWM pin). Showing configuration of 16 WLEDs at 160 mA, in two strings of 8 LEDs each.

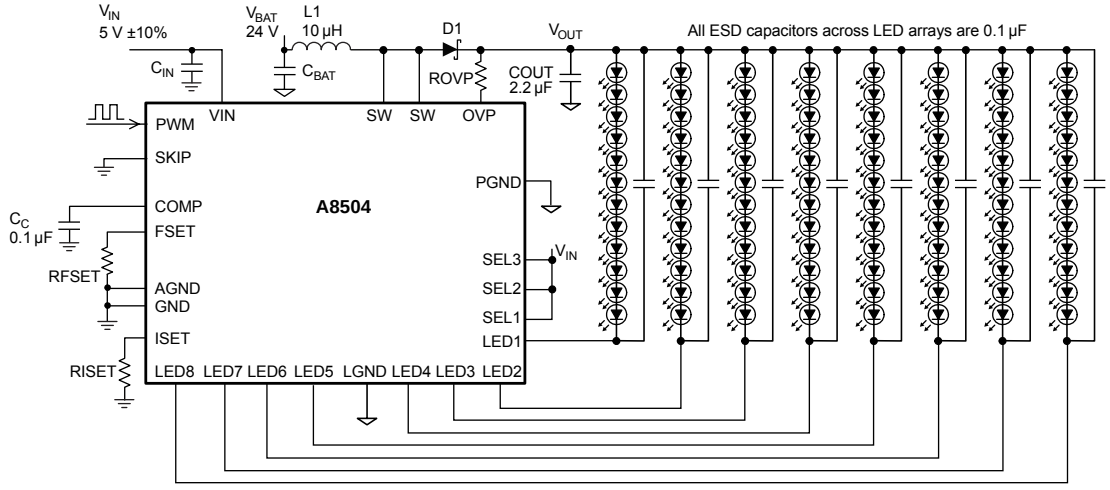


Figure 12. Typical application circuit for LED modules with ESD capacitors.

PCB Layout Guidelines

The A8504 evaluation board provides a useful model for designing application circuit layouts. The following guidelines should be observed:

- Place the supply bypass capacitor, C8, close to the VIN pin and the ground plane.
- Route analog ground, digital signal ground, LED ground (LGND pin), and power ground (PGND pin) separately. Connect all these grounds at the pad for the exposed thermal pad under the A8504, serving as a star ground.
- Place the input capacitors, C2 and C7, the inductor, L1, the boost diode D1, and the internal MOSFET and output capacitor, C4, so that they form the smallest loop practical. Avoid long traces for these paths.
- Place the RISET, RFSET, and OVP resistors and the compensation capacitor, C5, close to the ISET, FSET, OVP, and COMP pins, respectively.
- Provide a substantial solder pad under the exposed thermal pad on the bottom side of the A8504, to provide good thermal conduction. Connect the PCB solder pad to the PCB ground plane with multiple thermal vias. For a thermal via specification, please refer to JEDEC guidelines.
- For best thermal performance, avoid thermal stresses.

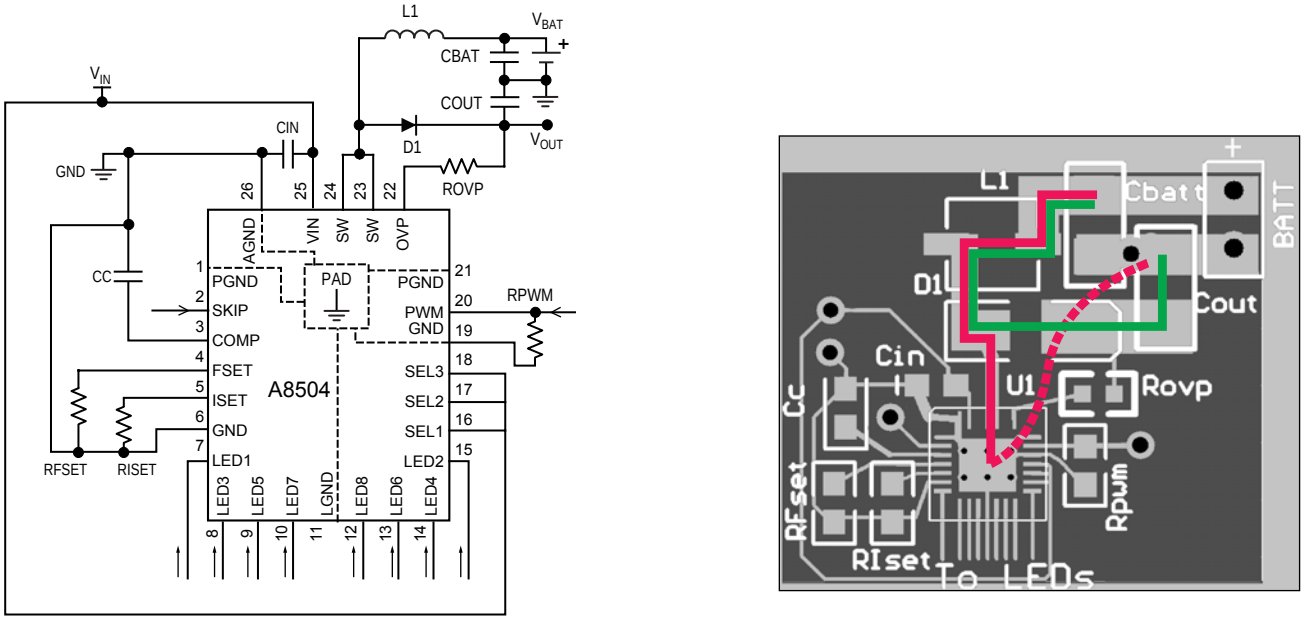


Figure 13. Schematic diagram of A8504 typical application circuit and composite view of typical PCB layout. In the composite view, the red line superimposed represents the current loop during switch on-time (return through the A8504 device and the PCB ground plane). The green line represents the current loop during off-time. Both of these loops should be designed to be as short as practicable.

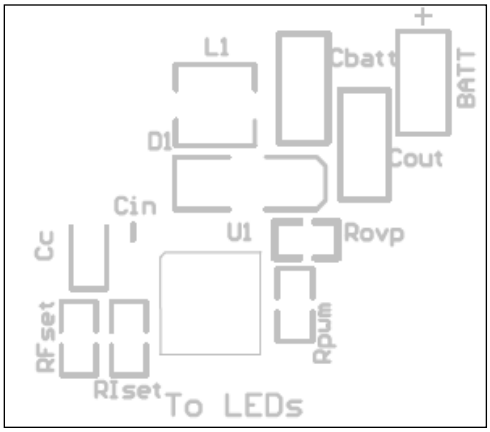


Figure 14. A8504 typical PCB layout silkscreen layer.

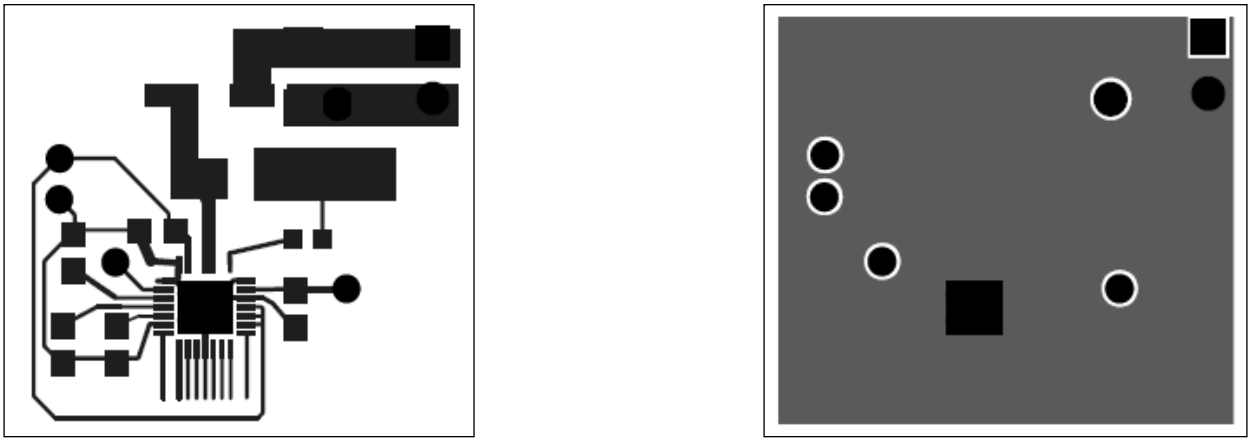
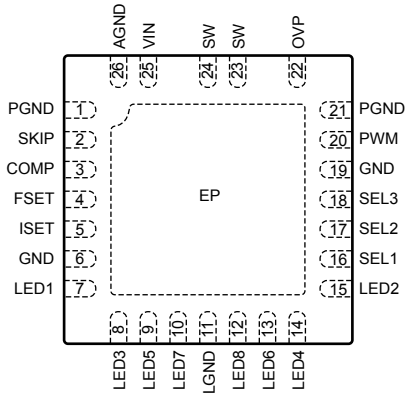


Figure 15. A8504 typical PCB layout top signal layer (left) and bottom ground plane layer (right)

Recommended Components Table (for application shown in figure 1)

Component	Reference Designator	Value	Part Number	Vendor
Capacitor	C_{BAT}	2.2 µF / 50 V		TDK
Capacitor	C_{OUT}	2.2 µF / 50 V		TDK
Capacitor	C_{IN}, C_C	0.1 µF / 6.3 V		
Diode	D1	60 V / 1.5 A	IR 10MQ060NTRPBF	International Rectifier
IC	A8504	–	A8504	Allegro MicroSystems
Inductor	L1	10 µH	SLF6028T-100M1R3-PF	TDK
		4.7 µH	VLS4012T-4R7M1R1	TDK
		4.7 µH	NR4012T4R7M	Taiyo Yuden
Resistor	RISET	14.3 kΩ		
Resistor	RFSET	24 kΩ		
Resistor	ROVP	270 kΩ		

Pin-out Diagram

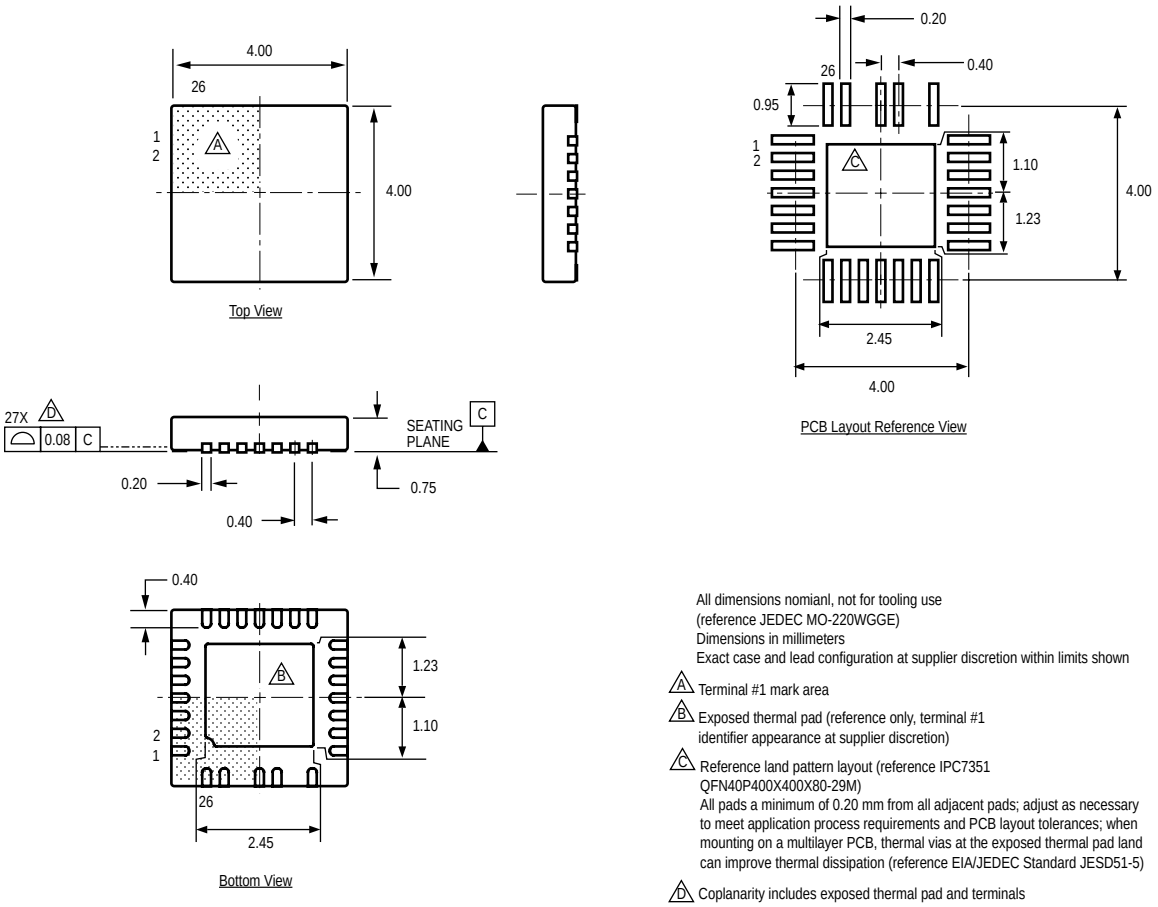


(Top View)

Terminal List Table

Number	Name	Description
1	PGND	Power ground pin.
2	SKIP	Reduces boost switching frequency in case of light load to improve frequency. Normally, this pin should be low; when high, f_{SW} is divided by 4.
3	COMP	Compensation pin; connect external compensation network for boost converter.
4	FSET	Sets boost switching frequency. Connect RFSET from FSET to GND to set frequency. Range for RFSET is 13 to 40 kΩ.
5	ISET	Sets 100% current through LED string. Connect RISET from ISET to GND. Range for RISET is 8.45 to 30 kΩ.
6	GND	Connect to AGND.
7	LED1	LED*x* capable of 45 mA.
8	LED3	
9	LED5	
10	LED7	
11	LGND	Power ground pin for LED current sink.
12	LED8	LED*x* capable of 45 mA.
13	LED6	
14	LED4	
15	LED2	
16	SEL1	SEL1, SEL2, and SEL3 decide active LED strings.
17	SEL2	
18	SEL3	
19	GND	Connect to AGND.
20	PWM	On/off and on/off LED current control with external PWM. Apply logic level PWM for PWM controlled dimming mode. When unused, connect to AGND.
21	PGND	Power ground pin.
22	OVP	Connect to this pin to output capacitor +Ve node through a resistor to enable OVP (overvoltage protection). Default OVP level with 0 Ω resistor is 30 V, and it can be programmed up to 47 V.
23	SW	DMOS drain node.
24	SW	
25	VIN	Input supply for the IC. Decouple with a 0.1 µF ceramic capacitor.
26	AGND	Circuit ground pin.
–	EP	Exposed pad. Electrically connected to PGND and LGND; connect to PCB copper plane for heat transfer.

Package EC, 4 × 4 mm 26-Pin QFN/MLP



All dimensions nomianl, not for tooling use
(reference JEDEC MO-220WGGE)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN40P400X400X80-29M)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

For the latest version of this document, visit our website:

www.allegromicro.com