DATA SHEET

PCA9533
4-bit I^2C LED dimmer

Product data

2003 Sep 19

Philips
Semiconductors

PHILIPS

4-bit I²C LED dimmer PCA9533

FEATURES

- 4 LED drivers (on, off, flashing at a programmable rate)
- 2 selectable, fully programmable blink rates (frequency and duty cycle) between 0.625 and 160 Hz (1.6 seconds and 6.25 milliseconds)
- 256 brightness steps
- Input/outputs not used as LED drivers can be used as regular GPIOs
- Internal oscillator requires no external components
- I²C interface logic compatible with SMBus
- Internal power-on reset
- Noise filter on SCL/SDA inputs
- 4 open drain outputs directly drive LEDs to 25 mA
- Edge rate control on outputs
- No glitch on power-up
- Supports hot insertion
- Low stand-by current
- Operating power supply voltage range of 2.3 V to 5.5 V
- 0 to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 150 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: SO8, TSSOP8

DESCRIPTION

The PCA9533 is a 4-bit I²C & SMBus I/O expander optimized for dimming LEDs in 256 discrete steps for Red/Green/Blue (RGB) color mixing and back light applications.

The PCA9533 contains an internal oscillator with two user programmable blink rates and duty cycles coupled to the output PWM. The LED brightness is controlled by setting the blink rate high enough (> 100 Hz) that the blinking can not be seen and then using the duty cycle to vary the amount of time the LED is on and thus the average current through the LED.

The initial setup sequence programs the two blink rates/duty cycles for each individual PWM. From then on, only one command from the bus master is required to turn individual LEDs ON, OFF, BLINK RATE 1 or BLINK RATE 2. Based on the programmed frequency and duty cycle, BLINK RATE 1 and BLINK RATE 2 will cause the LEDs to appear at a different brightness or blink at periods up to 1.6 second. The open drain outputs directly drive the LEDs with maximum output sink current of 25 mA per bit and 100 mA per package.

To blink LEDs at periods greater than 1.6 second the bus master (MCU, MPU, DSP, chipset, etc.) must send repeated commands to turn the LED on and off as is currently done when using normal I/O Expanders like the Philips PCF8574 or PCA9554. Any bits not used for controlling the LEDs can be used for General Purpose Parallel Input/Output (GPIO) expansion which provides a simple solution when additional I/O is needed for ACPI power switches, sensors, pushbuttons, alarm monitoring, fans, etc.

Power On Reset (POR) initializes the registers to their default state causing the bits to be set high (LED off).

Due to pin limitations, the PCA9533 is not featured with hardware address pins. The PCA9533/01 and the PCA9533/02 have different fixed I²C addresses allowing operation of both on the same bus.

PIN CONFIGURATION

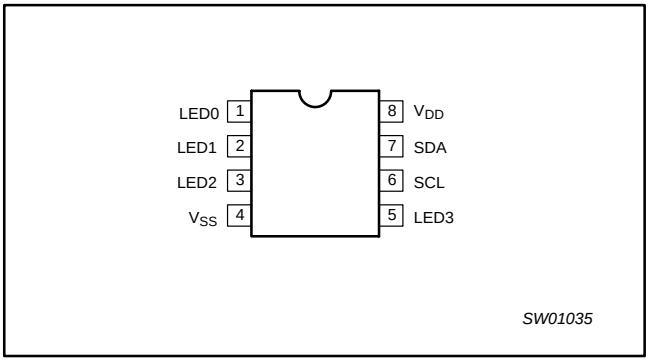


Figure 1. Pin configuration

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	LED0	LED driver 0
2	LED1	LED driver 1
3	LED2	LED driver 2
4	V_{SS}	Supply ground
5	LED3	LED driver 3
6	SCL	Serial clock line
7	SDA	Serial data line
8	V_{DD}	Supply voltage

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	TOPSIDE MARK	DRAWING NUMBER
8-Pin Plastic SO	-40 to +85 °C	PCA9533D/01	P9533/1	SOT96-1
8-Pin Plastic SO	-40 to +85 °C	PCA9533D/02	P9533/2	SOT96-1
8-Pin Plastic TSSOP	-40 to +85 °C	PCA9533DP/01	P33/1	SOT505-1
8-Pin Plastic TSSOP	-40 to +85 °C	PCA9533DP/02	P33/2	SOT505-1

Standard packing quantities and other packaging data is available at www.philipslogic.com/packaging.
I²C is a trademark of Philips Semiconductors Corporation.

BLOCK DIAGRAM

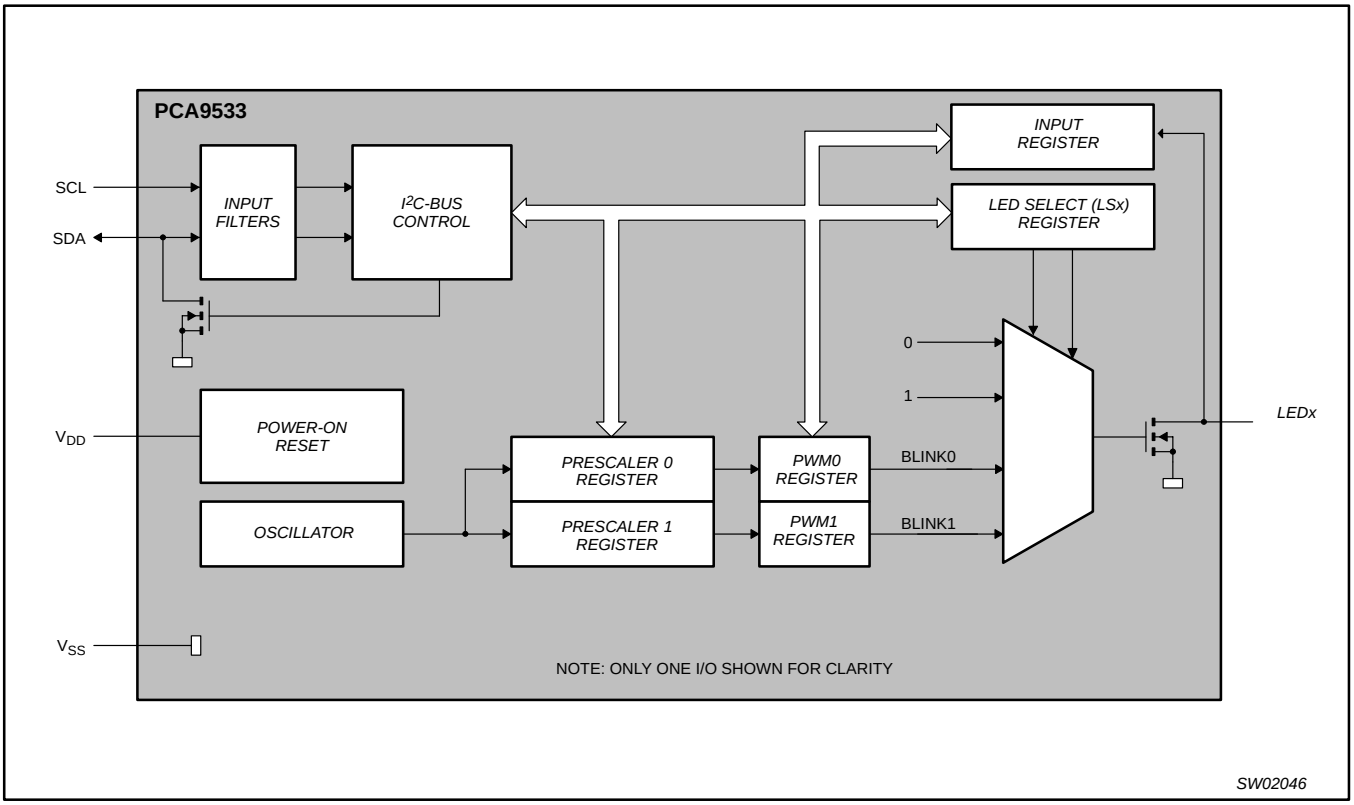


Figure 2. Block diagram

DEVICE ADDRESSING

Following a START condition the bus master must output the address of the slave it is accessing. The address of the PCA9533/01 is shown in Figure 3 and PCA9533/02 in Figure 4.

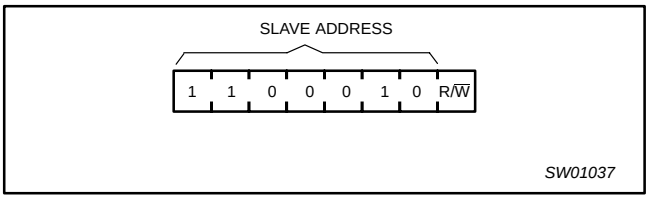


Figure 3. Slave address — PCA9533/01

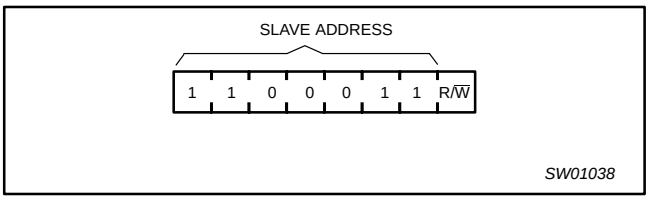


Figure 4. Slave address — PCA9533/02

The last bit of the address byte defines the operation to be performed. When set to logic 1 a read is selected while a logic 0 selects a write operation.

CONTROL REGISTER

Following the successful acknowledgement of the slave address, the bus master will send a byte to the PCA9533 which will be stored in the Control Register.

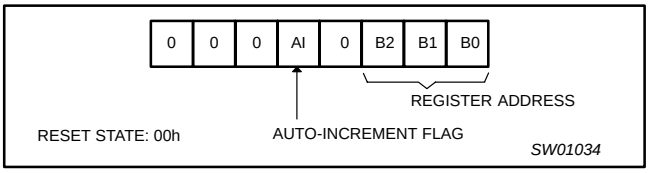


Figure 5. Control register

CONTROL REGISTER DEFINITION

B2	B1	B0	REGISTER NAME	TYPE	REGISTER FUNCTION
0	0	0	INPUT	READ	INPUT REGISTER
0	0	1	PSC0	READ/ WRITE	FREQUENCY PRESCALER 0
0	1	0	PWM0	READ/ WRITE	PWM REGISTER 0
0	1	1	PSC1	READ/ WRITE	FREQUENCY PRESCALER 1
1	0	0	PWM1	READ/ WRITE	PWM REGISTER 1
1	0	1	LS0	READ/ WRITE	LED SELECTOR

REGISTER DESCRIPTION

The lowest 3 bits are used as a pointer to determine which register will be accessed.

If the auto-increment flag is set, the three low order bits of the Control Register are automatically incremented after a read or write. This allows the user to program the registers sequentially. The contents of these bits will rollover to '000' after the last register is accessed.

When auto-increment flag is set (AI = 1) and a read sequence is initiated, the sequence must start by reading a register different from the input register (B2 B1 B0 ≠ 0 0 0).

Only the 3 least significant bits are affected by the AI flag.

Unused bits must be programmed with zeroes.

INPUT — INPUT REGISTER

bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	X	X	X	X

The INPUT register reflects the state of the device pins. Writes to this register will be acknowledged but will have no effect.

PSC0 — FREQUENCY PRESCALER 0

bit	7	6	5	4	3	2	1	0
default	0	0	0	0	0	0	0	0

PSC0 is used to program the period of the PWM output.

$$\text{The period of BLINK0} = \frac{(\text{PSC0} + 1)}{152}$$

PWM0 — PWM REGISTER 0

bit	7	6	5	4	3	2	1	0
default	1	0	0	0	0	0	0	0

The PWM0 register determines the duty cycle of BLINK0. The outputs are LOW (LED on) when the count is less than the value in PWM0 and HIGH (LED off) when it is greater. If PWM0 is programmed with 00h, then the PWM0 output is always HIGH (LED off) .

$$\text{The duty cycle of BLINK0 is:} \frac{\text{PWM0}}{256}$$

PSC1 — FREQUENCY PRESCALER 1

bit	7	6	5	4	3	2	1	0
default	0	0	0	0	0	0	0	0

PSC1 is used to program the period of PWM output.

$$\text{The period of BLINK1} = \frac{(\text{PSC1} + 1)}{152}$$

PWM1 — PWM REGISTER 1

bit	7	6	5	4	3	2	1	0
default	1	0	0	0	0	0	0	0

The PWM1 register determines the duty cycle of BLINK1. The outputs are LOW (LED on) when the count is less than the value in PWM1 and HIGH (LED off) when it is greater. If PWM1 is programmed with 00h, then the PWM1 output is always HIGH (LED off).

$$\text{The duty cycle of BLINK1 is:} \frac{\text{PWM1}}{256}$$

LS0 — LED SELECTOR

	LED3		LED2		LED 1		LED 0	
bit	7	6	5	4	3	2	1	0
default	0	0	0	0	0	0	0	0

The LSx LED select registers determine the source of the LED data.
- 00 = Output is set low Hi-Z (LED off - default)
- 01 = Output is set low (LED on)
- 10 = Output blinks at PWM0 rate
- 11 = Output blinks at PWM1 rate

POWER-ON RESET

When power is applied to V_{DD}, an internal Power On Reset holds the PCA9533 in a reset state until V_{DD} has reached V_{POR}. At this point, the reset condition is released and the PCA9533 registers are initialized to their default states, with all outputs in the off state.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 6).

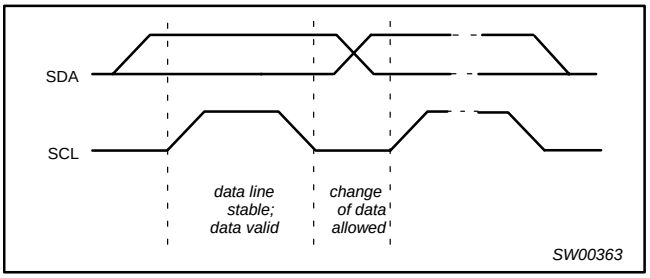


Figure 6. Bit transfer

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P) (see Figure 7).

System configuration

A device generating a message is a transmitter: a device receiving is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves (see Figure 8).

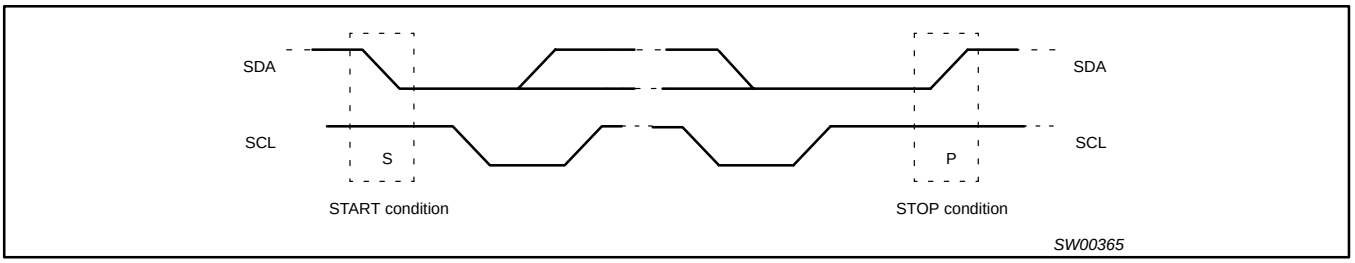


Figure 7. Definition of start and stop conditions

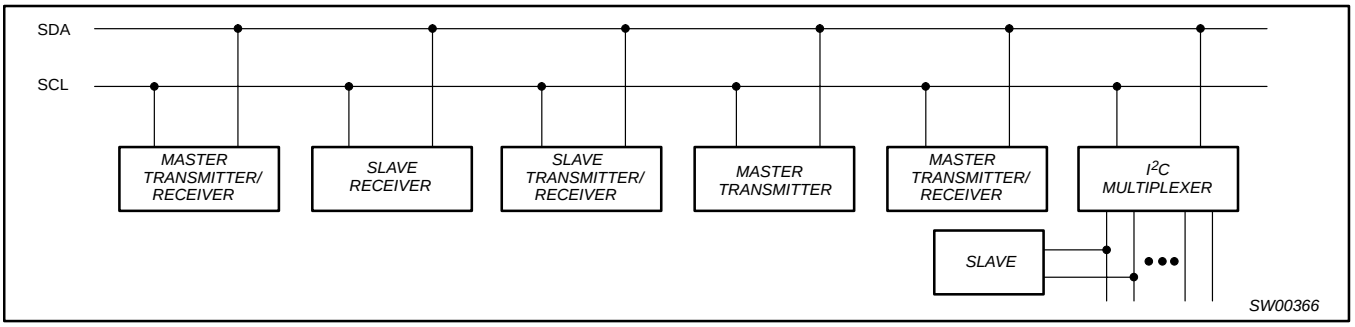


Figure 8. System configuration

Acknowledge

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

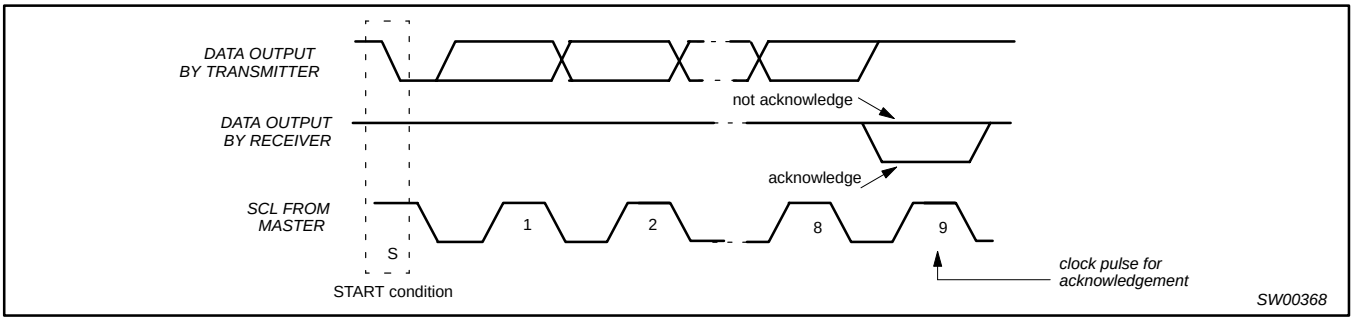


Figure 9. Acknowledgement on the I2C-bus

Bus transactions

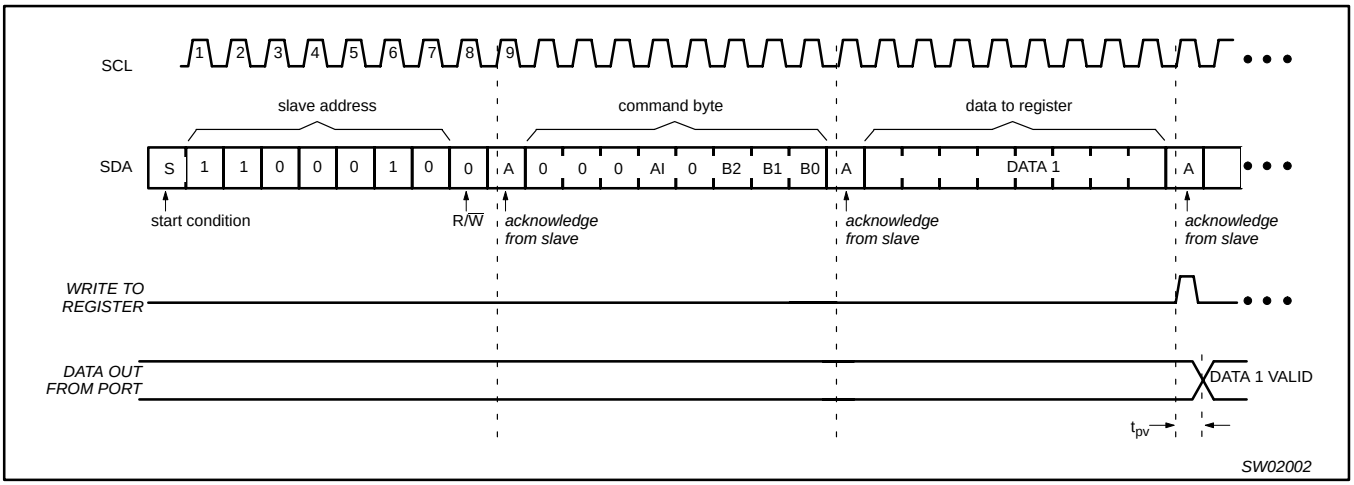


Figure 10. WRITE to register

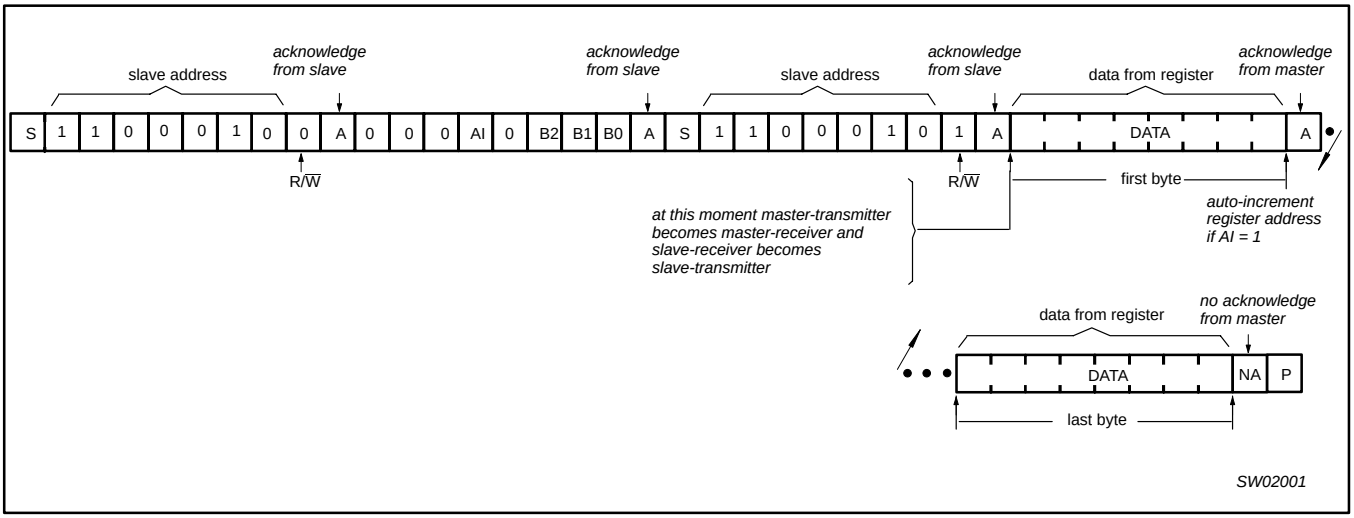
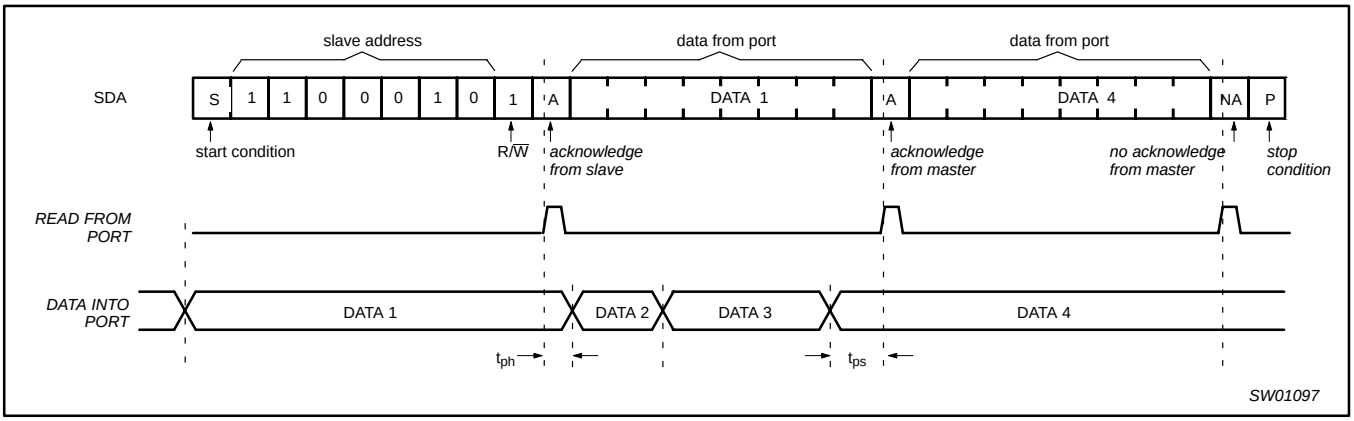


Figure 11. READ from register



NOTES:
1. This figure assumes the command byte has previously been programmed with 00h.
2. PCA9533/01 shown.

Figure 12. READ input port register

APPLICATION DATA

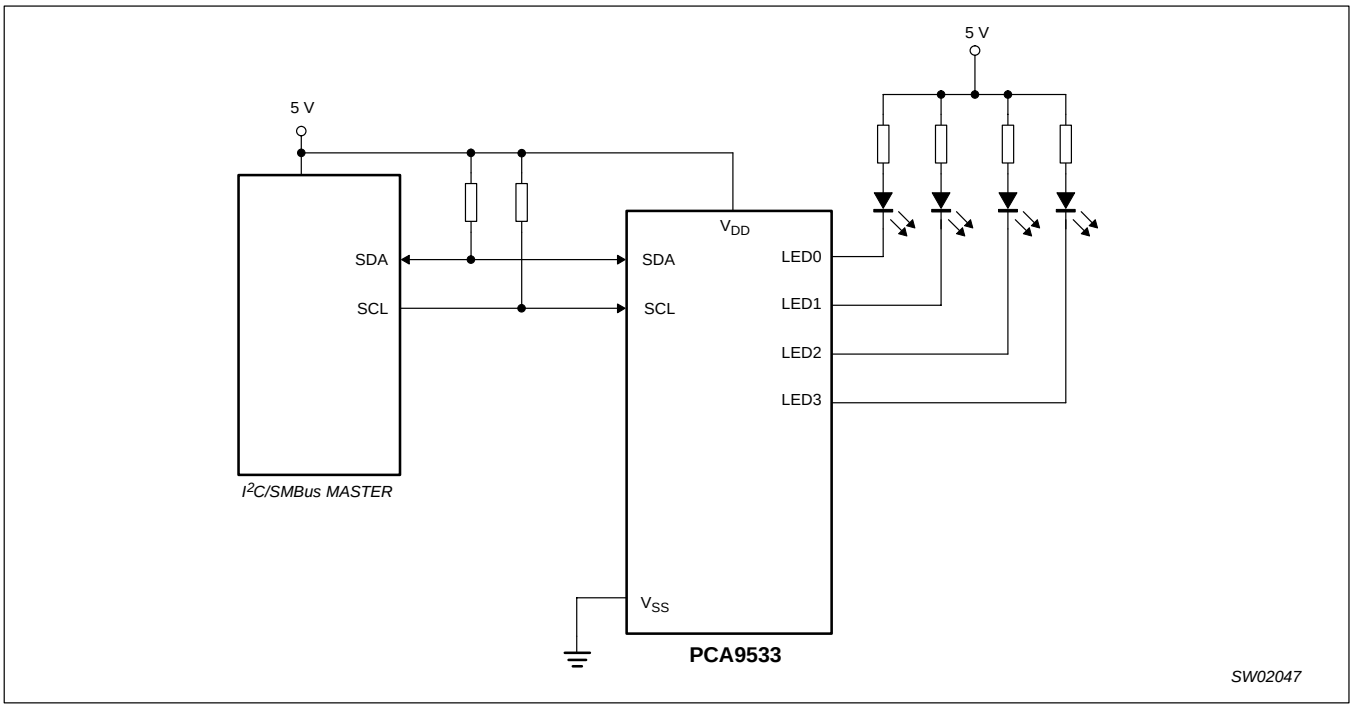


Figure 13. Typical application

Minimizing I_{DD} when the I/O is used to control LEDs

When the I/Os are used to control LEDs, they are normally connected to V_{DD} through a resistor as shown in Figure 13. Since the LED acts as a diode, when the LED is off the I/O V_{IN} is about 1.2 V less than V_{DD}. The supply current , I_{DD}, increases as V_{IN} becomes lower than V_{DD} and is specified as ΔI_{DD} in the DC characteristics table.

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V_{DD} when the LED is off. Figure 14 shows a high value resistor in parallel with the LED. Figure 15 shows V_{DD} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_{IN} at or above V_{DD} and prevents additional supply current consumption when the LED is off.

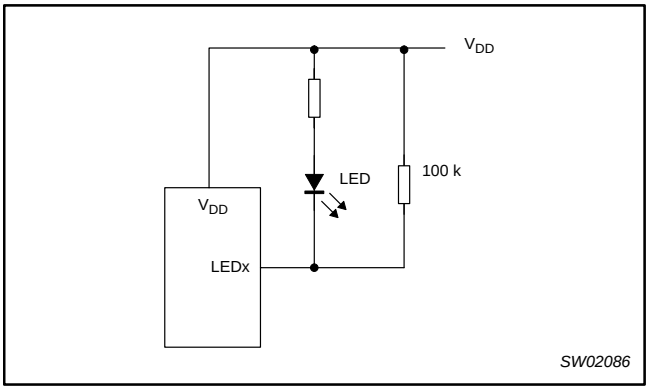


Figure 14. High value resistor in parallel with the LED

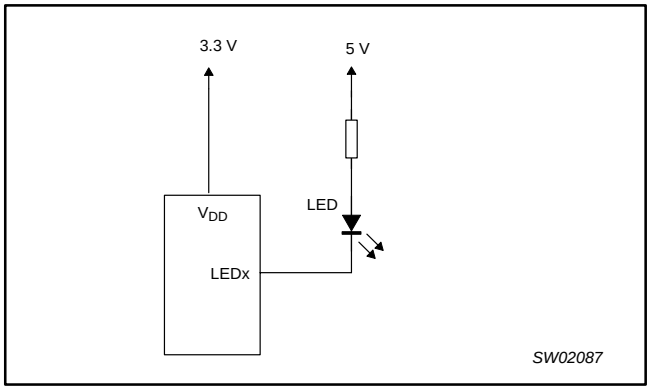


Figure 15. Device supplied by a lower voltage

Programming example

The following example will show how to set LED0 and LED1 off. It will set LED2 to blink at 1 Hz, 50% duty cycle. LED3 will be set to be dimmed at 25% of their maximum brightness (duty cycle = 25%). PCA9533/01 is used in this example.

Table 1.

	I²C-bus
Start	S
PCA9533 address	C4h
PSC0 subaddress + auto-increment	11h
Set prescaler PSC0 to achieve a period of 1 second: $\text{Blink period} = 1 = \frac{\text{PSC0} + 1}{152}$ PSC0 = 151	97h
Set PWM0 duty cycle to 50%: $\frac{\text{PWM0}}{256} = 0.5$ PWM0 = 128	80h
Set prescaler PWM1 to dim at maximum frequency Blink period = maximum PSC1 = 0	00h
Set PWM1 output duty cycle to 25%: $\frac{\text{PWM1}}{256} = 0.25$ PWM1 = 64	40h
Set LED0 on, LED1 off, LED2 set to blink at PSC0, PWM0, LED3 set to blink at PCS1, PWM1	E1h
Stop	P

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{DD}	Supply voltage		-0.5	6.0	V
$V_{I/O}$	DC voltage on an I/O		V_{SS} - 0.5	5.5	V
$I_{I/O}$	DC output current on an I/O		—	+25	mA
I_{SS}	Supply current		—	100	mA
P_{tot}	Total power dissipation		—	400	mW
T_{stg}	Storage temperature range		-65	+150	°C
T_{amb}	Operating ambient temperature		-40	+85	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC24 under "*Handling MOS devices*".

DC CHARACTERISTICS

V_{DD} = 2.3 to 5.5 V; V_{SS} = 0 V; T_{amb} = -40 to +85 °C; unless otherwise specified. TYP at 3.3 V and 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supplies						
V_{DD}	Supply voltage		2.3	—	5.5	V
I_{DD}	Supply current	Operating mode; V_{DD} = 5.5 V; no load; $V_I = V_{DD}$ or V_{SS}; f_{SCL} = 100 kHz	—	350	500	µA
I_{stb}	Standby current	Standby mode; V_{DD} = 5.5 V; no load; $V_I = V_{DD}$ or V_{SS}; f_{SCL} = 0 kHz	—	1.9	3.0	µA
ΔI_{DD}	Additional standby current	Standby mode; V_{DD} = 5.5 V; Every LED I/O at V_{IN} = 4.3 V; f_{SCL} = 0 kHz	—	—	325	µA
V_{POR}	Power-on reset voltage	No load; $V_I = V_{DD}$ or V_{SS}	—	1.7	2.2	V
Input SCL; input/output SDA						
V_{IL}	LOW-level input voltage		-0.5	—	0.3 V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7 V_{DD}	—	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4V	3	6.5	—	mA
I_L	Leakage current	$V_I = V_{DD} = V_{SS}$	-1	—	+1	µA
C_I	Input capacitance	$V_I = V_{SS}$	—	3.7	5	pF
I/Os						
V_{IL}	LOW-level input voltage		-0.5	—	0.8	V
V_{IH}	HIGH-level input voltage		2.0	—	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; V_{DD} = 2.3 V; Note 1	9	—	—	mA
		V_{OL} = 0.4 V; V_{DD} = 3.0 V; Note 1	12	—	—	mA
		V_{OL} = 0.4 V; V_{DD} = 5.0 V; Note 1	15	—	—	mA
		V_{OL} = 0.7 V; V_{DD} = 2.3 V; Note 1	15	—	—	mA
		V_{OL} = 0.7 V; V_{DD} = 3.0 V; Note 1	20	—	—	mA
		V_{OL} = 0.7 V; V_{DD} = 5.0 V; Note 1	25	—	—	mA
I_L	Input leakage current	V_{DD} = 3.6 V; V_I = 0 or V_{DD}	-1	—	1	µA
C_{IO}	Input/output capacitance		—	2.1	5	pF

NOTE:

1. Each I/O must be externally limited to a maximum of 25 mA and the device must be limited to a maximum current of 100 mA.

AC SPECIFICATIONS

SYMBOL	PARAMETER	STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNITS
		MIN	MAX	MIN	MAX	
f_{SCL}	Operating frequency	0	100	0	400	kHz
t_{BUF}	Bus free time between STOP and START conditions	4.7	—	1.3	—	µs
$t_{HD;STA}$	Hold time after (repeated) START condition	4.0	—	0.6	—	µs
$t_{SU;STA}$	Repeated START condition setup time	4.7	—	0.6	—	µs
$t_{SU;STO}$	Setup time for STOP condition	4.0	—	0.6	—	µs
$t_{HD;DAT}$	Data in hold time	0	—	0	—	ns
$t_{VD;ACK}$	Valid time for ACK condition[2]	—	600	—	600	ns
$t_{VD;DAT}$ (L)	Data out valid time[3]	—	600	—	600	ns
$t_{VD;DAT}$ (H)	Data out valid time[3]	—	1500	—	600	ns
$t_{SU;DAT}$	Data setup time	250	—	100	—	ns
t_{LOW}	Clock LOW period	4.7	—	1.3	—	µs
t_{HIGH}	Clock HIGH period	4.0	—	0.6	—	µs
t_F	Clock/Data fall time	—	300	20 + 0.1 C_b[1]	300	ns
t_R	Clock/Data rise time	—	1000	20 + 0.1 C_b[1]	300	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filters	—	50	—	50	ns
Port Timing						
t_{PV}	Output data valid	—	200	—	200	ns
t_{PS}	Input data setup time	100	—	100	—	ns
t_{PH}	Input data hold time	1	—	1	—	µs

NOTES:
1. C_b = total capacitance of one bus line in pF.
2. $t_{VD;ACK}$ = time for Acknowledgement signal from SCL low to SDA (out) low.
3. $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL low.

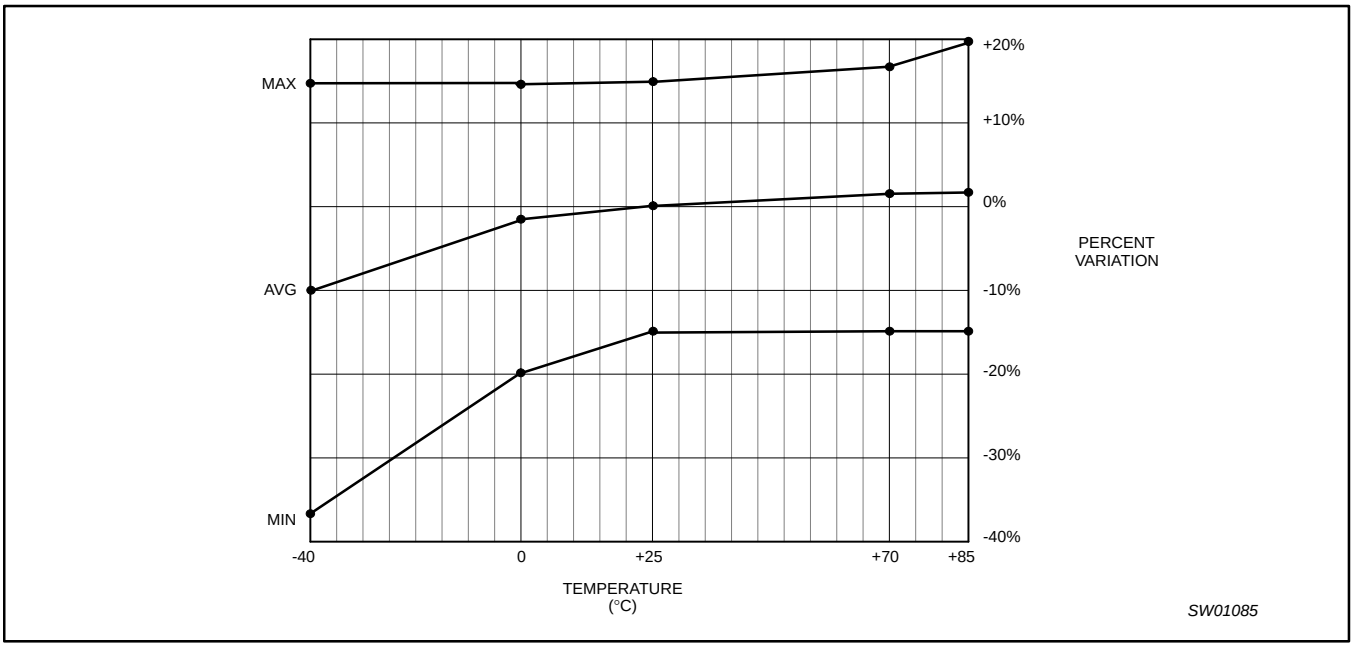


Figure 16. Typical frequency variation over process at V_{DD} = 2.3 V to 3.0 V

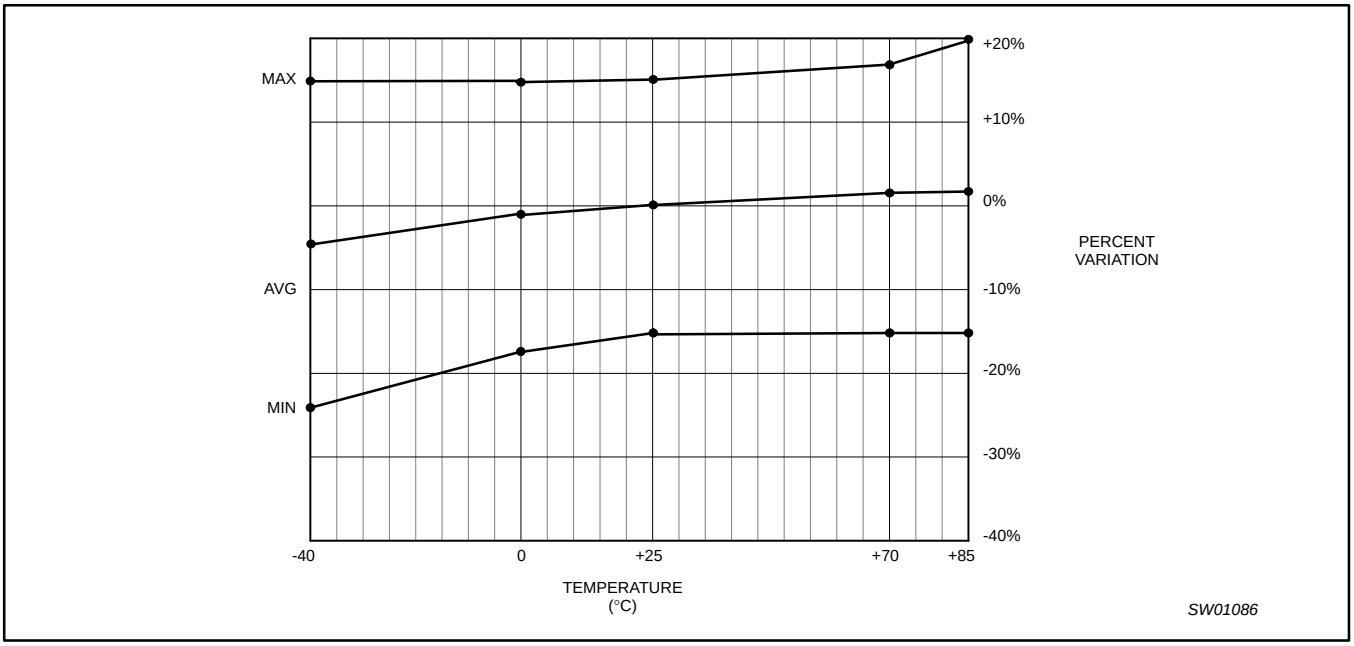


Figure 17. Typical frequency variation over process at V_{DD} = 3.0 V to 5.5 V

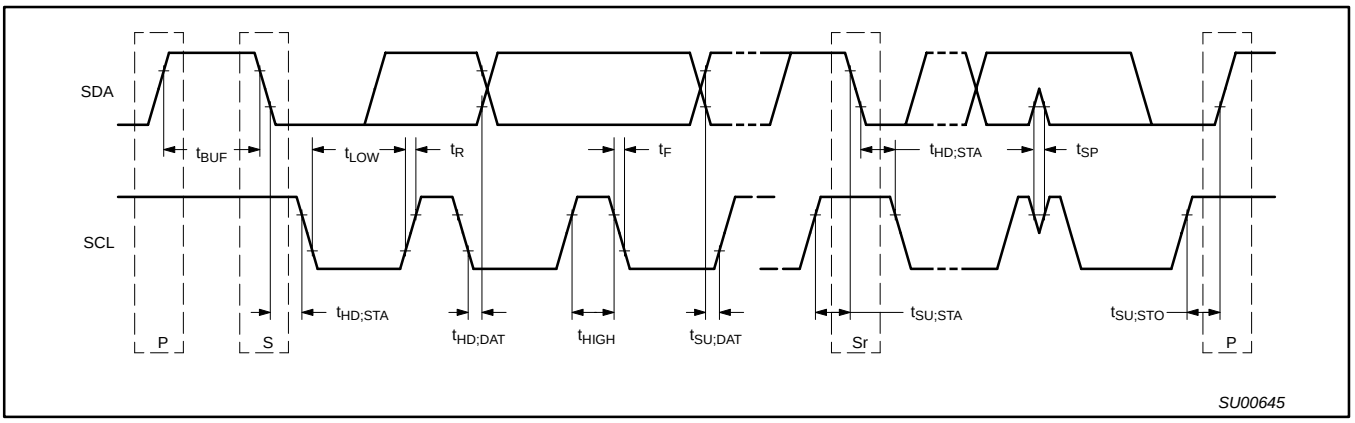


Figure 18. Definition of timing

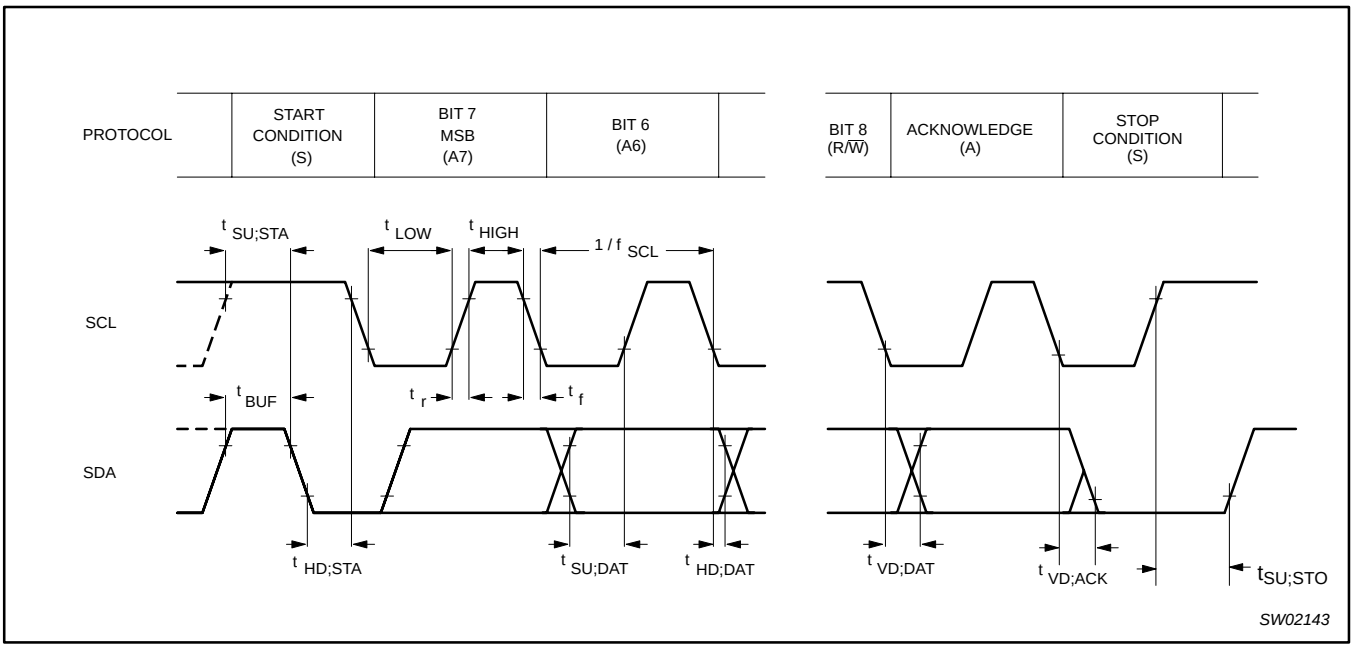
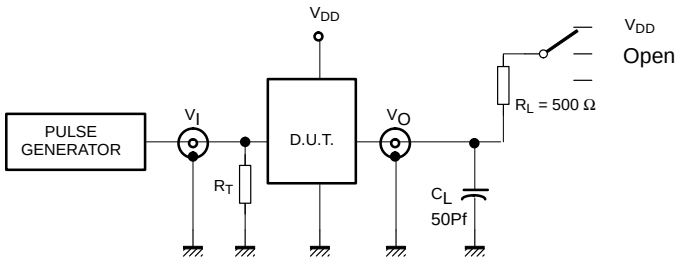


Figure 19. I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}



DEFINITIONS

R_L = Load resistor.

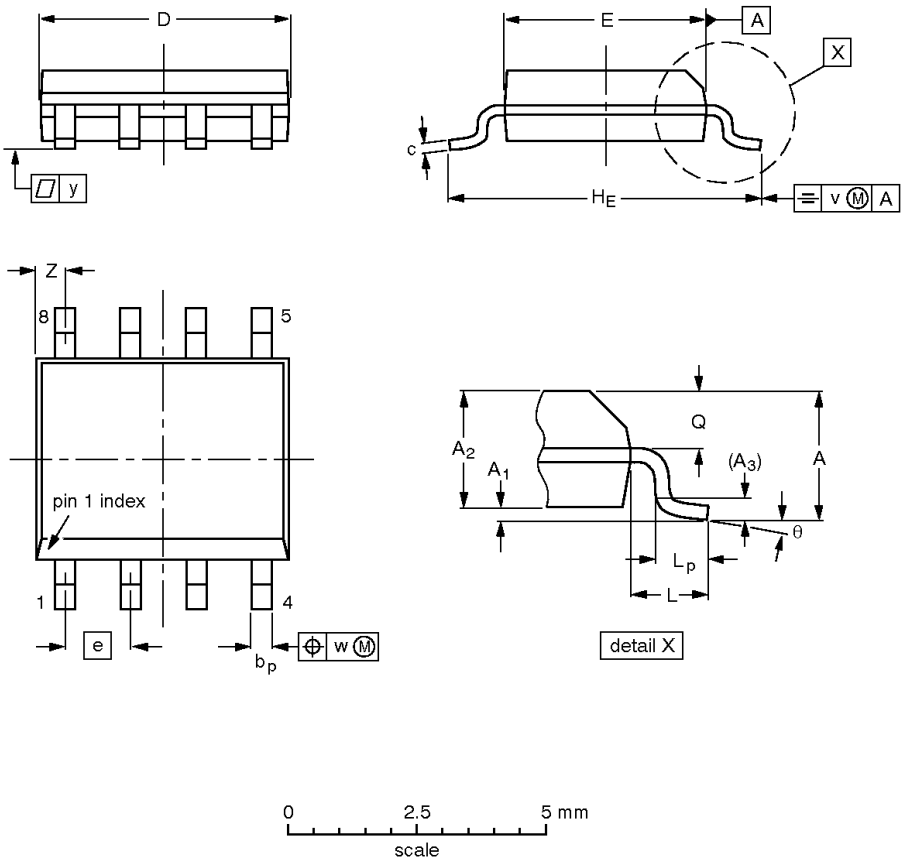
C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to the output impedance Z_O of the pulse generators.

SW02142

Figure 20. Test circuitry for switching times

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

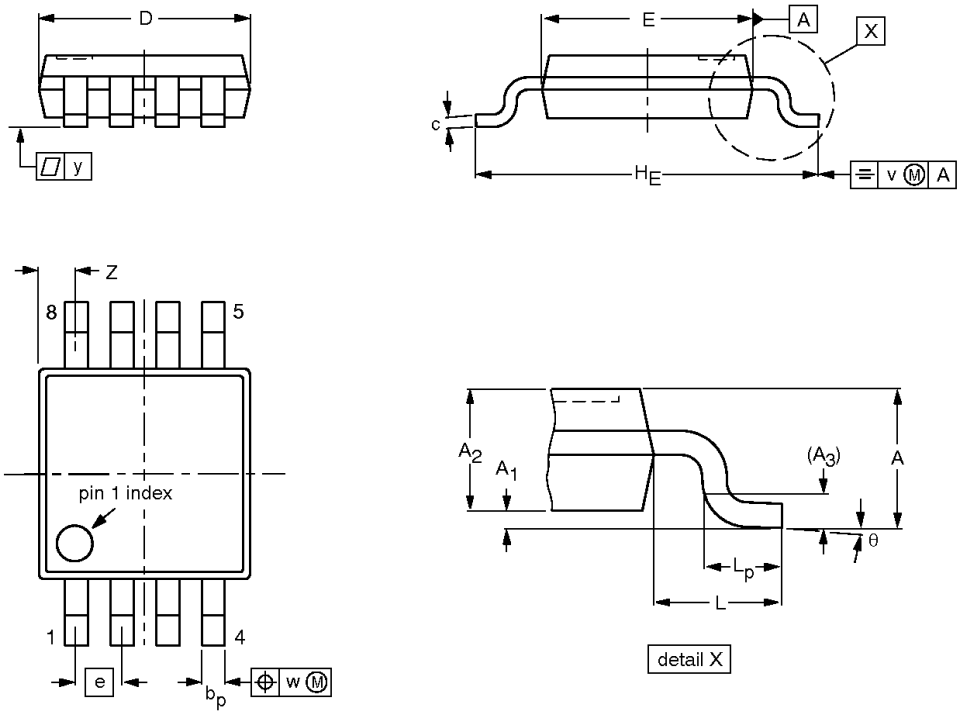
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

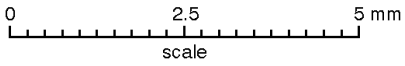
Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-1						~~99-04-09~~ 03-02-18

REVISION HISTORY

Rev	Date	Description
_1	20030919	**Product data (9397 750 12061); ECN 853-2404 30307 dated 08 September 2003.**

4-bit I²C LED dimmer PCA9533

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

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Date of release: 09-03

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